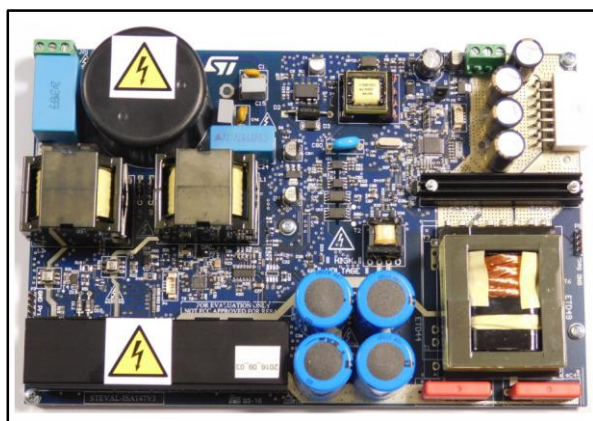


500 W fully digital AC-DC power supply (D-SMPS) based on STM32F334C8 microcontroller

Data brief



Features

- Input AC voltage: 90 V to 264 V
- Input AC frequency: 45 Hz to 65 Hz
- Nominal power: 500 W
- Output voltage: 12 V
- Semi-Bridgeless PFC stage
- DC-DC stage: resonant LLC with synchronous rectification
- Peak efficiency: 94%
- PFC switching frequency: 60 kHz
- DC-DC switching frequency: 80 kHz to 115 kHz (burst mode above)
- HF transformer isolation voltage: 4 kV
- Cooling: natural convection up to 300 W, forced cooling above 300 W
- PFC control: managed by STM32F051K8
- LLC control: managed by STM32F334C8
- Input short-circuit protection
- Input under/overvoltage protection
- Input under/overfrequency protection
- DC Bus under/overvoltage protection
- Output short-circuit protection
- Output under/overvoltage protection
- Overtemperature protection
- RoHS compliant

Description

The STEVAL-ISA147V3 is a digital switch mode AC-DC converter consisting of two power stages: an input semi-bridgeless power factor corrector (SBPFC) controlled by an STM32F051K8, and a regulation stage implemented with an LLC half bridge with synchronous rectification (SR), controlled by an STM32F334C8 microcontroller.

This 500 W AC-DC converter uses the so-called bridgeless PFC topology, with the advantage of lower conduction losses and higher efficiency by eliminating the need for a diode rectifier stage. This choice also allows a reduced component count compared to a standard PFC.

The input stage is typically controlled using an outer voltage loop for bus voltage regulation and an inner control loop to shape the current according to a sinusoidal waveform. The outer loop adjusts the current reference in order to maintain a regulated bus voltage, independent of load or input voltage variations. The output isolation and regulation stage is implemented using a half-bridge LLC topology, operating with constant duty cycle and variable frequency control.

1 Description continued

The DC-DC stage performs voltage step-down using an HF transformer with a primary to secondary turn ratio chosen to maintain good efficiency and regulation over the entire operating range. The transformer is supplied with a square wave voltage generated by the primary side active switches. On the secondary side, this voltage waveform is rectified and then smoothed by the output filter; on the primary side, switching losses are reduced thanks to zero voltage switching (ZVS). On the secondary side, synchronous rectification (SR) is used to ensure low conduction losses. The overall effect of these design choices is high system efficiency, in line with the stringent requirements of the power supply industry.

The system is controlled by two microcontrollers from the STM32 product family. On the primary side, an STM32F051K8 controls the bridgeless PFC by sampling the current of the two MOSFETs, the input AC voltage and the output bus voltage. Two control signals, PWM1 and PWM2, are then generated to drive two power switches. On the secondary side, an STM32F334C8 microcontroller samples the output voltage and adjusts the frequency of the LLC bridge control signals to ensure stable operation throughout the overall load range. In addition, two ADC channels are used to sample the rising and falling edges of the drain-to-source voltage of the SR MOSFETs. The two microcontrollers exchange information about the status of the input and output power stage via bidirectional serial communication.

Both the power stage and control stage are supplied by an offline flyback circuit which provides a suitable, regulated voltage to the microcontrollers, the gate drive ICs and signal conditioning circuits.

2 Schematic diagram

Figure 1: STEVAL-ISA147V3 circuit schematic (1 of 6)

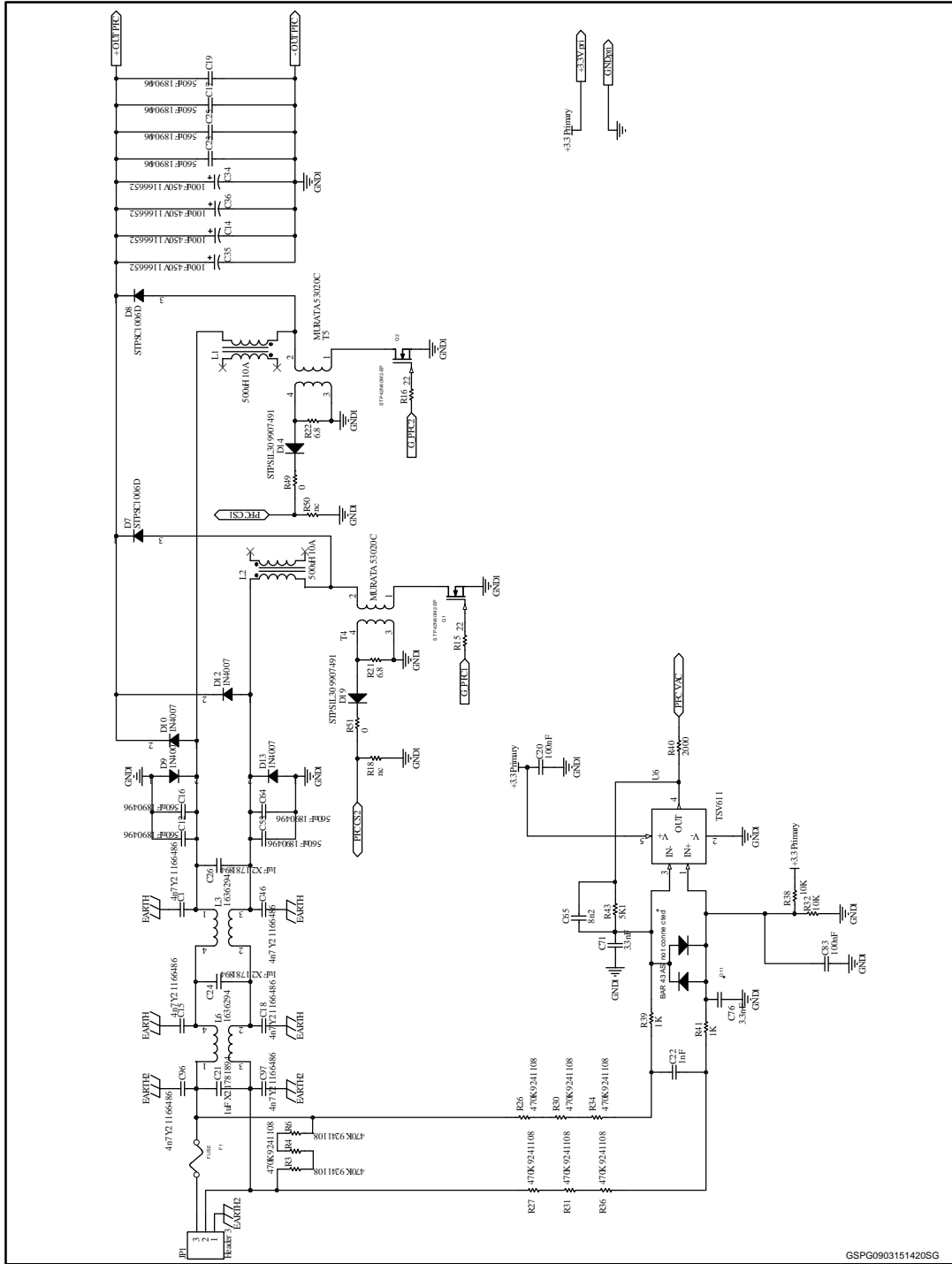


Figure 2: STEVAL-ISA147V3 circuit schematic (2 of 6)

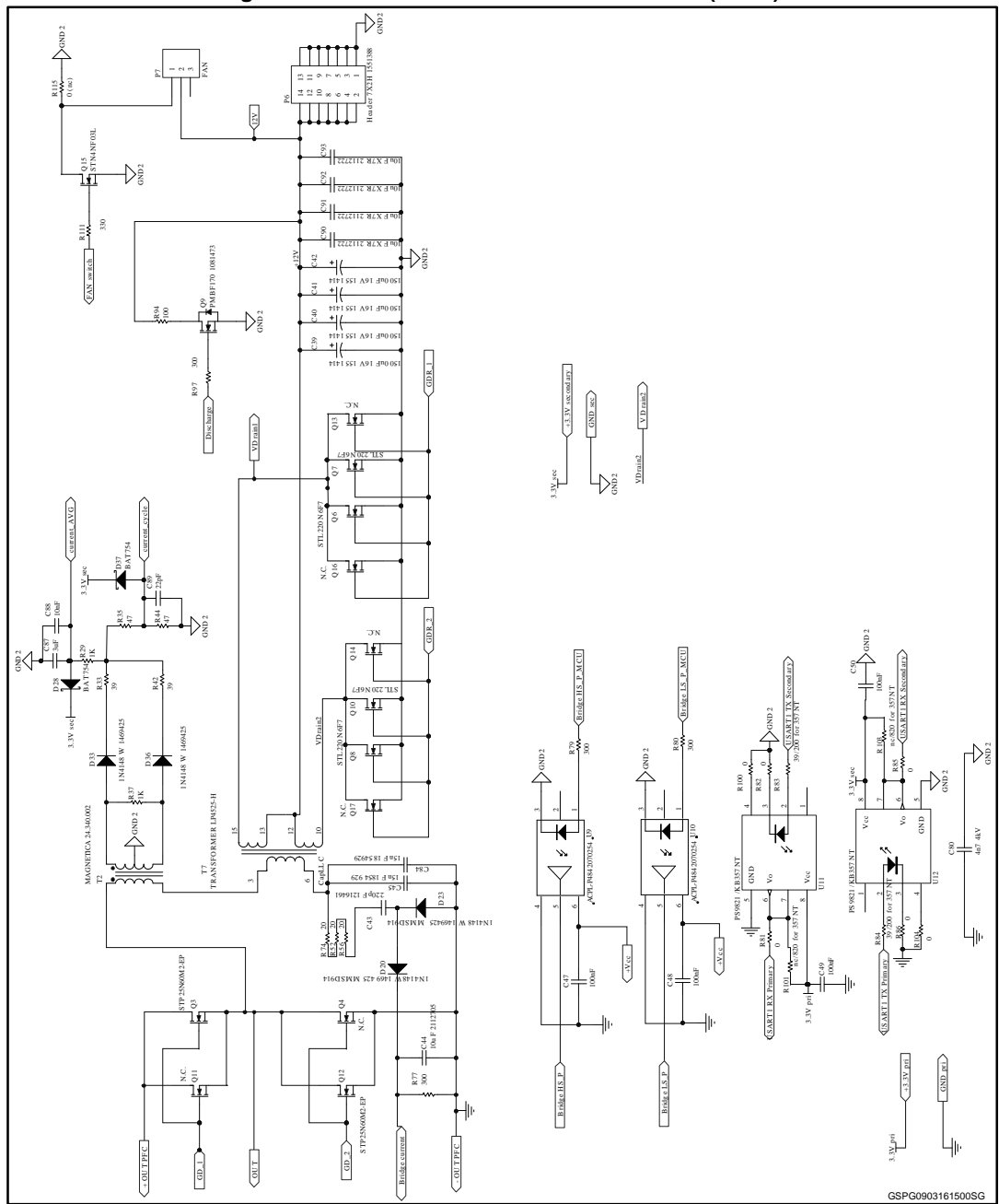


Figure 5: STEVAL-ISA147V3 circuit schematic (5 of 6)

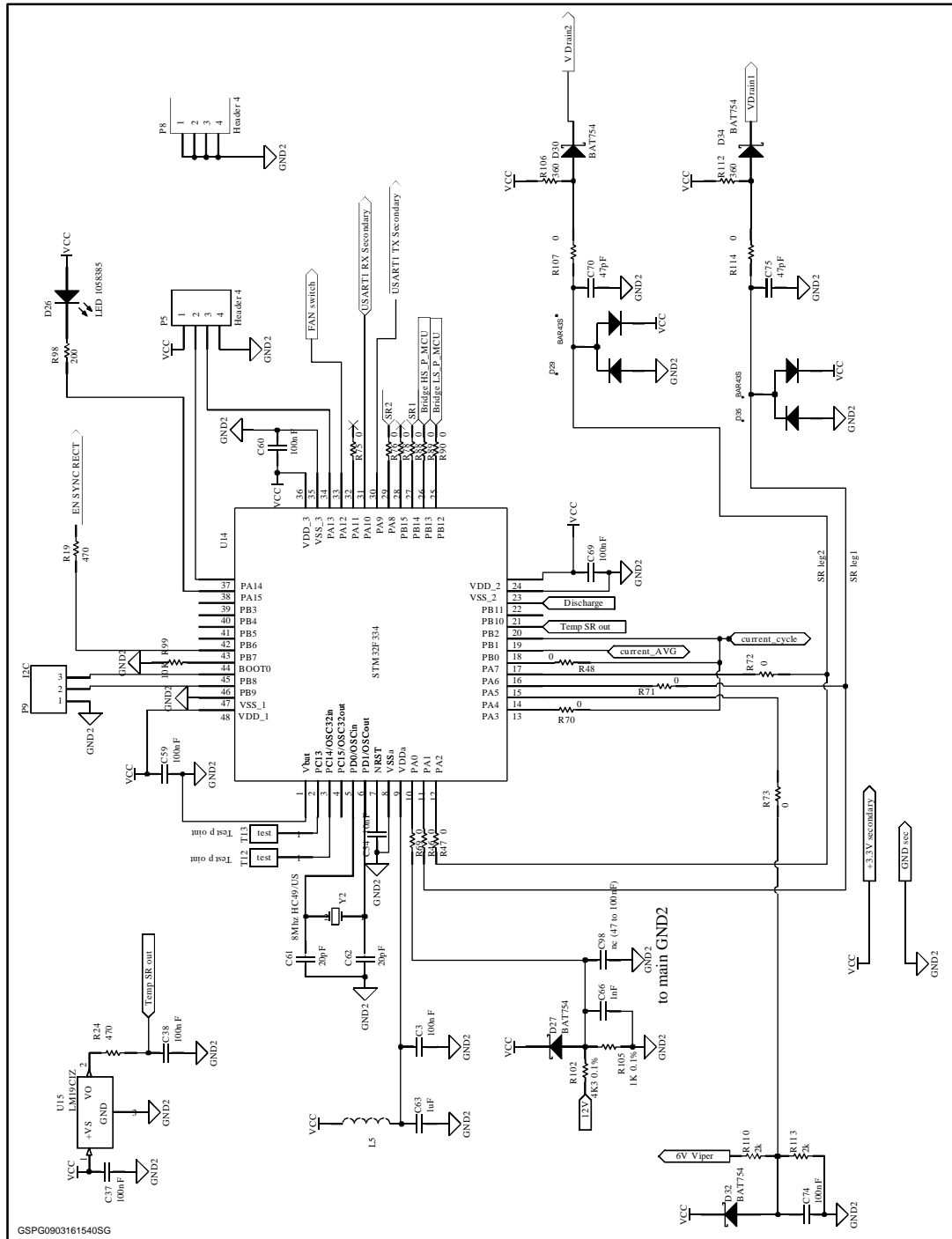
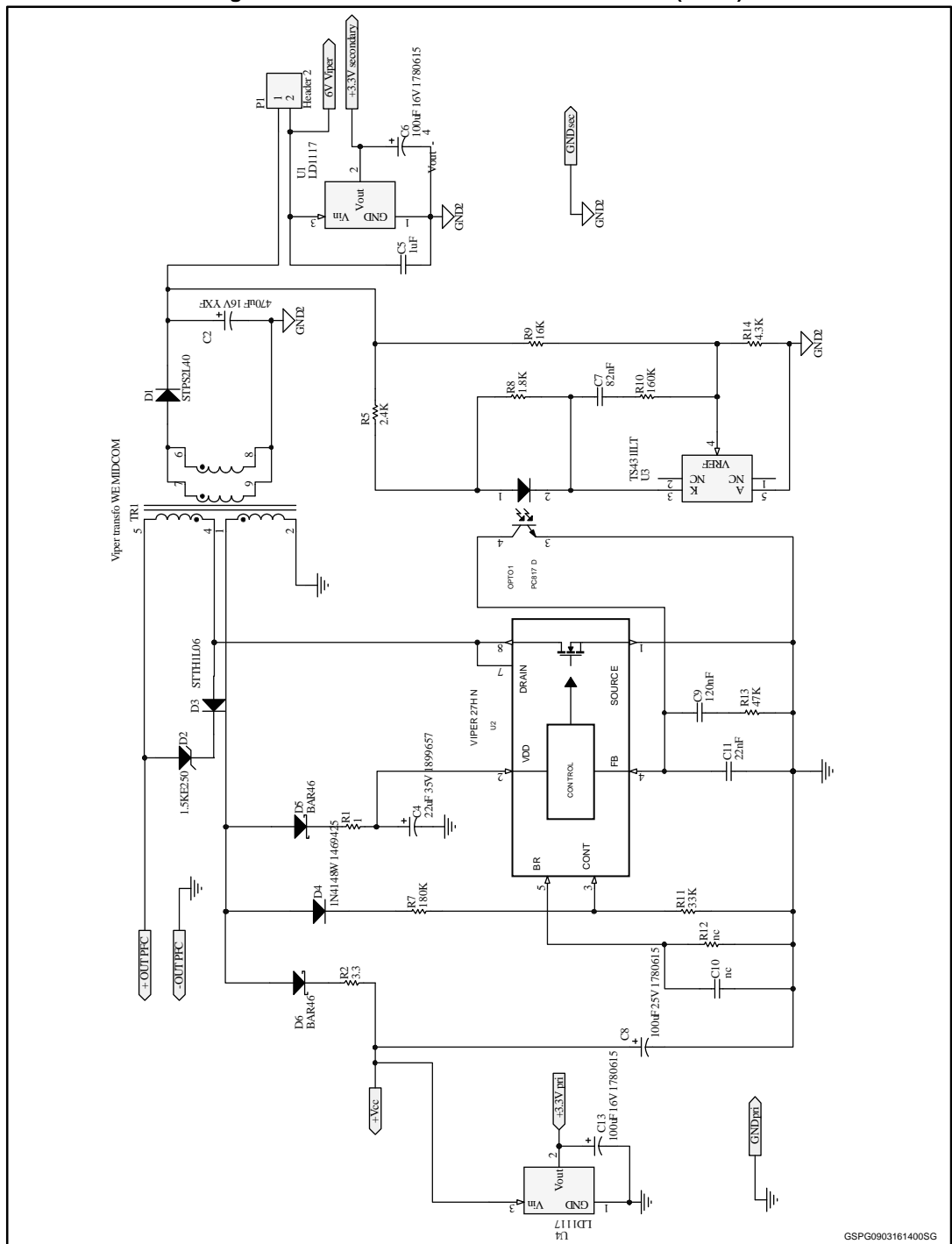


Figure 6: STEVAL-ISA147V3 circuit schematic (6 of 6)



GSPG0903161400SG

3 Revision history

Table 1: Document revision history

Date	Version	Changes
11-Mar-2016	1	Initial release.

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