

## 256K x 16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC SRAM

AUGUST 2014

### FEATURES

- High-speed access time: 55ns, 70ns
- CMOS low power operation  
36 mW (typical) operating  
9  $\mu$ W (typical) CMOS standby
- TTL compatible interface levels
- Single power supply  
1.65V--2.2V  $V_{DD}$  (IS62WV25616ALL)  
2.5V--3.6V  $V_{DD}$  (IS62WV25616BLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available
- Lead-free available

### DESCRIPTION

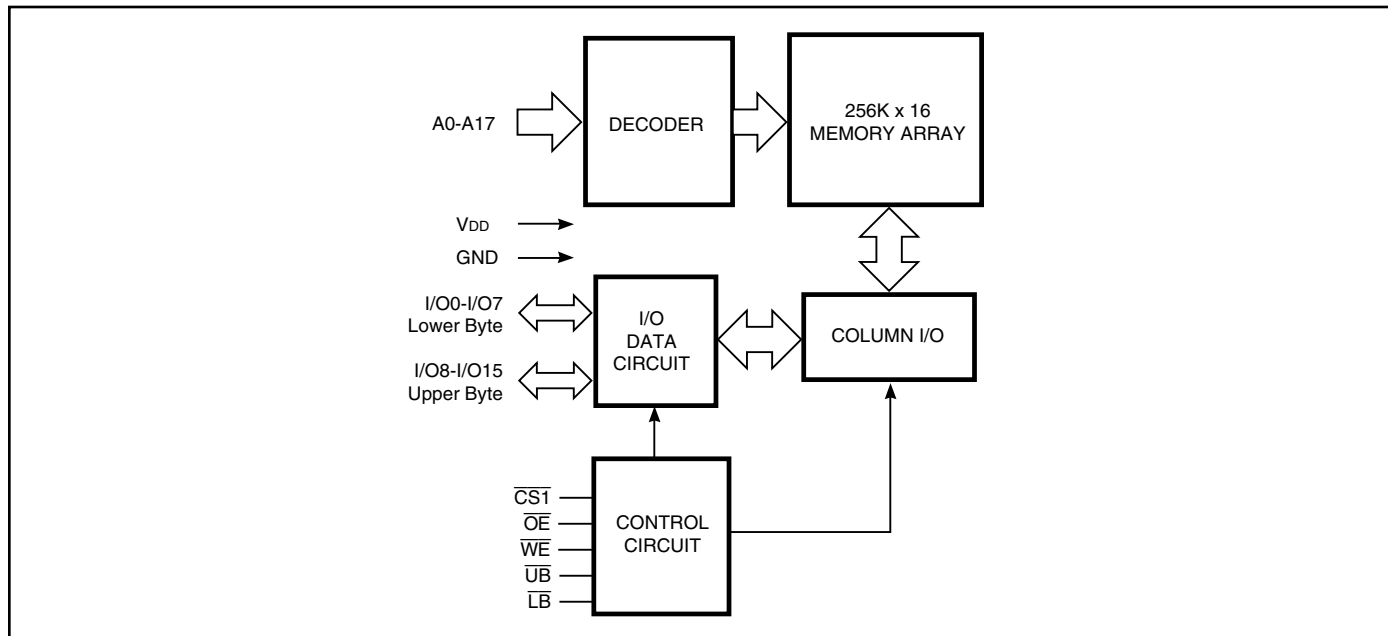
The *ISSI* IS62WV25616ALL/IS62WV25616BLL are high-speed, low power, 4M bit SRAMs organized as 256K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When  $\overline{CS1}$  is HIGH (deselected) or when  $\overline{CS1}$  is LOW and both  $\overline{LB}$  and  $\overline{UB}$  are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory. A data byte allows Upper Byte ( $\overline{UB}$ ) and Lower Byte ( $\overline{LB}$ ) access.

The IS62WV25616ALL/IS62WV25616BLL are packaged in the JEDEC standard 44-Pin TSOP (TYPE II) and 48-pin mini BGA (6mmx8mm).

### FUNCTIONAL BLOCK DIAGRAM



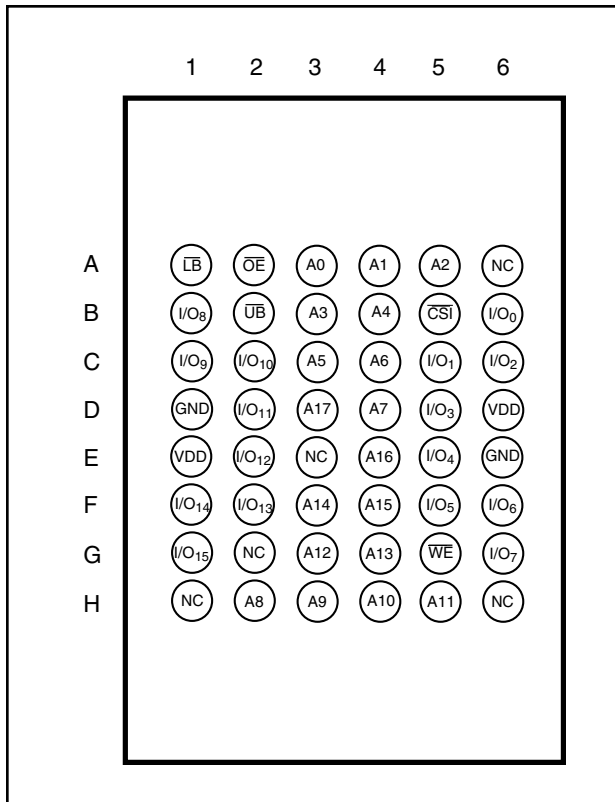
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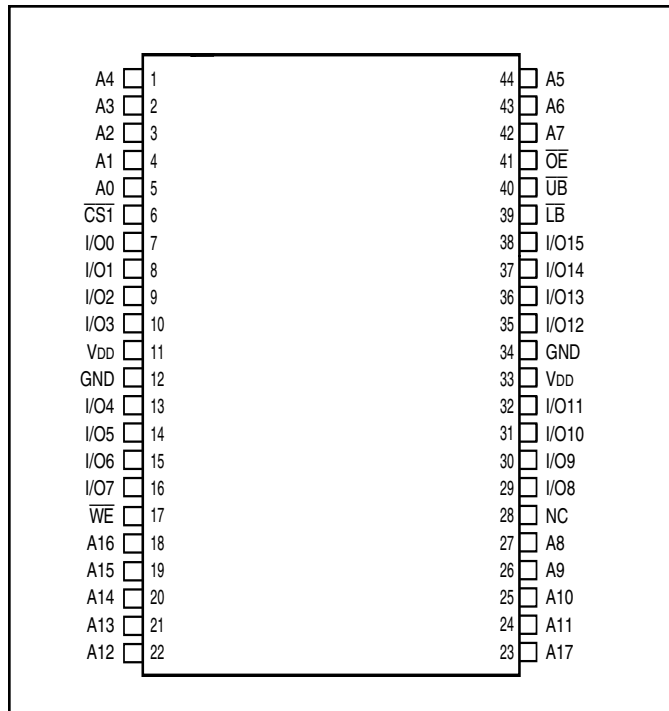
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- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

**PIN CONFIGURATIONS**

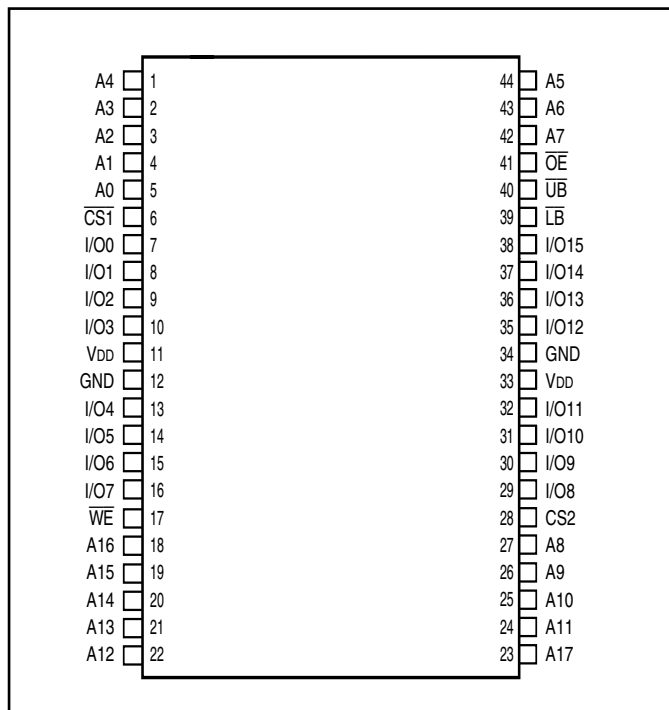
**48- ball mini BGA (6mm x 8mm)  
(Package Code B)**



**44-Pin mini TSOP (Type II)  
(Package Code T)**



**44-Pin mini TSOP (Type II)  
2 Chip Enable Option  
(Package Code T2)**



**PIN DESCRIPTIONS**

A0-A17	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
CS1, CS2	Chip Enable Input
OE	Output Enable Input
WE	Write Enable Input
LB	Lower-byte Control (I/O0-I/O7)
UB	Upper-byte Control (I/O8-I/O15)
NC	No Connection
VDD	Power
GND	Ground

**TRUTH TABLE**

Mode	$\overline{WE}$	$\overline{CS1}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN		V <sub>DD</sub> Current
						I/O0-I/O7	I/O8-I/O15	
Not Selected	X	H	X	X	X	High-Z	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
	X	X	X	H	H	High-Z	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
Output Disabled	H	L	H	L	X	High-Z	High-Z	I <sub>CC</sub>
	H	L	H	X	L	High-Z	High-Z	I <sub>CC</sub>
Read	H	L	L	L	H	DOUT	High-Z	I <sub>CC</sub>
	H	L	L	H	L	High-Z	DOUT	
	H	L	L	L	L	DOUT	DOUT	
Write	L	L	X	L	H	DIN	High-Z	I <sub>CC</sub>
	L	L	X	H	L	High-Z	DIN	
	L	L	X	L	L	DIN	DIN	

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.2 to V <sub>DD</sub> +0.3	V
V <sub>DD</sub>	V <sub>DD</sub> Related to GND	-0.2 to V <sub>DD</sub> +0.3	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W

**Note:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**OPERATING RANGE (V<sub>DD</sub>)**

Range	Ambient Temperature	IS62WV25616ALL	IS62WV25616BLL
Commercial	0°C to +70°C	1.65V - 2.2V	2.5V-3.6V
Industrial	-40°C to +85°C	1.65V - 2.2V	2.5V-3.6V

**DC ELECTRICAL CHARACTERISTICS (Over Operating Range)**

Symbol	Parameter	Test Conditions	V <sub>DD</sub>	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	1.65-2.2V	1.4	—	V
		I <sub>OH</sub> = -1 mA	2.5-3.6V	2.2	—	V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA	1.65-2.2V	—	0.2	V
		I <sub>OL</sub> = 2.1 mA	2.5-3.6V	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage		1.65-2.2V	1.4	V <sub>DD</sub> + 0.2	V
			2.5-3.6V	2.2	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub> <sup>(1)</sup>	Input LOW Voltage		1.65-2.2V	-0.2	0.4	V
			2.5-3.6V	-0.2	0.8	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>		-1	1	μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> , Outputs Disabled		-1	1	μA

**Notes:** 1. V<sub>IL</sub> (min.) = -1.0V for pulse width less than 10 ns.

# IS62WV25616ALL, IS62WV25616BLL

## IS62WV25616ALL, POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 70	Unit
I <sub>CC</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = Max.,	Com.	25	mA
		I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Ind.	30	
I <sub>CC1</sub>	Operating Supply Current	V <sub>DD</sub> = Max., $\overline{CS1} = 0.2V$	Com.	10	mA
		$\overline{WE} = V_{DD} - 0.2V$ f = 1MHz	Ind.	10	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CS1} = V_{IH}$ , f = 1 MHz	Com. Ind.	0.35 0.35	mA
	ULB Control	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CS1} = V_{IL}$ , f = 0, $\overline{UB} = V_{IH}$ , $\overline{LB} = V_{IH}$			
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max., $\overline{CS1} \geq V_{DD} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	Com. Ind.	15 15	μA
	ULB Control	V <sub>DD</sub> = Max., $\overline{CS1} = V_{IL}$ , V <sub>IN</sub> ≤ 0.2V, f = 0; $\overline{UB} / \overline{LB} = V_{DD} - 0.2V$			

## IS62WV25616BLL, POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 55	Max. 70	Unit
I <sub>CC</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = Max.,	Com.	40	35	mA
		I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Ind.	45	40	
I <sub>CC1</sub>	Operating Supply Current	V <sub>DD</sub> = Max., $\overline{CS1} = 0.2V$	Com.	15	15	mA
		$\overline{WE} = V_{DD} - 0.2V$ f = 1MHz	Ind.	15	15	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CS1} = V_{IH}$ , f = 1 MHz	Com. Ind.	0.35 0.35	0.35 0.35	mA
	ULB Control	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CS1} = V_{IL}$ , f = 0, $\overline{UB} = V_{IH}$ , $\overline{LB} = V_{IH}$				
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max., $\overline{CS1} \geq V_{DD} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	Com. Ind.	15 15	15 15	μA
	ULB Control	V <sub>DD</sub> = Max., $\overline{CS1} = V_{IL}$ , V <sub>IN</sub> ≤ 0.2V, f = 0; $\overline{UB} / \overline{LB} = V_{DD} - 0.2V$	typ. <sup>(1)</sup>	3		

Note:

1. Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C. Not 100% tested.

**CAPACITANCE<sup>(1)</sup>**

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	8	pF
C <sub>OUT</sub>	Input/Output Capacitance	V <sub>OUT</sub> = 0V	10	pF

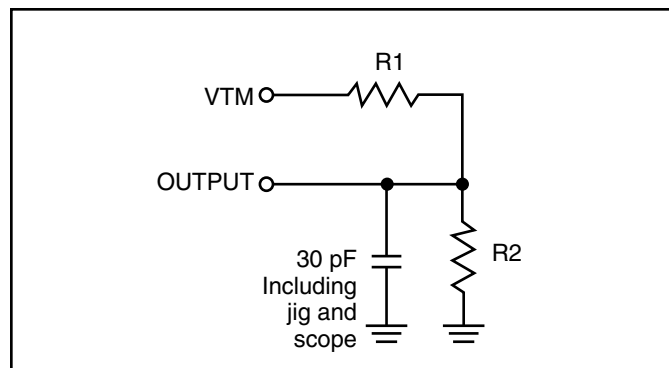
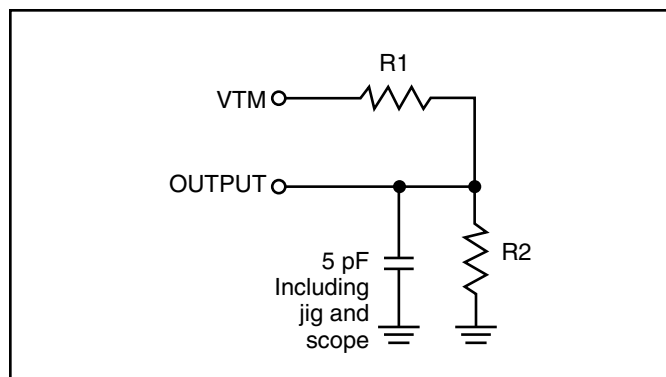
**Note:**

1. Tested initially and after any design or process changes that may affect these parameters.

**AC TEST CONDITIONS**

Parameter	IS62WV25616ALL (Unit)	IS62WV25616BLL (Unit)
Input Pulse Level	0.4V to V <sub>DD</sub> -0.2V	0.4V to V <sub>DD</sub> -0.3V
Input Rise and Fall Times	5 ns	5ns
Input and Output Timing and Reference Level	V <sub>REF</sub>	V <sub>REF</sub>
Output Load	See Figures 1 and 2	See Figures 1 and 2

	IS62WV25616ALL 1.65V-2.2V	IS62WV25616BLL 2.5V - 3.6V
R1(Ω)	3070	3070
R2(Ω)	3150	3150
V <sub>REF</sub>	0.9V	1.5V
V <sub>TM</sub>	1.8V	2.8V

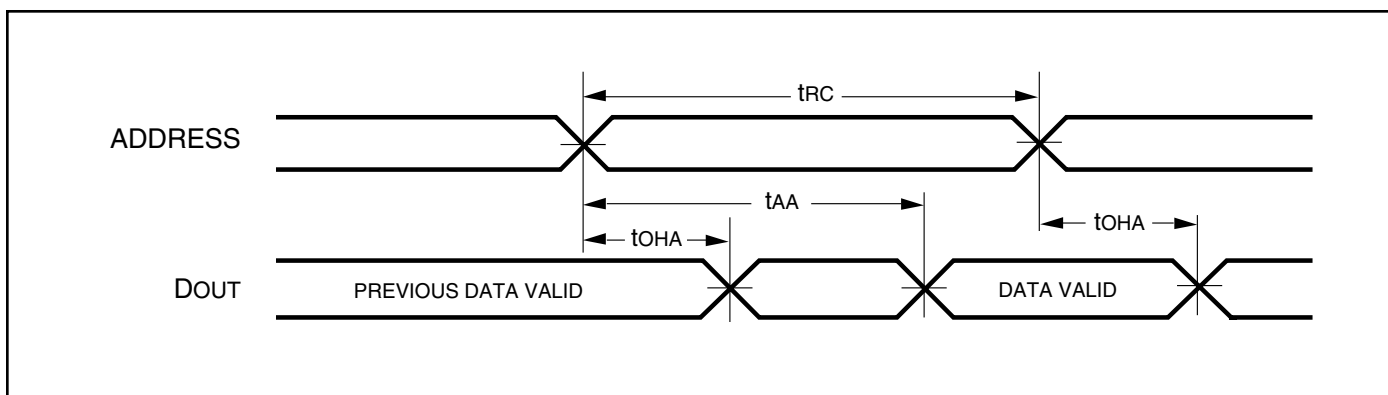
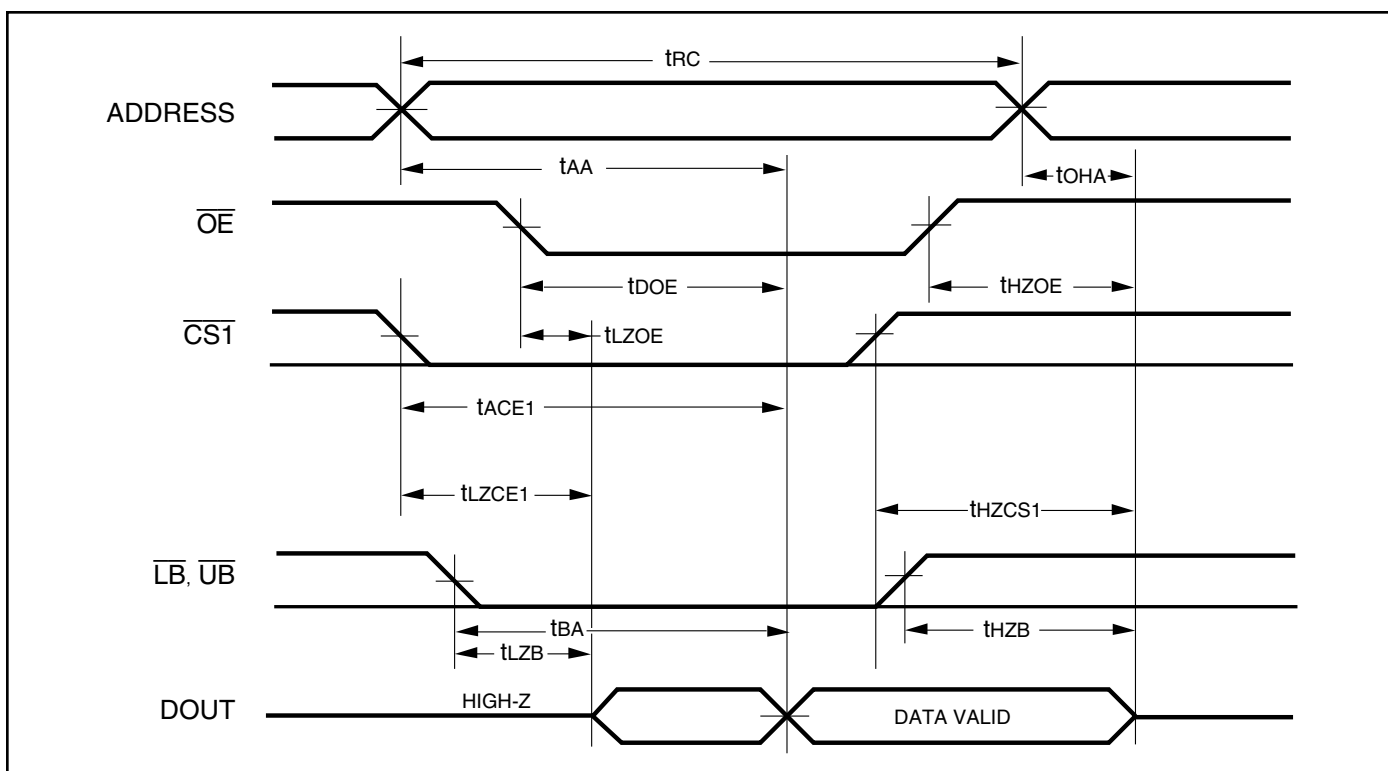
**AC TEST LOADS**

**Figure 1**

**Figure 2**

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

Symbol	Parameter	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	55	—	70	—	ns
t <sub>AA</sub>	Address Access Time	—	55	—	70	ns
t <sub>OHA</sub>	Output Hold Time	10	—	10	—	ns
t <sub>ACS1</sub>	$\overline{CS1}$ Access Time	—	55	—	70	ns
t <sub>DOE</sub>	$\overline{OE}$ Access Time	—	25	—	35	ns
t <sub>HZOE<sup>(2)</sup></sub>	$\overline{OE}$ to High-Z Output	—	20	—	25	ns
t <sub>LZOE<sup>(2)</sup></sub>	$\overline{OE}$ to Low-Z Output	5	—	5	—	ns
t <sub>HZCS1</sub>	$\overline{CS1}$ to High-Z Output	0	20	0	25	ns
t <sub>LZCS1</sub>	$\overline{CS1}$ to Low-Z Output	10	—	10	—	ns
t <sub>BA</sub>	$\overline{LB}$ , $\overline{UB}$ Access Time	—	55	—	70	ns
t <sub>HZB</sub>	$\overline{LB}$ , $\overline{UB}$ to High-Z Output	0	20	0	25	ns
t <sub>LZB</sub>	$\overline{LB}$ , $\overline{UB}$ to Low-Z Output	0	—	0	—	ns

**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V<sub>DD</sub>-0.2V/V<sub>DD</sub>-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

**AC WAVEFORMS**
**READ CYCLE NO. 1<sup>(1,2)</sup>** (Address Controlled) ( $\overline{CS1} = \overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$ ,  $\overline{UB}$  or  $\overline{LB} = V_{IL}$ )

**READ CYCLE NO. 2<sup>(1,3)</sup>** ( $\overline{CS1}$ ,  $\overline{OE}$ , AND  $\overline{UB}/\overline{LB}$  Controlled)

**Notes:**

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CS1}$ ,  $\overline{UB}$ , or  $\overline{LB} = V_{IL}$ .  $\overline{WE} = V_{IH}$ .
3. Address is valid prior to or coincident with  $\overline{CS1}$  LOW transition.

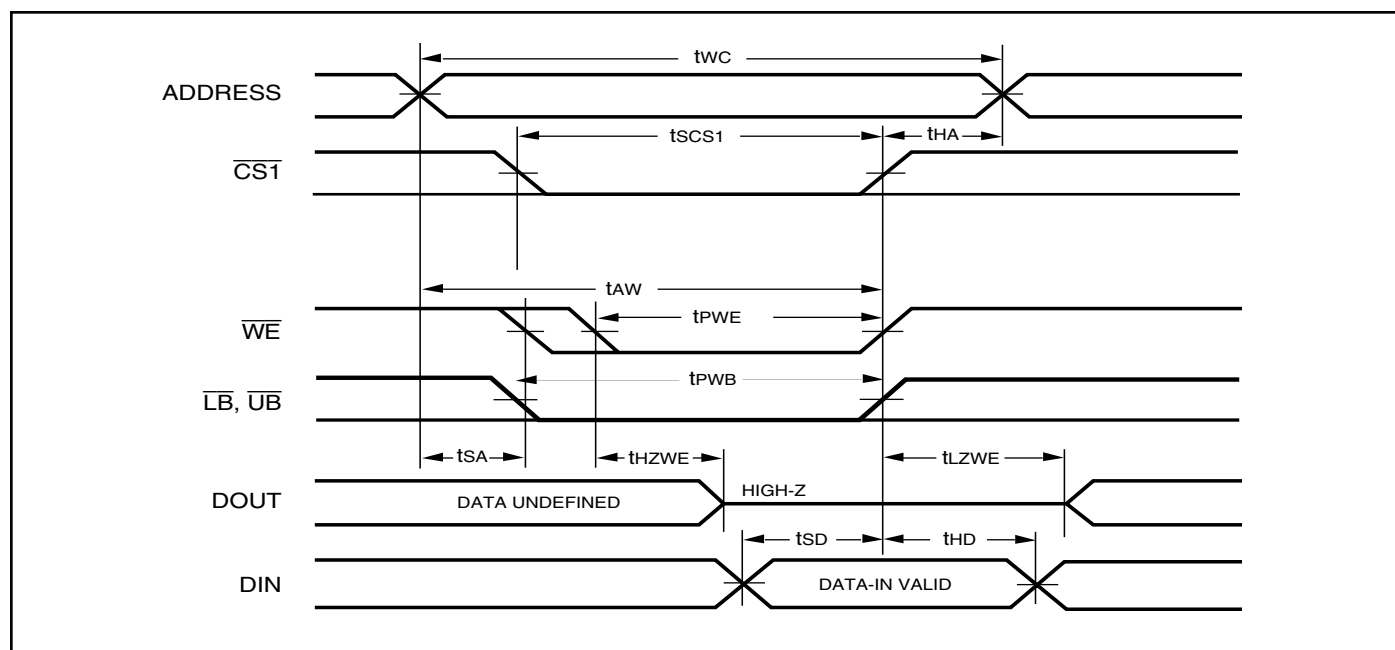
**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup>** (Over Operating Range)

Symbol	Parameter	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
t <sub>wc</sub>	Write Cycle Time	55	—	70	—	ns
t <sub>sCS1</sub>	$\overline{CS1}$ to Write End	45	—	60	—	ns
t <sub>aw</sub>	Address Setup Time to Write End	45	—	60	—	ns
t <sub>ha</sub>	Address Hold from Write End	0	—	0	—	ns
t <sub>sa</sub>	Address Setup Time	0	—	0	—	ns
t <sub>pWB</sub>	$\overline{LB}$ , $\overline{UB}$ Valid to End of Write	45	—	60	—	ns
t <sub>pWE</sub>	$\overline{WE}$ Pulse Width	40	—	50	—	ns
t <sub>sd</sub>	Data Setup to Write End	25	—	30	—	ns
t <sub>hd</sub>	Data Hold from Write End	0	—	0	—	ns
t <sub>hzWE<sup>(3)</sup></sub>	$\overline{WE}$ LOW to High-Z Output	—	20	—	20	ns
t <sub>lzWE<sup>(3)</sup></sub>	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	ns

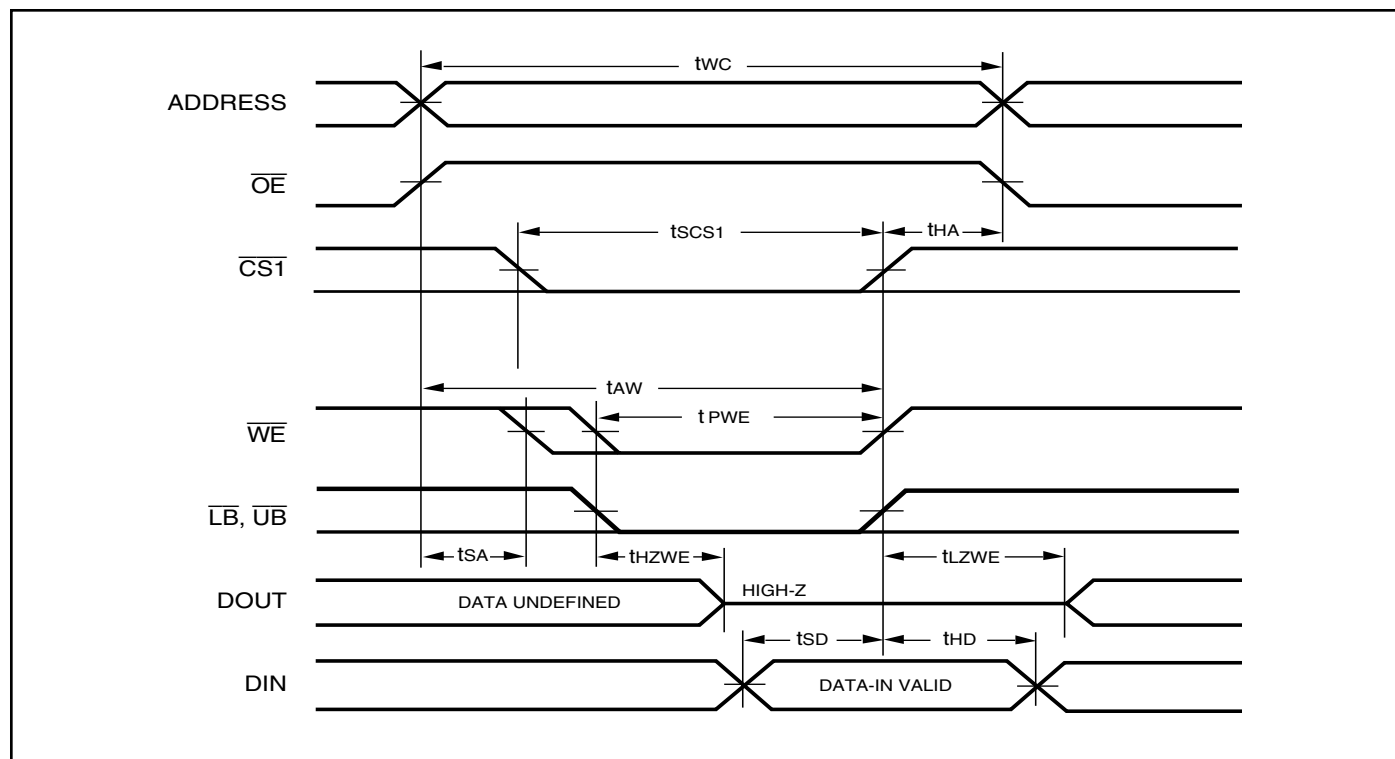
**Notes:**

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4V to V<sub>DD</sub>-0.2V/V<sub>DD</sub>-0.3V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of  $\overline{CS1}$  LOW and  $\overline{UB}$  or  $\overline{LB}$ , and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

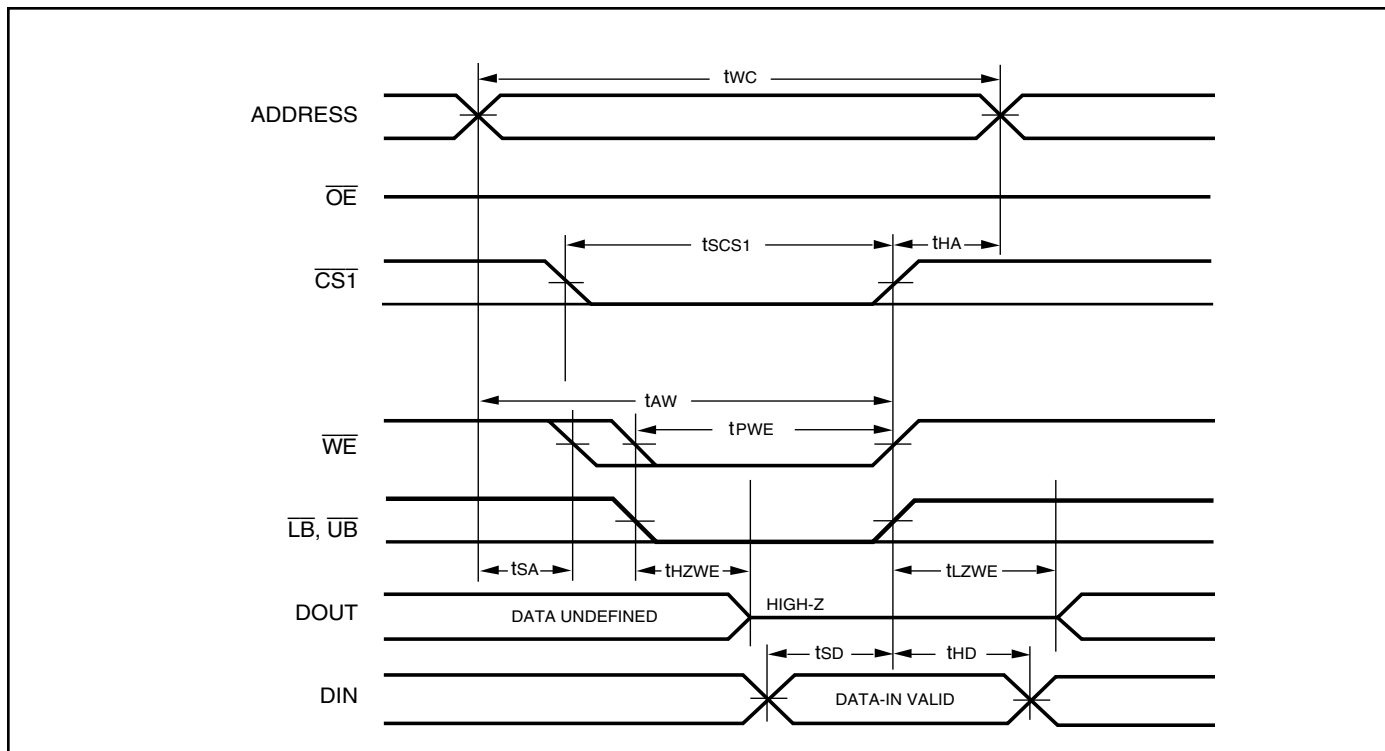


**AC WAVEFORMS**
**WRITE CYCLE NO. 1<sup>(1,2)</sup> ( $\overline{CS1}$  Controlled,  $\overline{OE}$  = HIGH or LOW)**

**Notes:**

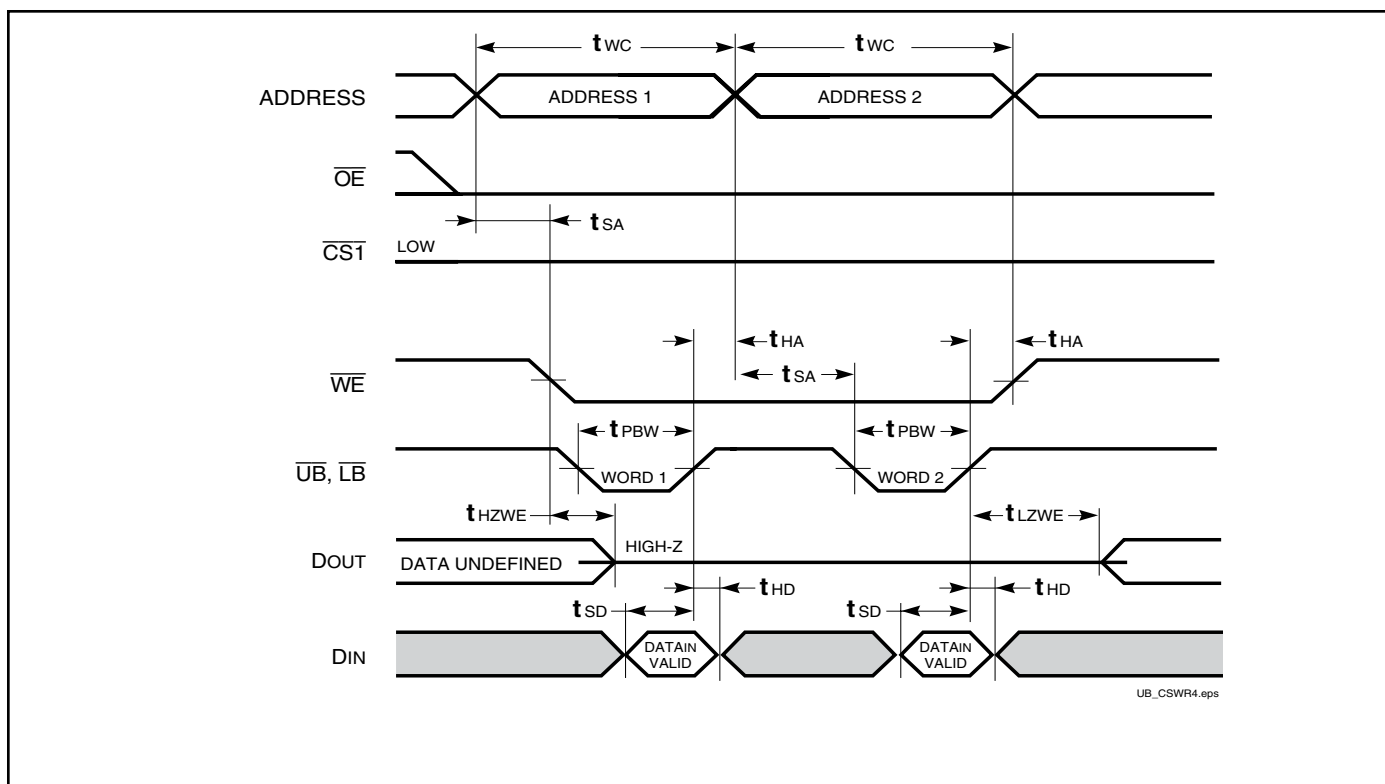
1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the  $\overline{CS1}$  and  $\overline{WE}$  inputs and at least one of the  $\overline{LB}$  and  $\overline{UB}$  inputs being in the LOW state.
2.  $WRITE = (\overline{CS1}) [ (\overline{LB}) = (\overline{UB}) ] (\overline{WE})$ .

**WRITE CYCLE NO. 2 ( $\overline{WE}$  Controlled:  $\overline{OE}$  is HIGH During Write Cycle)**


**WRITE CYCLE NO. 3** ( $\overline{OE}$  Controlled:  $\overline{OE}$  is LOW During Write Cycle)



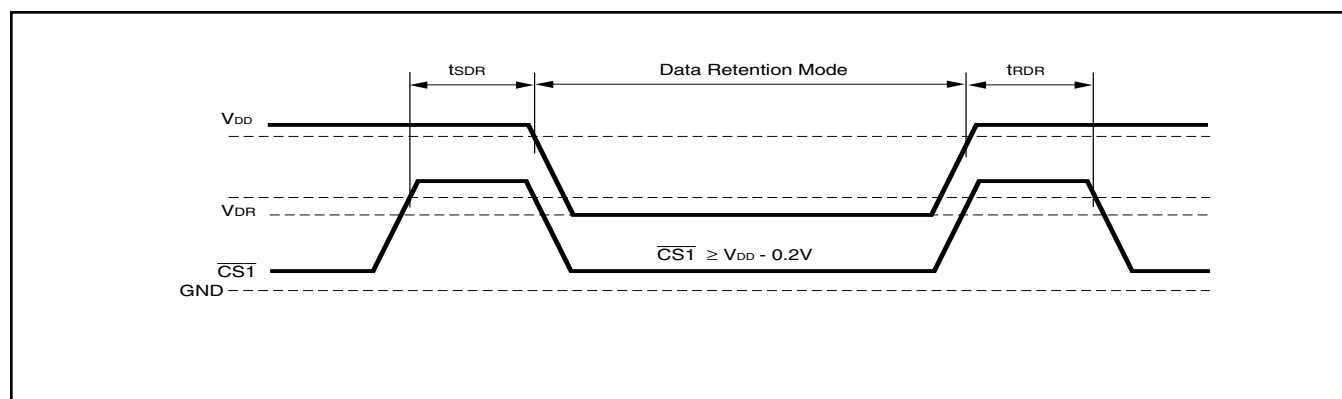
**WRITE CYCLE NO. 4** ( $\overline{UB}/\overline{LB}$  Controlled)



UB\_CSWR4.eps

**DATA RETENTION SWITCHING CHARACTERISTICS**

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V <sub>DR</sub>	V <sub>DD</sub> for Data Retention	See Data Retention Waveform	1.2	3.6	V
I <sub>DR</sub>	Data Retention Current	V <sub>DD</sub> = 1.2V, $\overline{CS1} \geq V_{DD} - 0.2V$	—	15	μA
t <sub>SDR</sub>	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t <sub>RDR</sub>	Recovery Time	See Data Retention Waveform	t <sub>RC</sub>	—	ns

**DATA RETENTION WAVEFORM ( $\overline{CS1}$  Controlled)**


## IS62WV25616ALL, IS62WV25616BLL

### ORDERING INFORMATION

#### IS62WV25616ALL (1.65V-2.2V)

##### Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
70	IS62WV25616ALL-70T	TSOP

##### Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
70	IS62WV25616ALL-70TI	TSOP
70	IS62WV25616ALL-70BI	mini BGA (6mmx8mm)
70	IS62WV25616ALL-70BLI	mini BGA (6mmx8mm), Lead-free

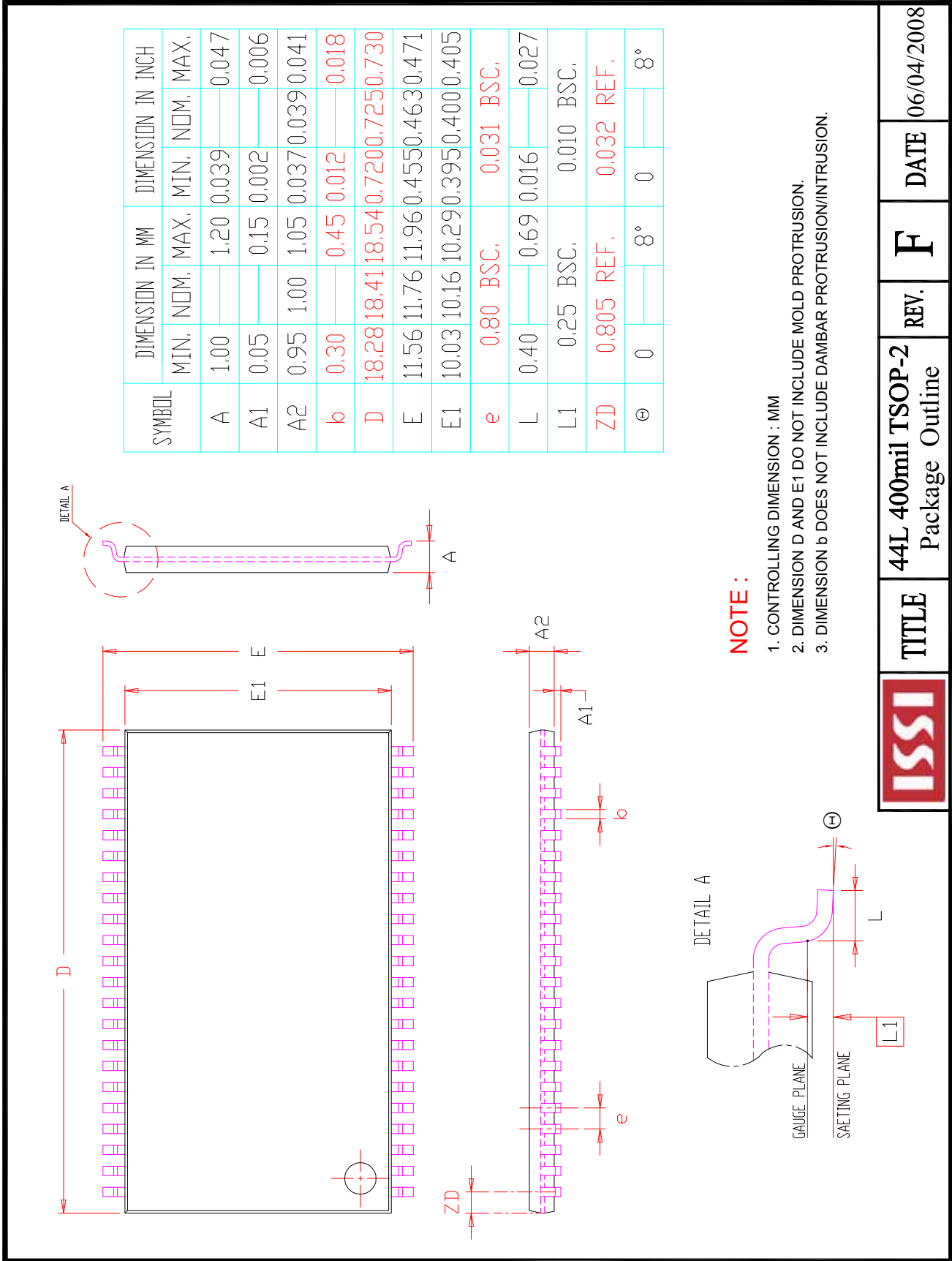
#### IS62WV25616BLL (2.5V - 3.6V)

##### Commercial Range: 0°C to +70°C

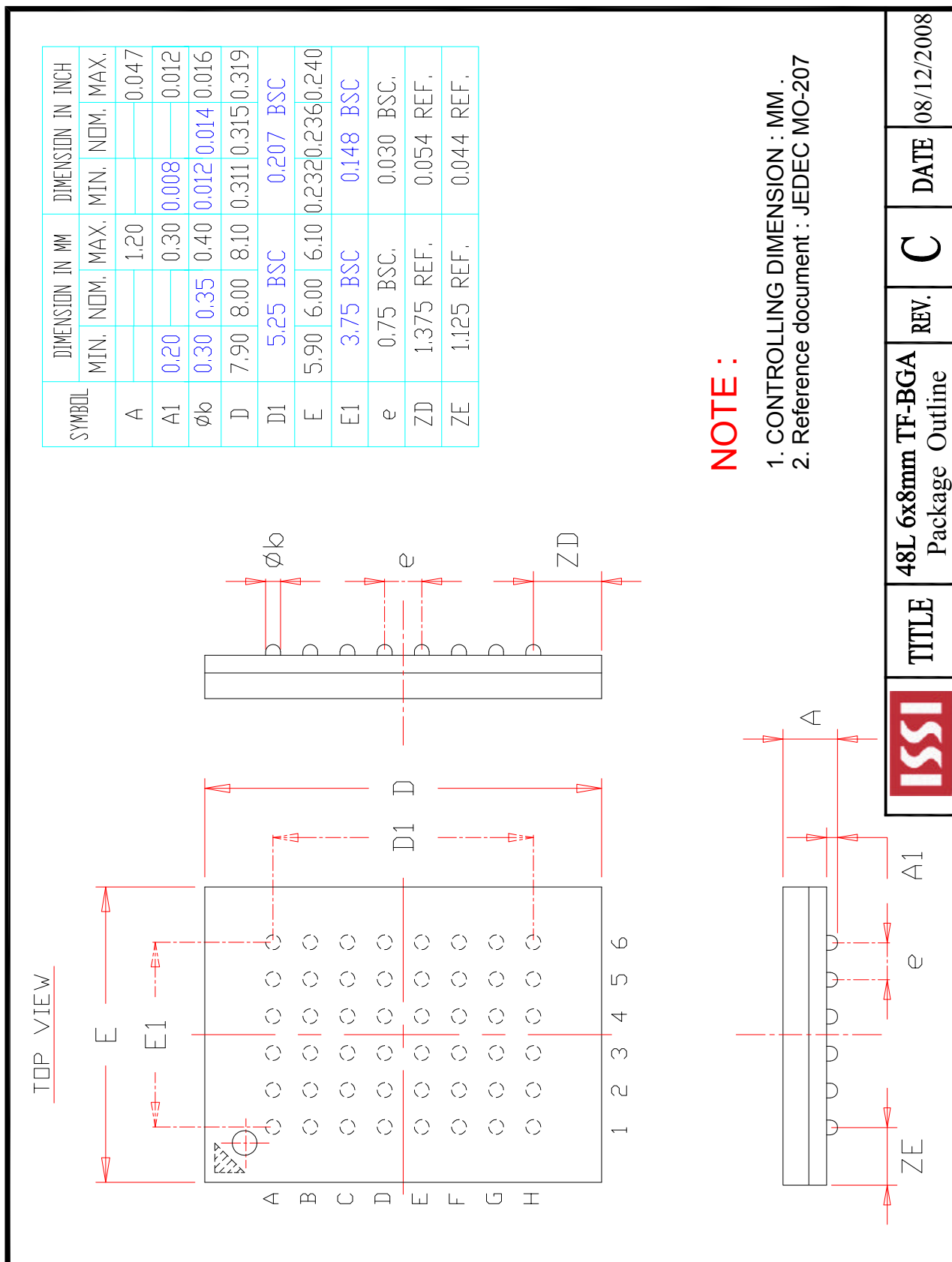
Speed (ns)	Order Part No.	Package
55	IS62WV25616BLL-55T	TSOP
70	IS62WV25616BLL-70T	TSOP

##### Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS62WV25616BLL-55TI	TSOP
55	IS62WV25616BLL-55TLI	TSOP, Lead-free
55	IS62WV25616BLL-55T2LI	TSOP, Lead-free, 2 CS Option
55	IS62WV25616BLL-55BI	mini BGA (6mmx8mm)
55	IS62WV25616BLL-55BLI	mini BGA (6mmx8mm), Lead-free



	<b>TITLE</b>	<b>REV.</b>	<b>DATE</b>
	44L 400mil TSOP-2 Package Outline	F	06/04/2008



SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.20	0.30	0.008	0.012
$\phi b$	0.30	0.40	0.012	0.014
D	7.90	8.00	0.311	0.315
D1	5.25	BSC	0.207	BSC
E	5.90	6.00	0.232	0.236
E1	3.75	BSC	0.148	BSC
e	0.75	BSC.	0.030	BSC.
ZD	1.375	REF.	0.054	REF.
ZE	1.125	REF.	0.044	REF.

**NOTE :**

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207

	TITLE	48L 6x8mm TF-BGA Package Outline	REV.	C	DATE	08/12/2008
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