

MC74HC4066A

Quad Analog Switch/ Multiplexer/Demultiplexer High-Performance Silicon-Gate CMOS

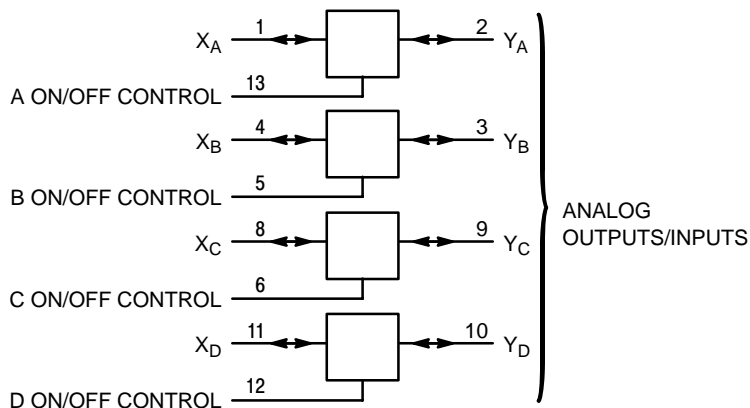
The MC74HC4066A utilizes silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF-channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full power-supply range (from V_{CC} to GND).

The HC4066A is identical in pinout to the metal-gate CMOS MC14016 and MC14066. Each device has four independent switches. The device has been designed so the ON resistances (R_{ON}) are more linear over input voltage than R_{ON} of metal-gate CMOS analog switches.

The ON/OFF control inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. For analog switches with voltage-level translators, see the HC4316A.

- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Wide Power-Supply Voltage Range ($V_{CC} - GND$) = 2.0 to 12.0 Volts
- Analog Input Voltage Range ($V_{CC} - GND$) = 2.0 to 12.0 Volts
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14016 or MC14066
- Low Noise
- Chip Complexity: 44 FETs or 11 Equivalent Gates

LOGIC DIAGRAM



ANALOG INPUTS/OUTPUTS = X_A, X_B, X_C, X_D
PIN 14 = V_{CC}
PIN 7 = GND

FUNCTION TABLE

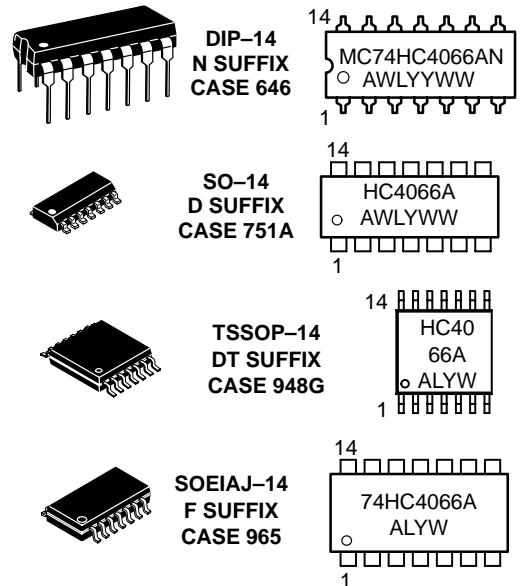
| On/Off Control Input | State of Analog Switch |
|----------------------|------------------------|
| L | Off |
| H | On |



ON Semiconductor®

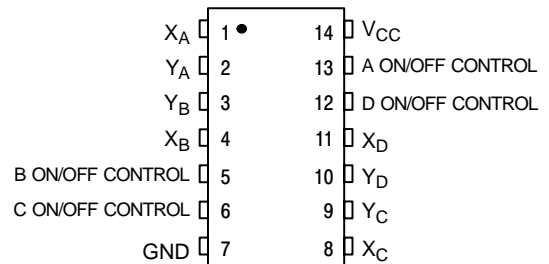
<http://onsemi.com>

MARKING DIAGRAMS



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

| Device | Package | Shipping |
|-----------------|----------|-------------|
| MC74HC4066AN | DIP-14 | 2000 / Box |
| MC74HC4066ADR2 | SO-14 | 2500 / Reel |
| MC74HC4066ADT | TSSOP-14 | 96 / Rail |
| MC74HC4066ADTR2 | TSSOP-14 | 2500 / Reel |

MC74HC4066A

MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|------------------|---|--------------------------------|------|
| V _{CC} | Positive DC Supply Voltage (Referenced to GND) | - 0.5 to + 14.0 | V |
| V _{IS} | Analog Input Voltage (Referenced to GND) | - 0.5 to V _{CC} + 0.5 | V |
| V _{in} | Digital Input Voltage (Referenced to GND) | - 0.5 to V _{CC} + 0.5 | V |
| I | DC Current Into or Out of Any Pin | ± 25 | mA |
| P _D | Power Dissipation in Still Air, Plastic DIP† EIAJ/SOIC Package† TSSOP Package† | 750 | mW |
| | | 500 | |
| | | 450 | |
| T _{stg} | Storage Temperature | - 65 to + 150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package) | 260 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

EIAJ/SOIC Package: - 7 mW/°C from 65° to 125°C

TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit | |
|---------------------------------|---|--------------------------|-----------------|------|----|
| V _{CC} | Positive DC Supply Voltage (Referenced to GND) | 2.0 | 12.0 | V | |
| V _{IS} | Analog Input Voltage (Referenced to GND) | GND | V _{CC} | V | |
| V _{in} | Digital Input Voltage (Referenced to GND) | GND | V _{CC} | V | |
| V _{IO} * | Static or Dynamic Voltage Across Switch | - | 1.2 | V | |
| T _A | Operating Temperature, All Package Types | -55 | + 125 | °C | |
| t _r , t _f | Input Rise and Fall Time, ON/OFF Control Inputs (Figure 10) | V _{CC} = 2.0 V | 0 | 1000 | ns |
| | | V _{CC} = 3.0 V | 0 | 600 | |
| | | V _{CC} = 4.5 V | 0 | 500 | |
| | | V _{CC} = 9.0 V | 0 | 400 | |
| | | V _{CC} = 12.0 V | 0 | 250 | |

*For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTIC Digital Section (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|-----------------|--|---|----------------------|------------------|-----------|------------|------|
| | | | | - 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| V _{IH} | Minimum High-Level Voltage ON/OFF Control Inputs | R _{on} = Per Spec | 2.0 | 1.5 | 1.5 | 1.5 | V |
| | | | 3.0 | 2.1 | 2.1 | 2.1 | |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 9.0 | 6.3 | 6.3 | 6.3 | |
| | | | 12.0 | 8.4 | 8.4 | 8.4 | |
| V _{IL} | Maximum Low-Level Voltage ON/OFF Control Inputs | R _{on} = Per Spec | 2.0 | 0.5 | 0.5 | 0.5 | V |
| | | | 3.0 | 0.9 | 0.9 | 0.9 | |
| | | | 4.5 | 1.35 | 1.35 | 1.35 | |
| | | | 9.0 | 2.7 | 2.7 | 2.7 | |
| | | | 12.0 | 3.6 | 3.6 | 3.6 | |
| I _{in} | Maximum Input Leakage Current ON/OFF Control Inputs | V _{in} = V _{CC} or GND | 12.0 | ± 0.1 | ± 1.0 | ± 1.0 | µA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{in} = V _{CC} or GND V _{IO} = 0 V | 6.0 | 2 | 20 | 40 | µA |
| | | | 12.0 | 4 | 40 | 160 | |

NOTE: Information on typical parametric values can be found in the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

MC74HC4066A

DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limit | | | Unit |
|------------------|--|---|----------------------|------------------|--------|---------|------|
| | | | | - 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| R _{on} | Maximum "ON" Resistance | V _{in} = V _{IH} V _{IS} = V _{CC} to GND I _S ≤ 2.0 mA (Figures 1, 2) | 2.0† | – | – | – | Ω |
| | | | 3.0† | – | – | – | |
| | | | 4.5 | 120 | 160 | 200 | |
| | | | 9.0 | 70 | 85 | 100 | |
| | | | 12.0 | 70 | 85 | 100 | |
| | | V _{in} = V _{IH} V _{IS} = V _{CC} or GND (Endpoints) I _S ≤ 2.0 mA (Figures 1, 2) | 2.0 | – | – | – | |
| | | | 3.0 | – | – | – | |
| | | | 4.5 | 70 | 85 | 120 | |
| | | | 9.0 | 50 | 60 | 80 | |
| | | | 12.0 | 50 | 60 | 80 | |
| ΔR _{on} | Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package | V _{in} = V _{IH} V _{IS} = 1/2 (V _{CC} – GND) I _S ≤ 2.0 mA | 2.0 | – | – | – | Ω |
| | | | 4.5 | 20 | 25 | 30 | |
| | | | 9.0 | 15 | 20 | 25 | |
| | | | 12.0 | 15 | 20 | 25 | |
| I _{off} | Maximum Off-Channel Leakage Current, Any One Channel | V _{in} = V _{IL} V _{IO} = V _{CC} or GND Switch Off (Figure 3) | 12.0 | 0.1 | 0.5 | 1.0 | μA |
| I _{on} | Maximum On-Channel Leakage Current, Any One Channel | V _{in} = V _{IH} V _{IS} = V _{CC} or GND (Figure 4) | 12.0 | 0.1 | 0.5 | 1.0 | μA |

†At supply voltage (V_{CC}) approaching 3 V the analog switch-on resistance becomes extremely non-linear. Therefore, for low-voltage operation, it is recommended that these devices only be used to control digital signals.

NOTE: Information on typical parametric values can be found in the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, ON/OFF Control Inputs: t_r = t_f = 6 ns)

| Symbol | Parameter | V _{CC} V | Guaranteed Limit | | | Unit | |
|--|---|---------------------------|------------------|--------|---------|------|----|
| | | | - 55 to 25°C | ≤ 85°C | ≤ 125°C | | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9) | 2.0 | 40 | 50 | 60 | ns | |
| | | 3.0 | 30 | 40 | 50 | | |
| | | 4.5 | 10 | 13 | 15 | | |
| | | 9.0 | 10 | 13 | 15 | | |
| | | 12.0 | 10 | 13 | 15 | | |
| t _{PLZ} , t _{PHZ} | Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11) | 2.0 | 80 | 90 | 110 | ns | |
| | | 3.0 | 60 | 70 | 80 | | |
| | | 4.5 | 30 | 38 | 45 | | |
| | | 9.0 | 25 | 28 | 30 | | |
| | | 12.0 | 25 | 28 | 30 | | |
| t _{PZL} , t _{PZH} | Maximum Propagation Delay, ON/OFF Control to Analog Output (Figures 10 and 11) | 2.0 | 80 | 90 | 100 | ns | |
| | | 3.0 | 45 | 50 | 60 | | |
| | | 4.5 | 25 | 32 | 37 | | |
| | | 9.0 | 25 | 32 | 37 | | |
| | | 12.0 | 25 | 32 | 37 | | |
| C | Maximum Capacitance | ON/OFF Control Input | – | 10 | 10 | 10 | pF |
| | | Control Input = GND | – | 35 | 35 | 35 | |
| | | Analog I/O Feedthrough | – | 1.0 | 1.0 | 1.0 | |

NOTES:

- For propagation delays with loads other than 50 pF, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).
- Information on typical parametric values can be found in the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

| C _{PD} | Power Dissipation Capacitance (Per Switch) (Figure 13)* | Typical @ 25°C, V _{CC} = 5.0 V | | | pF |
|-----------------|---|---|--|--|----|
| | | 15 | | | |
| | | 15 | | | |

*Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

MC74HC4066A

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

| Symbol | Parameter | Test Conditions | V _{CC} V | Limit* 25°C 54/74HC | Unit |
|--------|--|--|--|--|------------------|
| BW | Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 5) | f _{in} = 1 MHz Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{OS} Increase f _{in} Frequency Until dB Meter Reads - 3 dB R _L = 50 Ω, C _L = 10 pF | 4.5 9.0 12.0 | 150 160 160 | MHz |
| - | Off-Channel Feedthrough Isolation (Figure 6) | f _{in} ≡ Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{IS} f _{in} = 10 kHz, R _L = 600 Ω, C _L = 50 pF f _{in} = 1.0 MHz, R _L = 50 Ω, C _L = 10 pF | 4.5 9.0 12.0 4.5 9.0 12.0 | - 50 - 50 - 50 - 40 - 40 - 40 | dB |
| - | Feedthrough Noise, Control to Switch (Figure 7) | V _{in} ≤ 1 MHz Square Wave (t _r = t _f = 6 ns) Adjust R _L at Setup so that I _S = 0 A R _L = 600 Ω, C _L = 50 pF R _L = 10 kΩ, C _L = 10 pF | 4.5 9.0 12.0 4.5 9.0 12.0 | 60 130 200 30 65 100 | mV _{PP} |
| - | Crosstalk Between Any Two Switches (Figure 12) | f _{in} ≡ Sine Wave Adjust f _{in} Voltage to Obtain 0 dBm at V _{IS} f _{in} = 10 kHz, R _L = 600 Ω, C _L = 50 pF f _{in} = 1.0 MHz, R _L = 50 Ω, C _L = 10 pF | 4.5 9.0 12.0 4.5 9.0 12.0 | - 70 - 70 - 70 - 80 - 80 - 80 | dB |
| THD | Total Harmonic Distortion (Figure 14) | f _{in} = 1 kHz, R _L = 10 kΩ, C _L = 50 pF THD = THD _{Measured} - THD _{Source} V _{IS} = 4.0 V _{PP} sine wave V _{IS} = 8.0 V _{PP} sine wave V _{IS} = 11.0 V _{PP} sine wave | 4.5 9.0 12.0 | 0.10 0.06 0.04 | % |

*Guaranteed limits not tested. Determined by design and verified by qualification.

MC74HC4066A

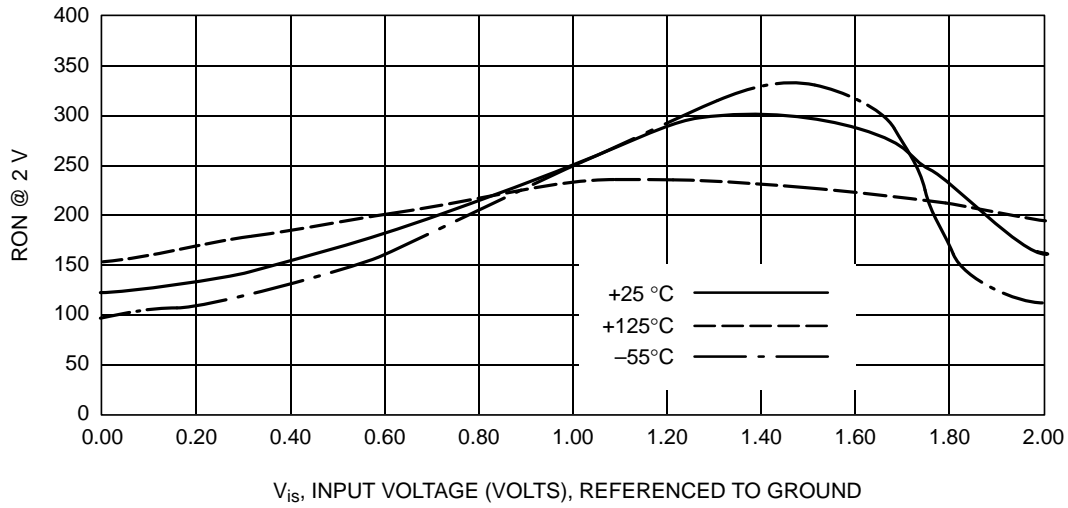


Figure 1a. Typical On Resistance, V_{CC} = 2.0 V

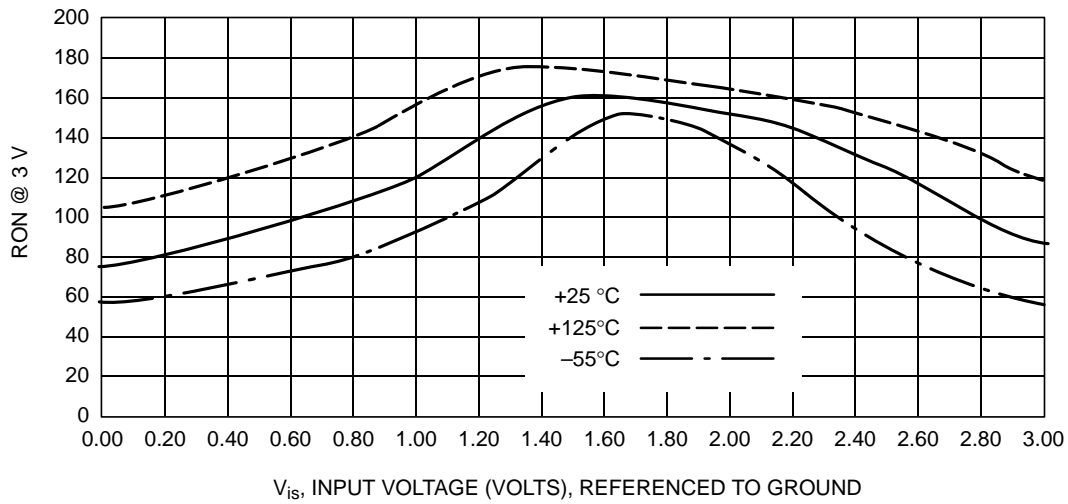


Figure 1b. Typical On Resistance, V_{CC} = 3.0 V

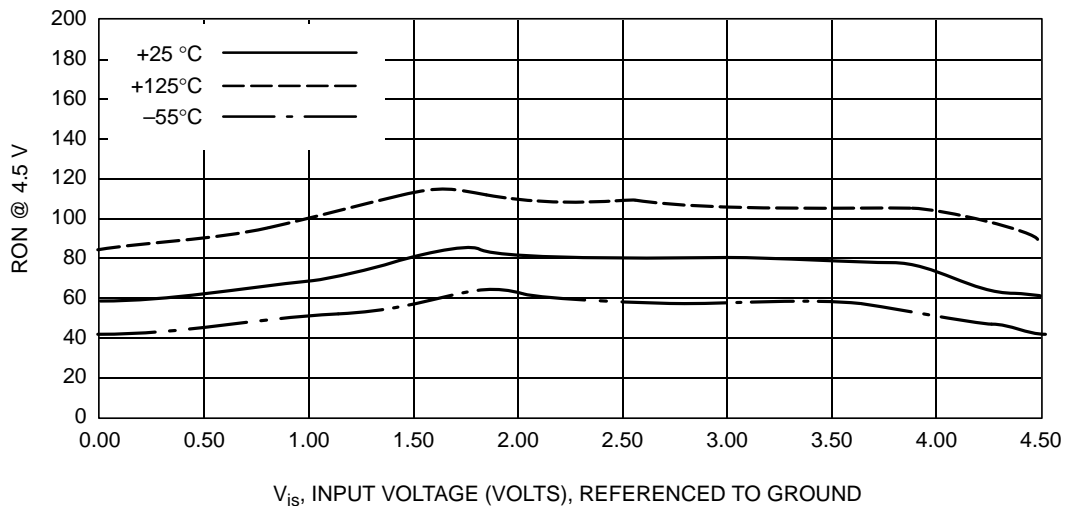


Figure 1c. Typical On Resistance, V_{CC} = 4.5 V

MC74HC4066A

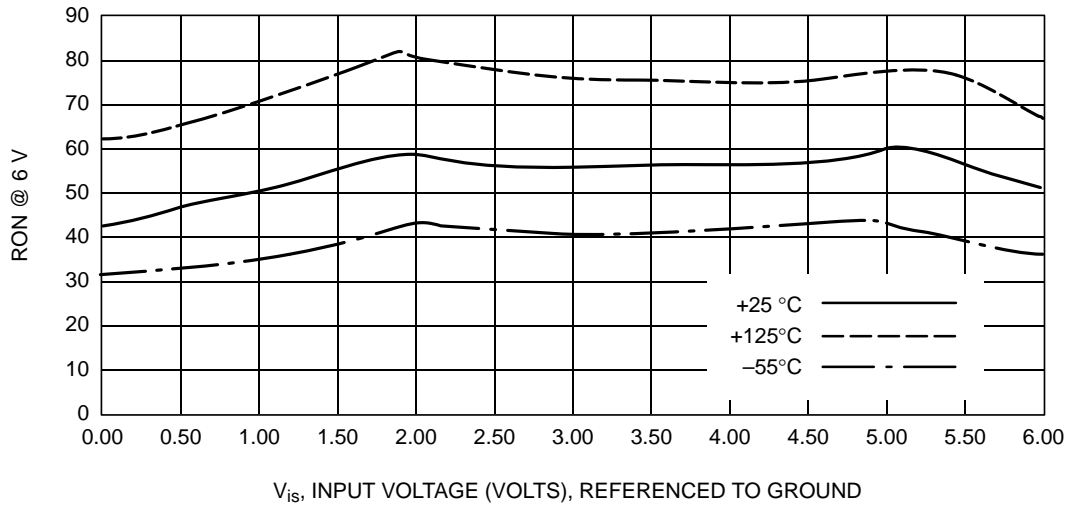


Figure 1d. Typical On Resistance, $V_{CC} = 6.0\text{ V}$

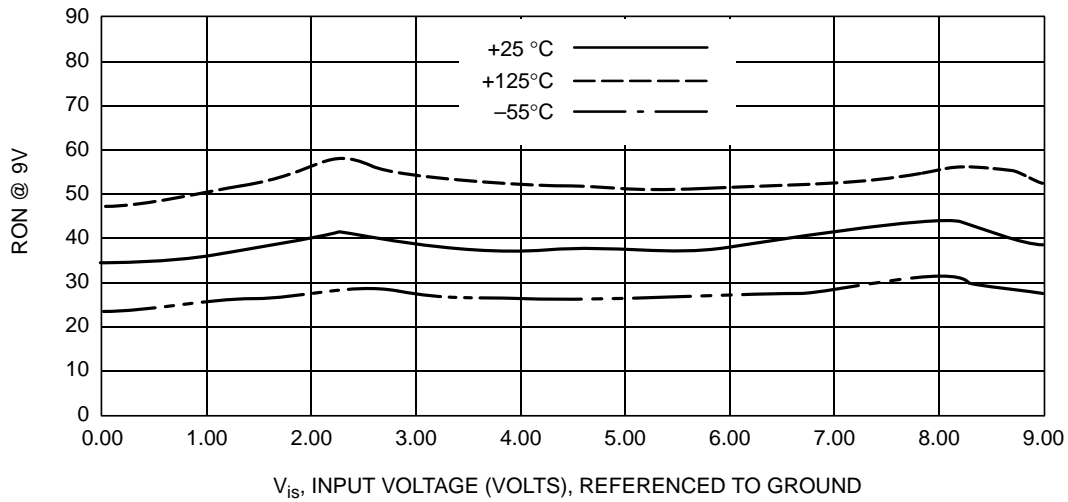


Figure 1e. Typical On Resistance, $V_{CC} = 9.0\text{ V}$

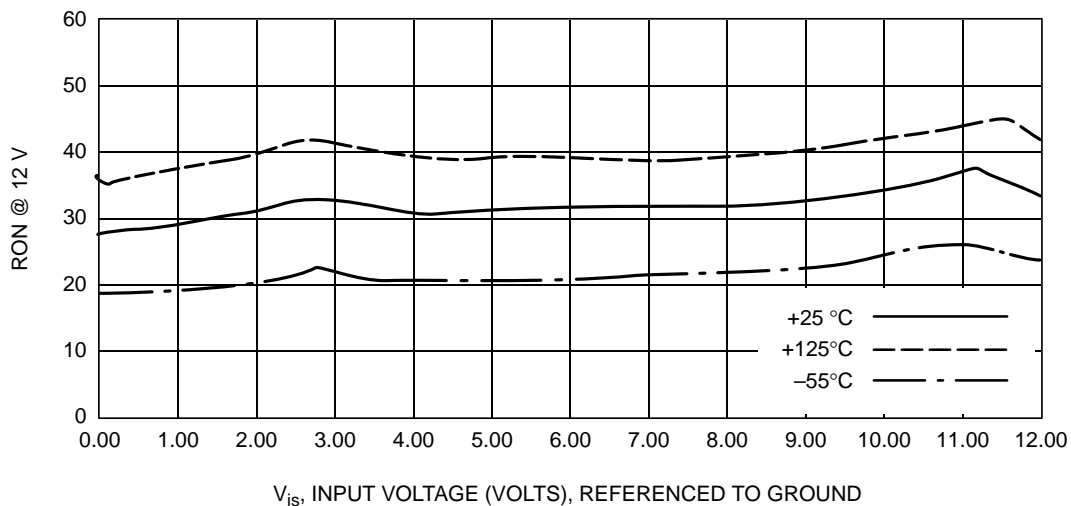


Figure 1f. Typical On Resistance, $V_{CC} = 12.0\text{ V}$

MC74HC4066A

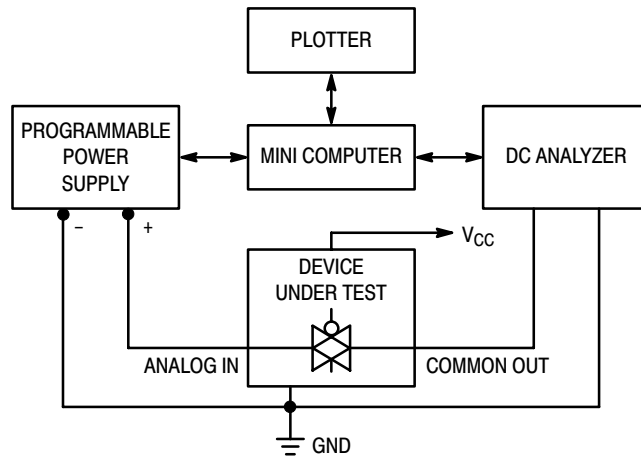


Figure 2. On Resistance Test Set-Up

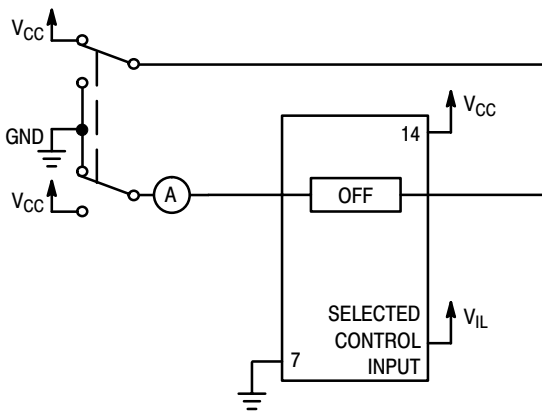


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

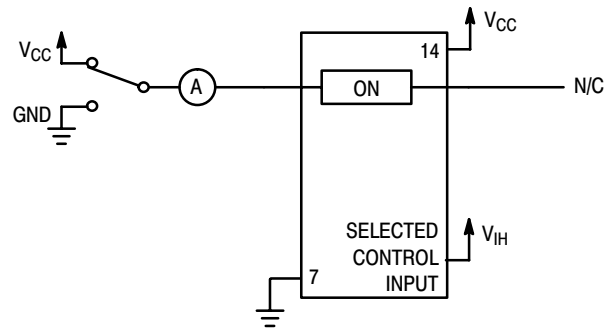
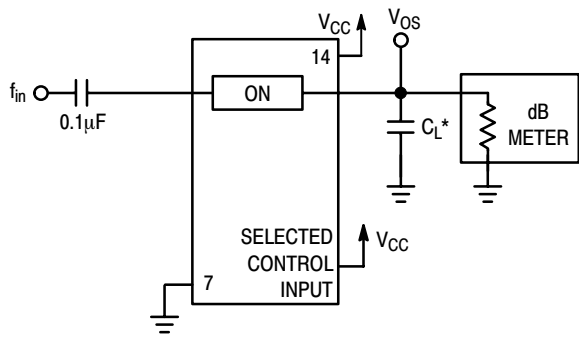
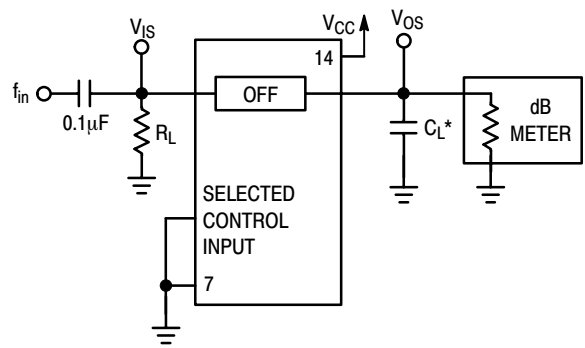


Figure 4. Maximum On Channel Leakage Current, Test Set-Up



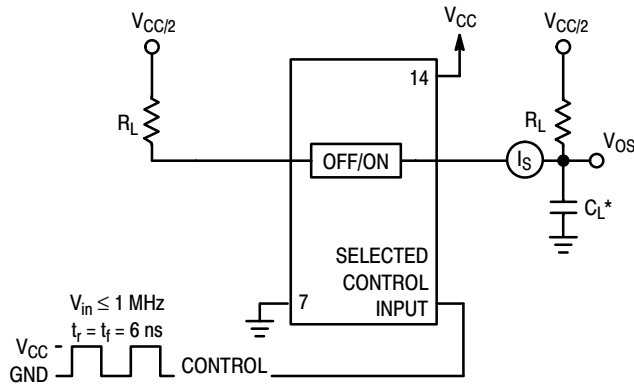
*Includes all probe and jig capacitance.

Figure 5. Maximum On-Channel Bandwidth Test Set-Up



*Includes all probe and jig capacitance.

Figure 6. Off-Channel Feedthrough Isolation, Test Set-Up



*Includes all probe and jig capacitance.

Figure 7. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set-Up

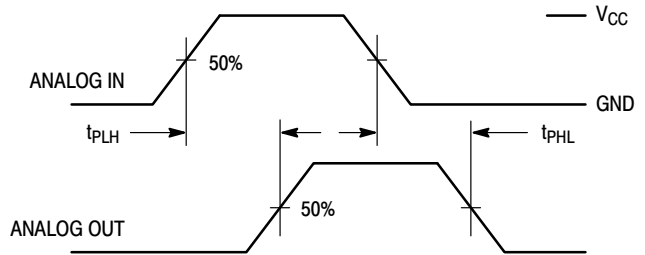
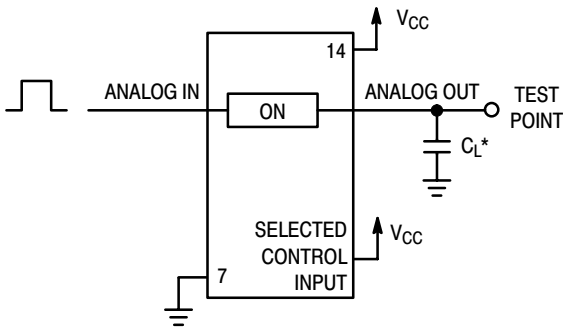


Figure 8. Propagation Delays, Analog In to Analog Out

MC74HC4066A



*Includes all probe and jig capacitance.

Figure 9. Propagation Delay Test Set-Up

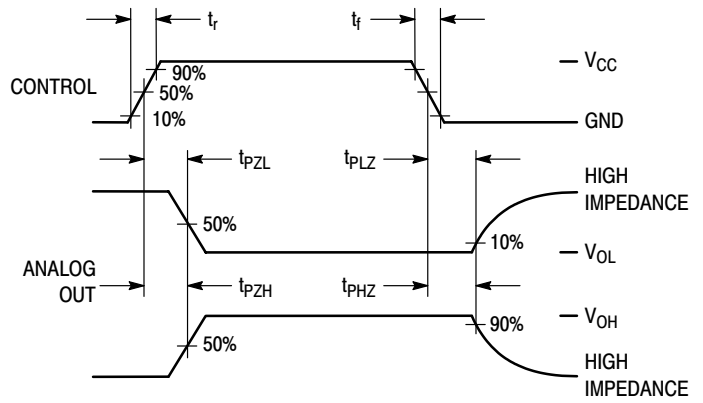
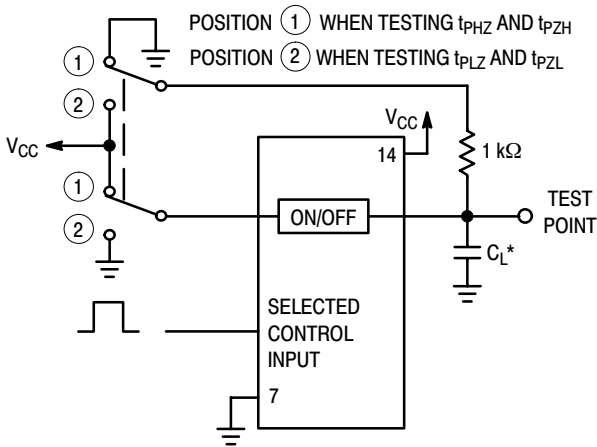
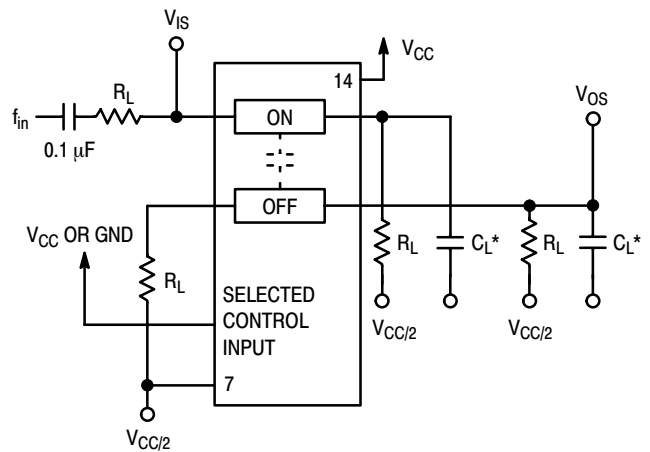


Figure 10. Propagation Delay, ON/OFF Control to Analog Out



*Includes all probe and jig capacitance.

Figure 11. Propagation Delay Test Set-Up



*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set-Up

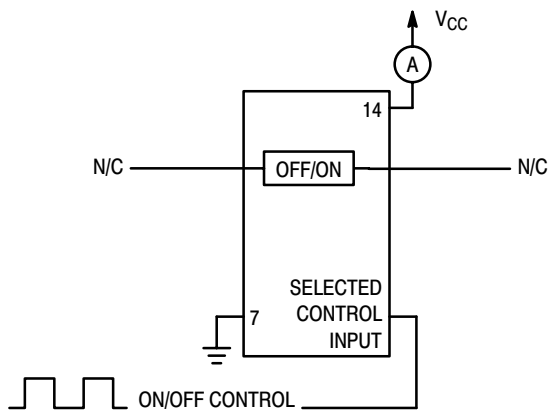
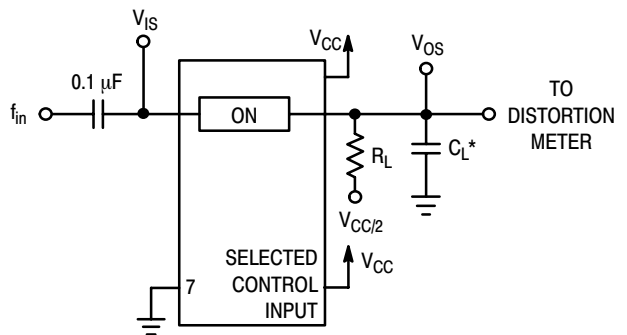


Figure 13. Power Dissipation Capacitance Test Set-Up



*Includes all probe and jig capacitance.

Figure 14. Total Harmonic Distortion, Test Set-Up

MC74HC4066A

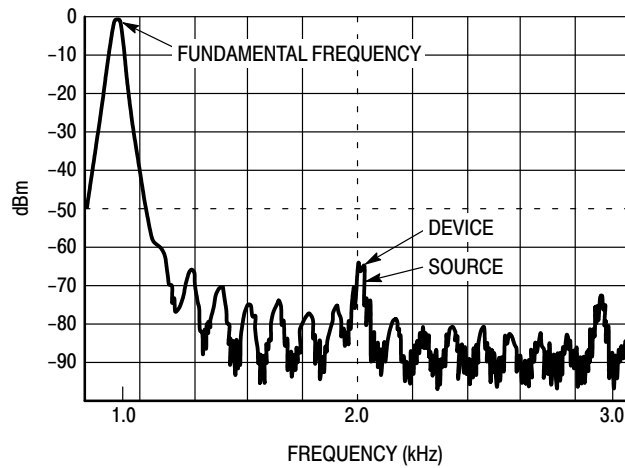


Figure 15. Plot, Harmonic Distortion

APPLICATION INFORMATION

The ON/OFF Control pins should be at V_{CC} or GND logic levels, V_{CC} being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to V_{CC} or GND through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked-up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages V_{CC} and GND. The positive peak analog voltage should not exceed V_{CC} . Similarly, the negative peak analog voltage should not go below GND. In the example

below, the difference between V_{CC} and GND is twelve volts. Therefore, using the configuration in Figure 16, a maximum analog signal of twelve volts peak-to-peak can be controlled.

When voltage transients above V_{CC} and/or below GND are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure 17. These diodes should be small signal, fast turn-on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the D_x diodes with Mosorbs (Mosorb™ is an acronym for high current surge protectors). Mosorbs are fast turn-on devices ideally suited for precise DC protection with no inherent wear out mechanism.

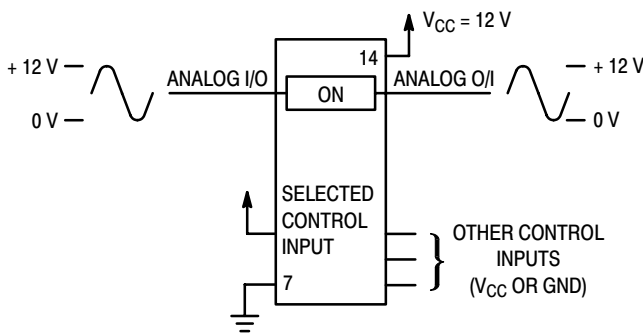


Figure 16. 12 V Application

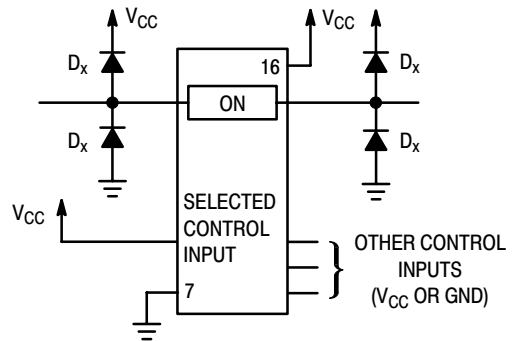


Figure 17. Transient Suppressor Application

MC74HC4066A

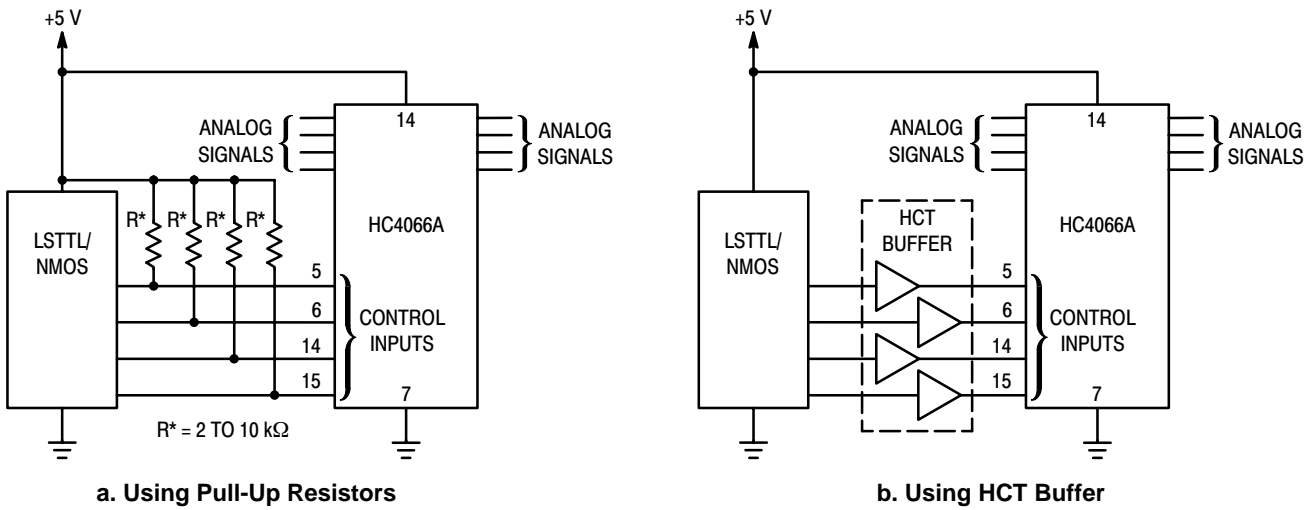


Figure 18. LSTTL/NMOS to HCMOS Interface

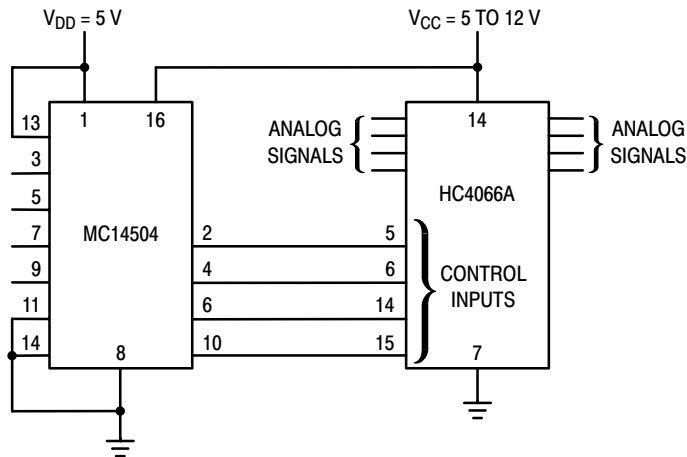


Figure 19. TTL/NMOS-to-CMOS Level Converter
Analog Signal Peak-to-Peak Greater than 5 V
(Also see HC4316A)

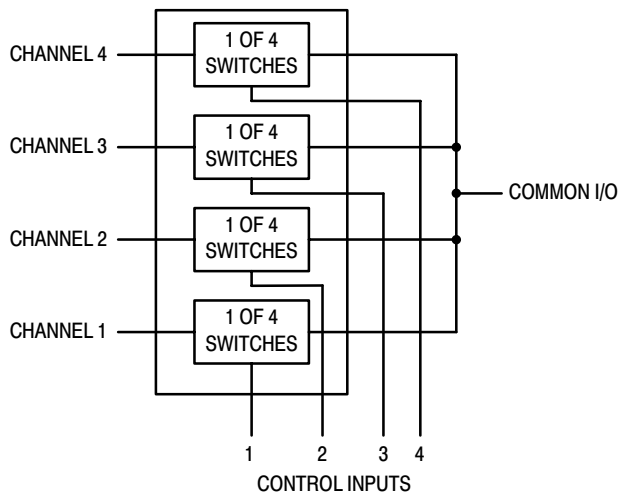


Figure 20. 4-Input Multiplexer

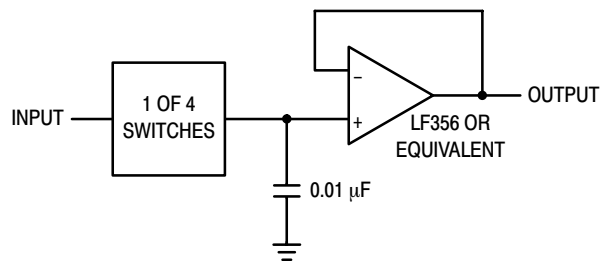
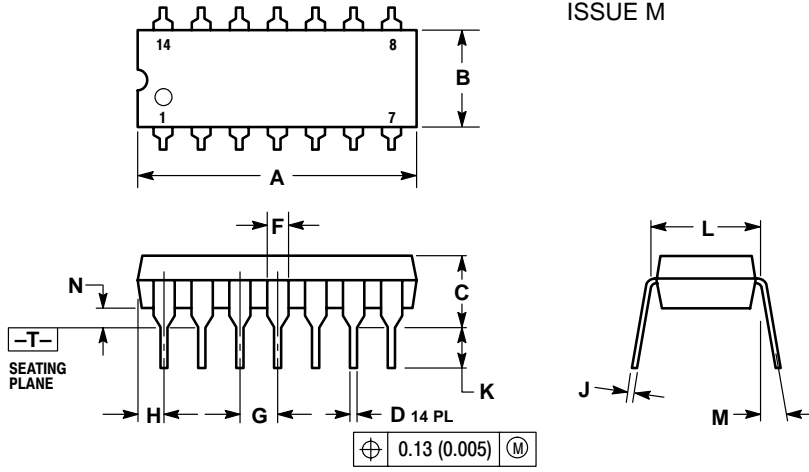


Figure 21. Sample/Hold Amplifier

MC74HC4066A

PACKAGE DIMENSIONS

PDIP-14
N SUFFIX
CASE 646-06
ISSUE M



NOTES:

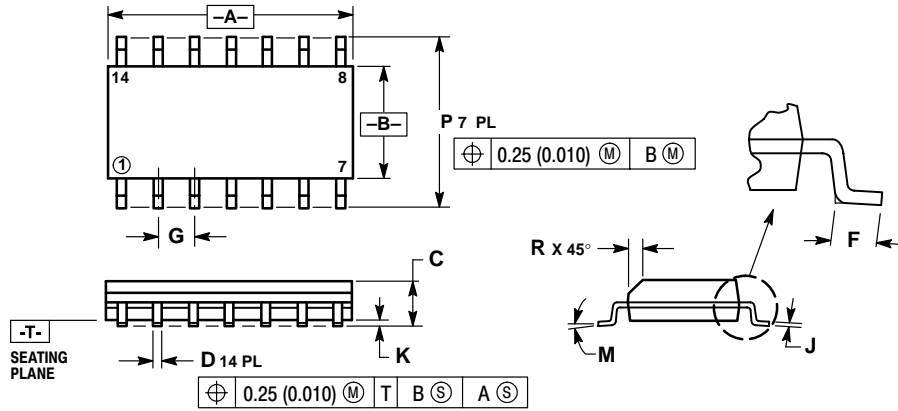
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.715 | 0.770 | 18.16 | 18.80 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.145 | 0.185 | 3.69 | 4.69 |
| D | 0.015 | 0.021 | 0.38 | 0.53 |
| F | 0.040 | 0.070 | 1.02 | 1.78 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.052 | 0.095 | 1.32 | 2.41 |
| J | 0.008 | 0.015 | 0.20 | 0.38 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.290 | 0.310 | 7.37 | 7.87 |
| M | --- | 10° | --- | 10° |
| N | 0.015 | 0.039 | 0.38 | 1.01 |

MC74HC4066A

PACKAGE DIMENSIONS

SOIC-14
D SUFFIX
CASE 751A-03
ISSUE F



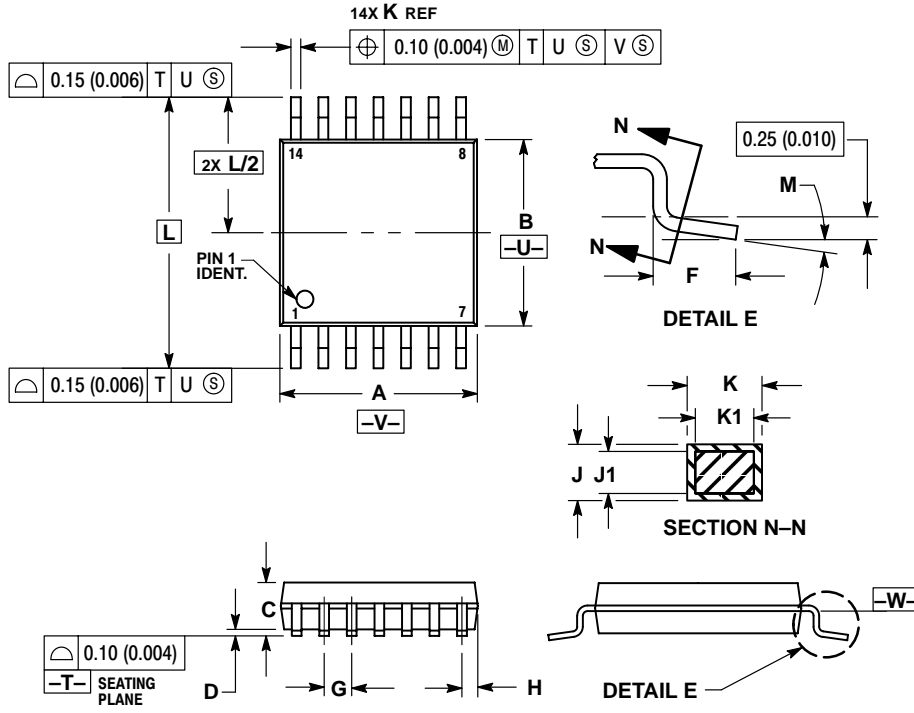
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.228 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

MC74HC4066A

PACKAGE DIMENSIONS

TSSOP-14
DT SUFFIX
CASE 948G-01
ISSUE O



NOTES:

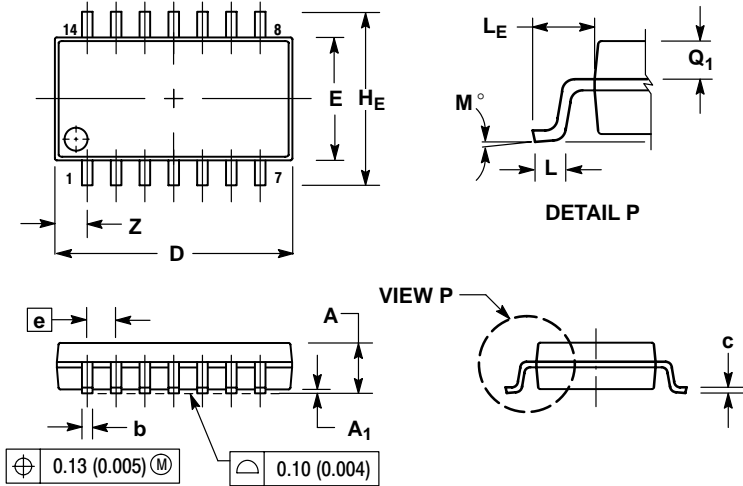
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

MC74HC4066A

PACKAGE DIMENSIONS


SO EIAJ-14
F SUFFIX
CASE 965-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| A ₁ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.18 | 0.27 | 0.007 | 0.011 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| H _E | 7.40 | 8.20 | 0.291 | 0.323 |
| 0.50 | 0.50 | 0.85 | 0.020 | 0.033 |
| L _E | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0° | 10° | 0° | 10° |
| Q ₁ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 1.42 | --- | 0.056 |

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