

BLF7G20L-90P; BLF7G20LS-90P

Power LDMOS transistor

Rev. 3 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

90 W LDMOS power transistor for base station applications at frequencies from 1800 MHz to 2000 MHz, designed for operation at 1427 MHz to 1525 MHz, 1805 MHz to 1880 MHz and 2110 MHz to 2170 MHz.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25\text{ °C}$ in a common source class-AB production test circuit.

Mode of operation	f (MHz)	I_{Dq} (mA)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR _{400k} (dBc)	ACPR _{600k} (dBc)	EVM _{rms} (%)
CW	1805 to 1880	550	28	84	19	54	-	-	-
GSM EDGE	1805 to 1880	550	28	40	19.5	41	-61	-74	2.5

1.2 Features and benefits

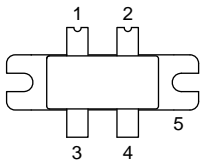
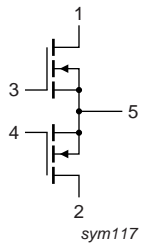

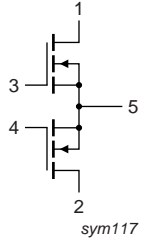
- Excellent ruggedness
- High efficiency
- Low R_{th} providing excellent thermal stability
- Designed for broadband operation (1427 MHz to 1525 MHz, 1805 MHz to 1880 MHz and 2110 MHz to 2170 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the frequency bands of 1427 MHz to 1525 MHz, 1805 MHz to 1880 MHz and 2110 MHz to 2170 MHz.

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF7G20L-90P (SOT1121A)			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source		
BLF7G20LS-90P (SOT1121B)			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF7G20L-90P	-	flanged LDMOST ceramic package; 2 mounting holes; 4 leads	SOT1121A
BLF7G20LS-90P	-	earless flanged LDMOST ceramic package; 4 leads	SOT1121B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
I_D	drain current		-	18	A
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_L = 90\text{ W}$	0.49	K/W

6. Characteristics

Table 6. Characteristics

$T_j = 25\text{ °C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.5\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 50\text{ mA}$	1.5	1.9	2.3	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	2	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	8.2	9.5	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	200	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 2.5\text{ A}$	-	3.8	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 1.75\text{ A}$	-	0.28	-	Ω

7. Test information

Table 7. Application information

$f = 1805\text{ MHz}$ to 1880 MHz ; RF performance at $V_{DS} = 28\text{ V}; I_{Dq} = 550\text{ mA}; T_{case} = 25\text{ °C}$; 2 sections combined unless otherwise specified; in a class-AB production test circuit.

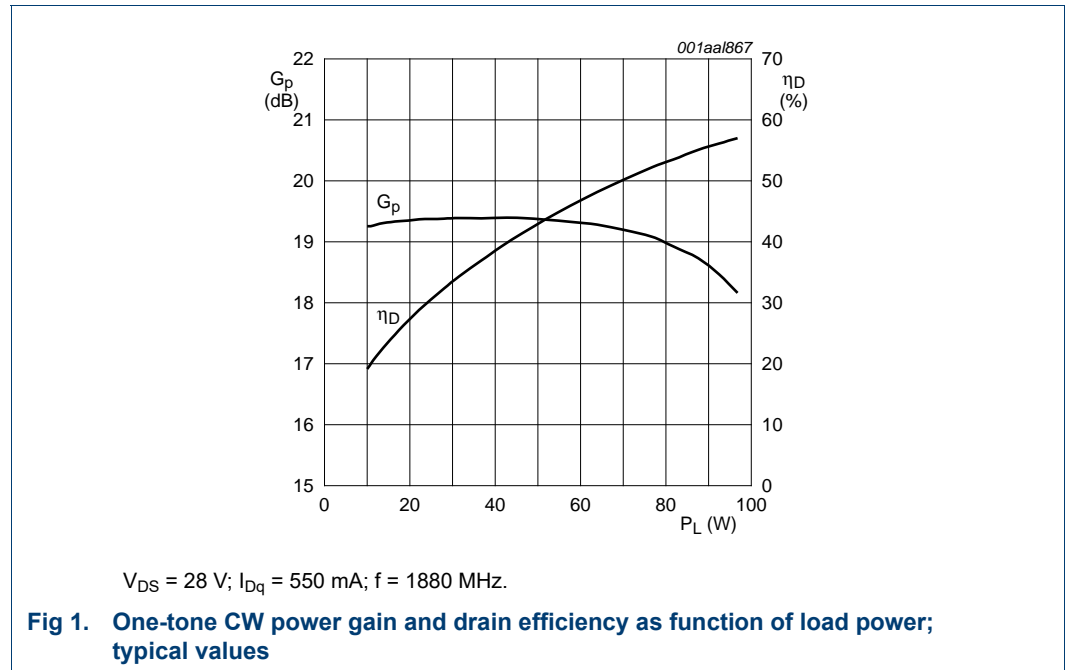
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Mode of operation: GSM EDGE; $P_{L(AV)} = 40\text{ W}$						
G_p	power gain		18.3	19.5	-	dB
RL_{in}	input return loss		-	-15	-8	dB
η_D	drain efficiency		38	41	-	%
$ACPR_{400k}$	adjacent channel power ratio (400 kHz)		-	-61	-58	dBc
$ACPR_{600k}$	adjacent channel power ratio (600 kHz)		-	-74	-70.5	dBc
EVM_{rms}	RMS EDGE signal distortion error		-	2.5	3.8	%
EVM_M	peak EDGE signal distortion error		-	8	12.5	%
Mode of operation: CW; $P_{L(AV)} = 84\text{ W}$						
G_p	power gain		17.8	19	-	dB
η_D	drain efficiency		51	54	-	%

7.1 Ruggedness in class-AB operation

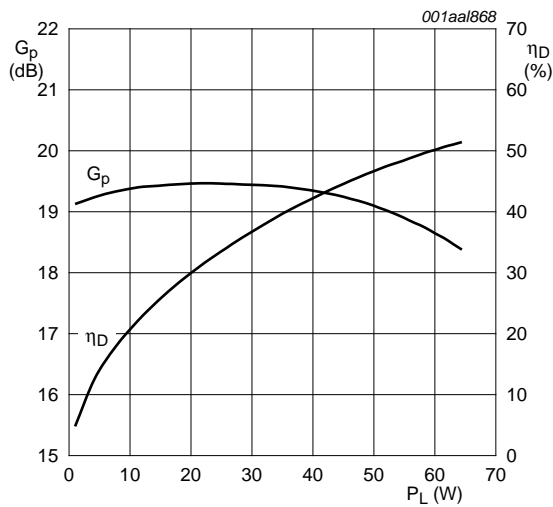
The BLF7G20L-90P and BLF7G20LS-90P are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:

- $V_{DS} = 28\text{ V}; I_{Dq} = 550\text{ mA}; P_L = 90\text{ W (CW)}, f = 1805\text{ MHz},$
- $V_{DS} = 28\text{ V}; I_{Dq} = 380\text{ mA}; P_L = 40\text{ W (CW, half device)}, f = 2110\text{ MHz},$
- $V_{DS} = 28\text{ V}; I_{Dq} = 380\text{ mA}; P_L = 55\text{ W (CW pulse, 10\%, 100 }\mu\text{s, halve device)},$
 $f = 1427\text{ MHz}.$

7.2 One-tone CW

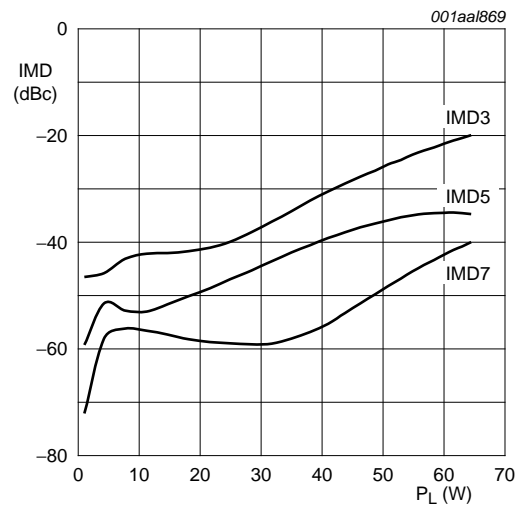


7.3 Two-tone CW



$V_{DS} = 28\text{ V}; I_{DQ} = 550\text{ mA}; f_1 = 1879.95\text{ MHz}; f_2 = 1880.05\text{ MHz}.$

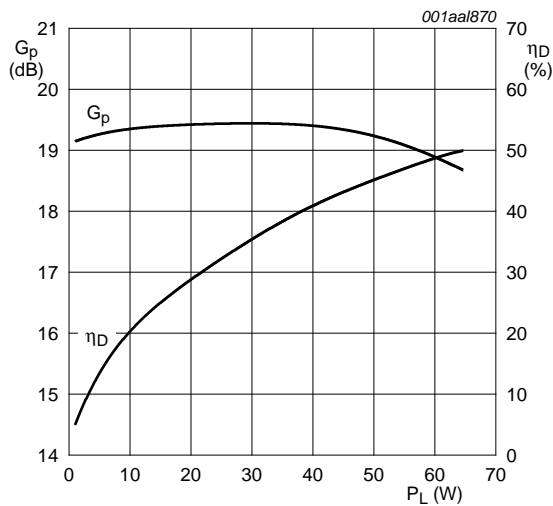
Fig 2. Two-tone CW power gain and drain efficiency as function of load power; typical values



$V_{DS} = 28\text{ V}; I_{DQ} = 550\text{ mA}; f_1 = 1879.95\text{ MHz}; f_2 = 1880.05\text{ MHz}.$

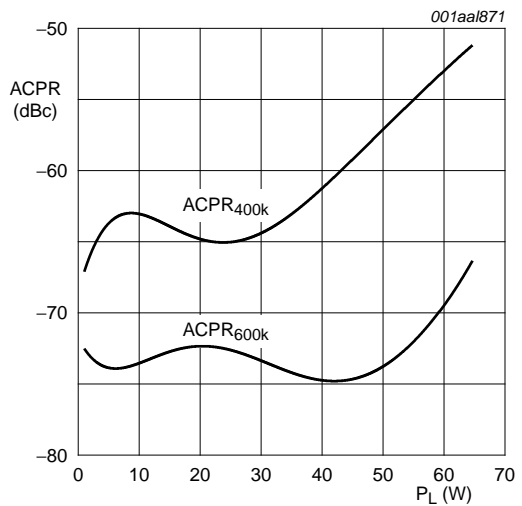
Fig 3. Two-tone CW intermodulation distortion as a function of load power; typical values

7.4 GSM EDGE



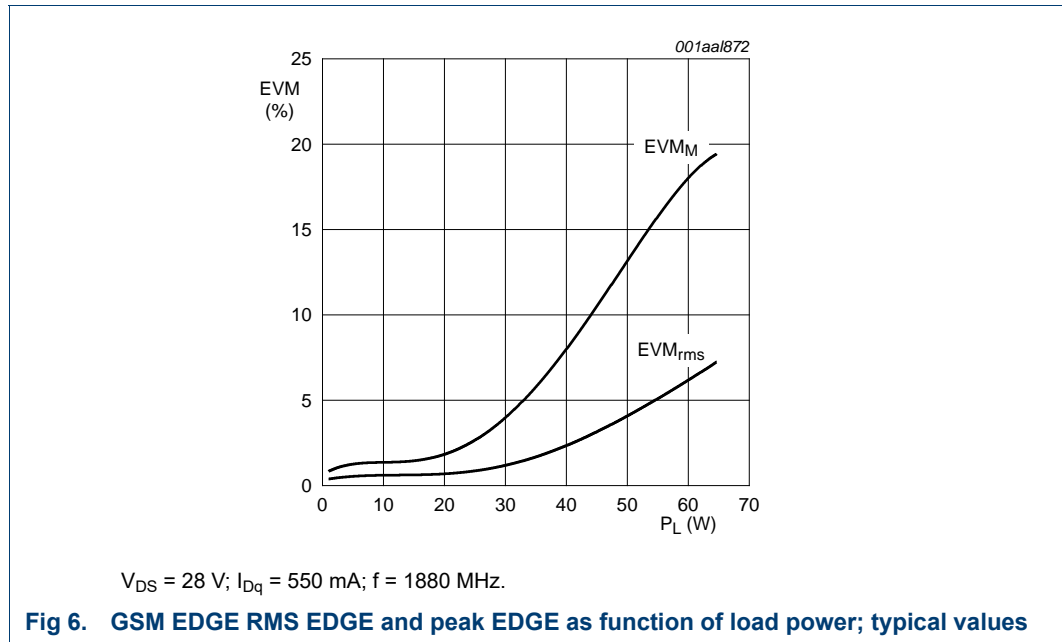
$V_{DS} = 28\text{ V}; I_{DQ} = 550\text{ mA}; f = 1880\text{ MHz}.$

Fig 4. GSM EDGE power gain and drain efficiency as function of load power; typical values



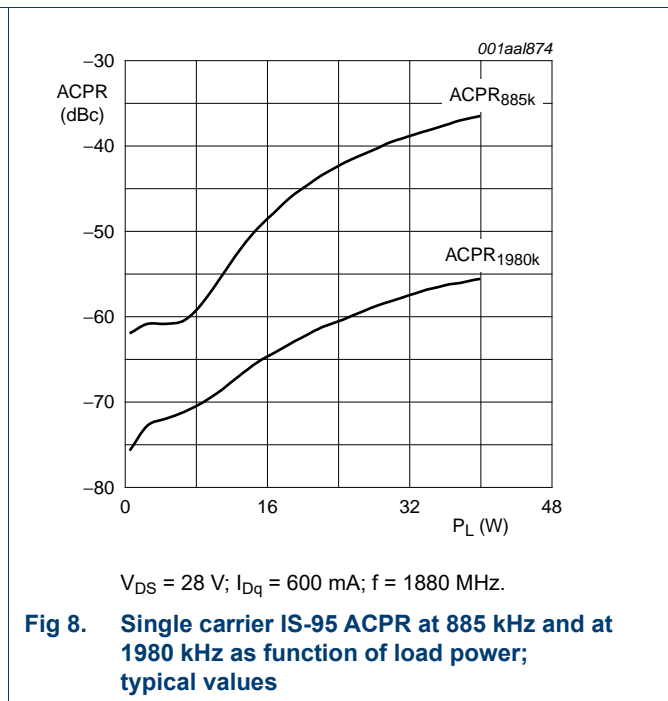
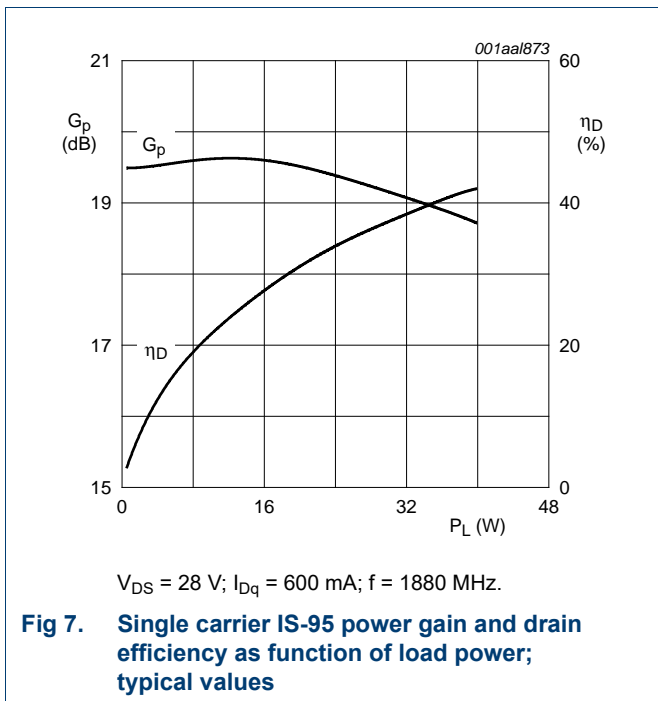
$V_{DS} = 28\text{ V}; I_{DQ} = 550\text{ mA}; f = 1880\text{ MHz}.$

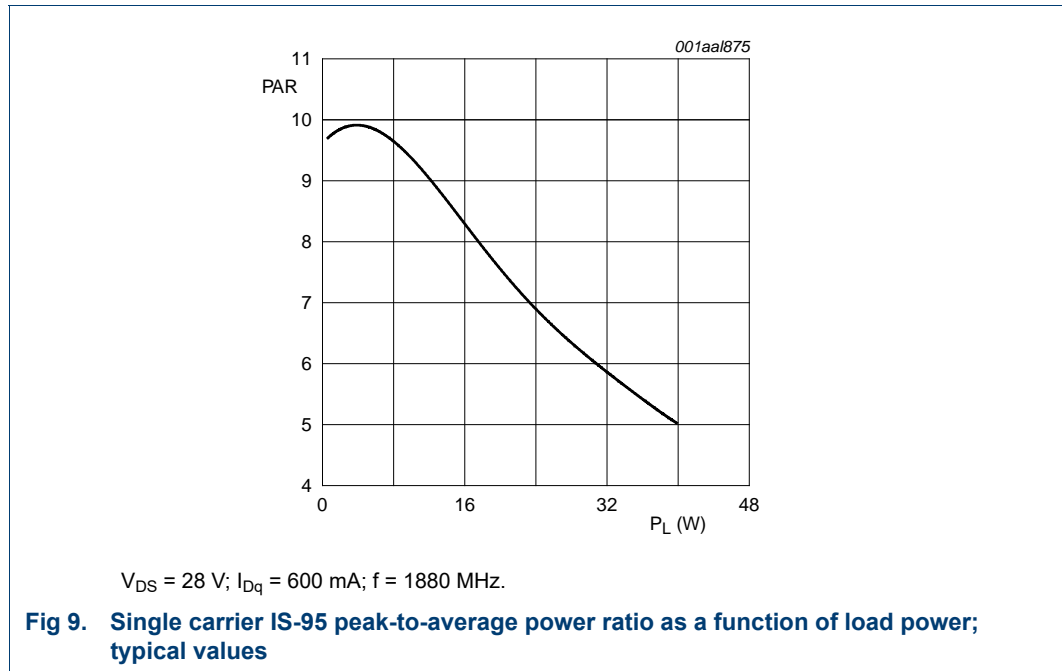
Fig 5. GSM EDGE ACPR at 400 kHz and at 600 kHz as function of load power; typical values



7.5 Single carrier IS-95

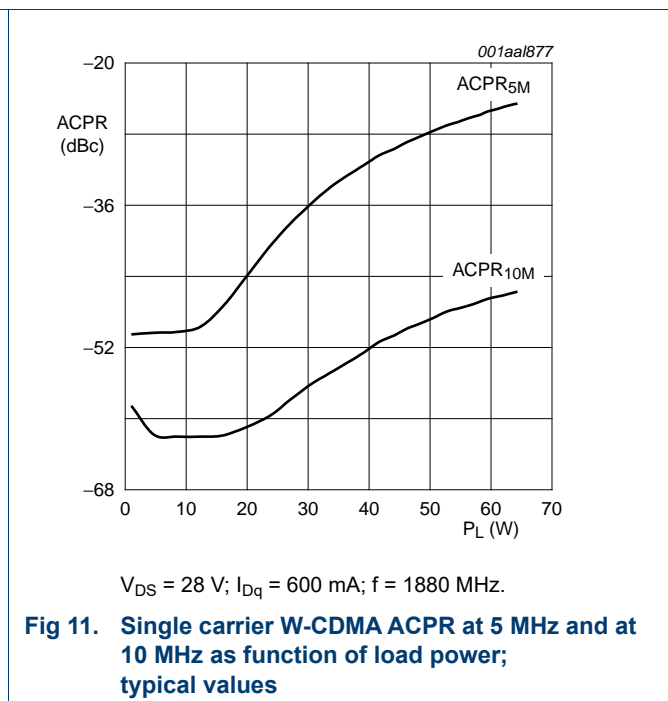
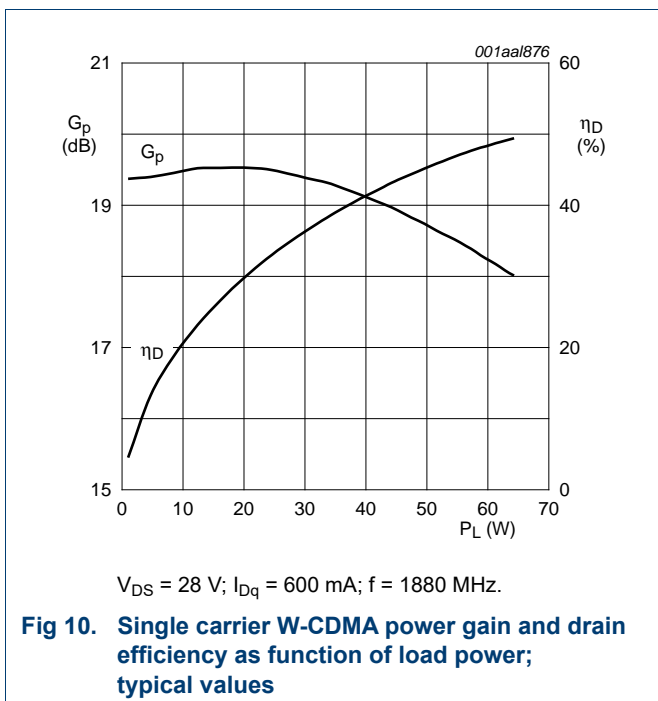
Single carrier IS-95 with pilot, paging, sync and 6 traffic channels (Walsh codes 8 - 13). PAR = 9.7 dB at 0.01 % probability on the CCDF. Channel bandwidth is 1.2288 MHz.





7.6 Single carrier W-CDMA

3GPP; test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.
Channel bandwidth is 3.84 MHz.



7.7 Test circuit

Table 8. List of components

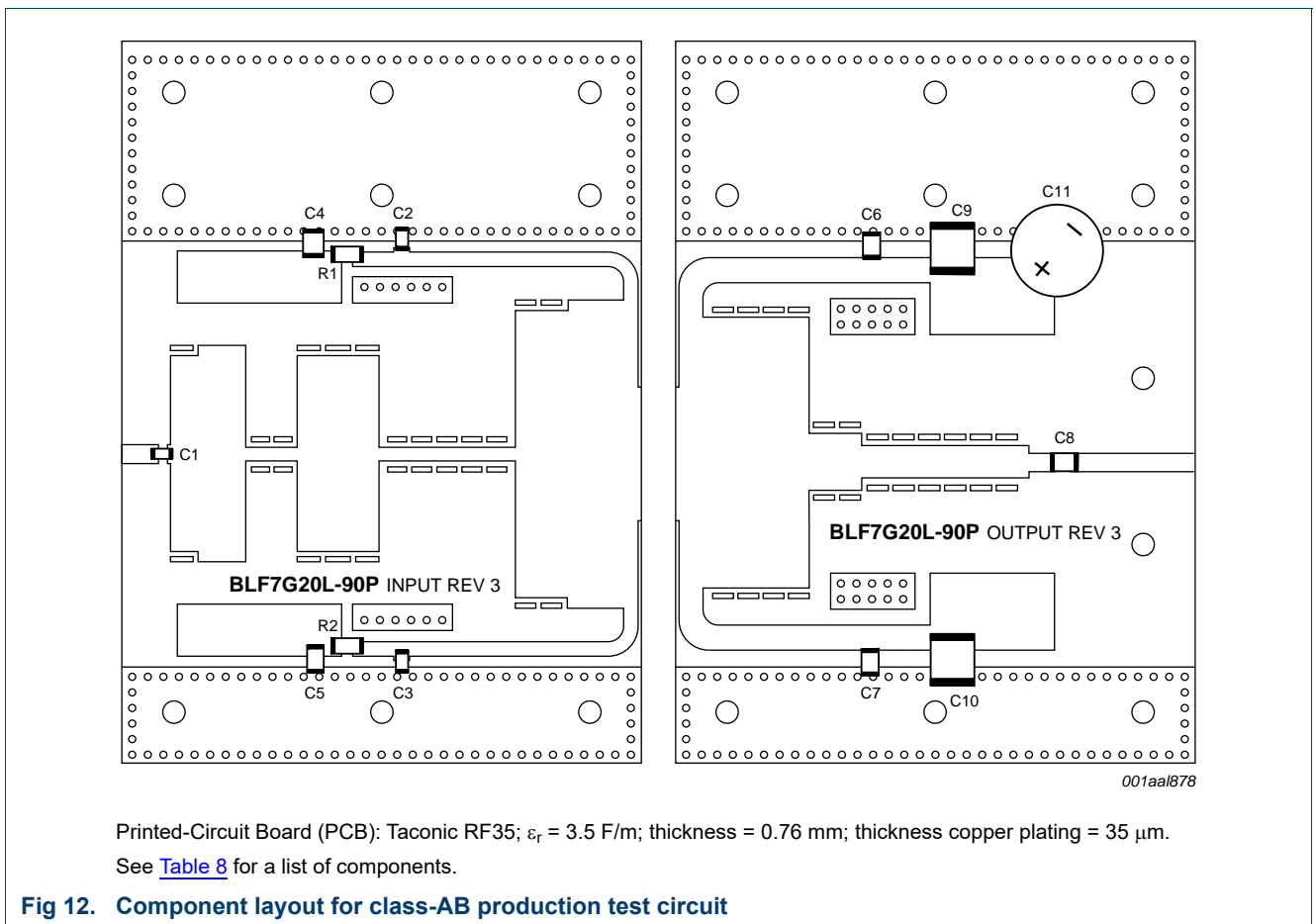
For test circuit see [Figure 12](#).

Component	Description	Value	Remarks
C1, C2, C3	multilayer ceramic chip capacitor	24 pF	[1]
C4, C5	multilayer ceramic chip capacitor	4.7 μ F	[2]
C6, C7, C8	multilayer ceramic chip capacitor	11 pF	[3]
C9, C10	multilayer ceramic chip capacitor	10 μ F	[2]
C11	electrolytic capacitor	470 μ F; 63 V	
R1, R2	SMD resistor	12 Ω	Philips 1206

[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] TDK or capacitor of same quality.

[3] American Technical Ceramics type 100B or capacitor of same quality.



7.8 Impedance information

Table 9. Typical impedance

Typical values valid for both section in parallel unless otherwise specified.

f MHz	Z _S Ω	Z _L Ω
1800	1.0 – j3.3	2.8 – j2.7
1840	1.2 – j3.3	2.8 – j2.5
1880	1.1 – j3.4	2.7 – j2.4

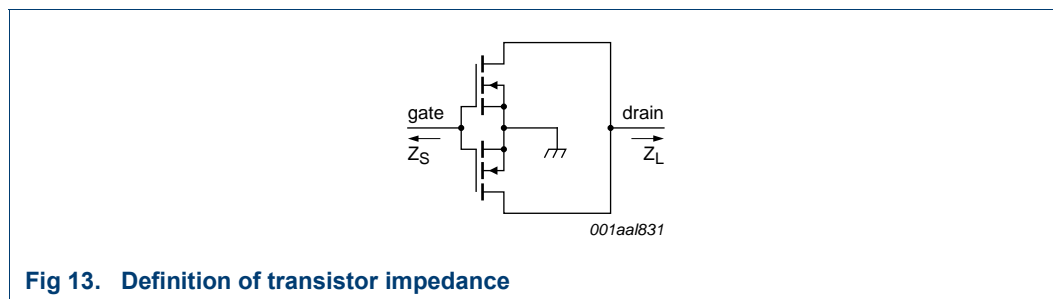
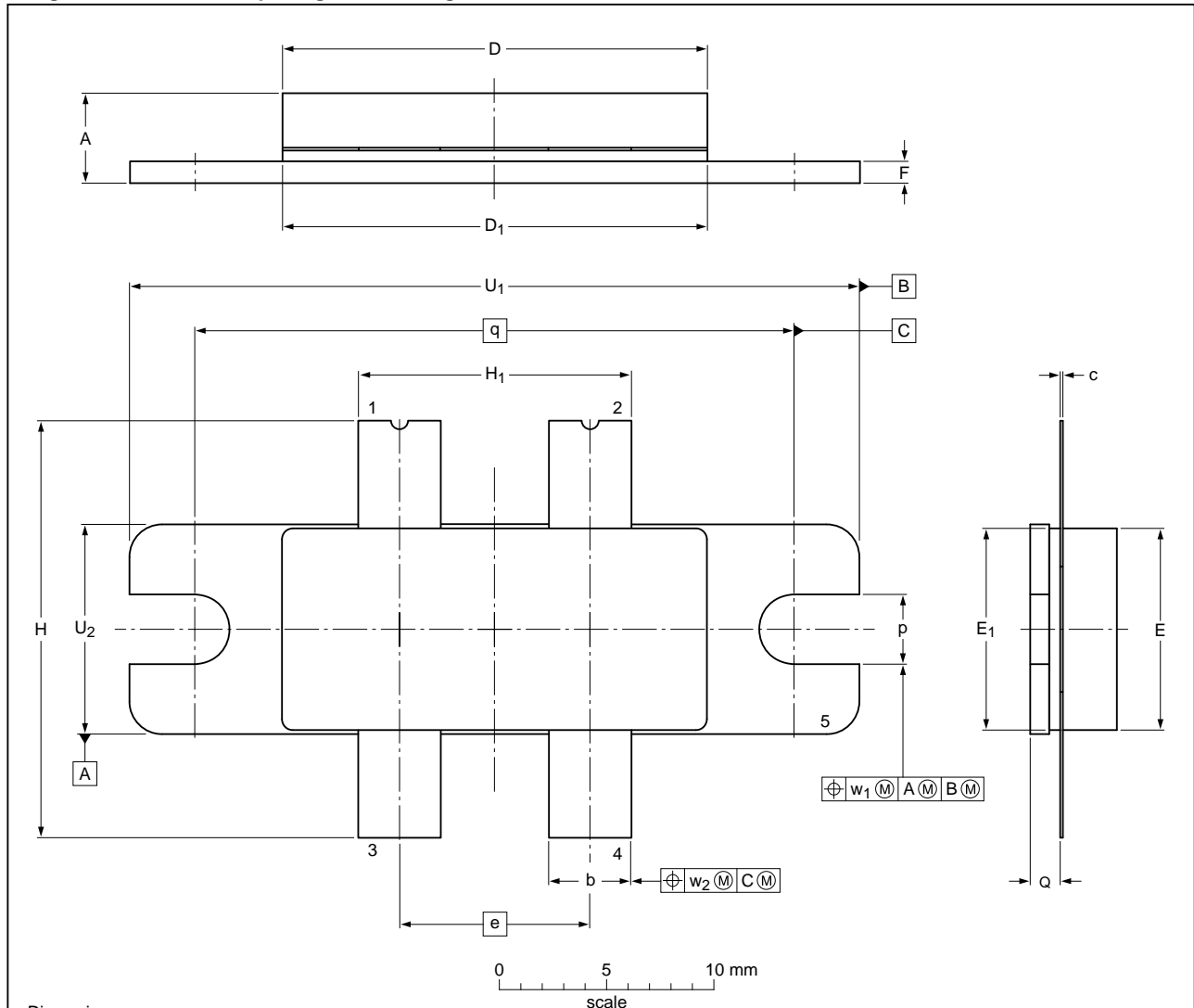


Fig 13. Definition of transistor impedance

8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 4 leads

SOT1121A



Dimensions

Unit ⁽¹⁾	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	p	Q ⁽²⁾	q	U ₁	U ₂	w ₁	w ₂
mm	max	4.75	3.94	0.18	20.02	19.96	9.53	9.53	1.14	19.94	12.83	3.38	1.70	34.16	9.91			
	nom					8.89							27.94				0.25	0.51
	min	3.45	3.68	0.10	19.61	19.66	9.27	9.27	0.89	18.92	12.57	3.12	1.45	33.91	9.65			
inches	max	0.187	0.155	0.007	0.788	0.786	0.375	0.375	0.045	0.785	0.505	0.133	0.067	1.345	0.39			
	nom					0.35							1.1				0.01	0.02
	min	0.136	0.145	0.004	0.772	0.774	0.365	0.365	0.035	0.745	0.495	0.123	0.057	1.335	0.38			

Note

- 1. millimeter dimensions are derived from the original inch dimensions.
- 2. dimension is measured 0.030 inch (0.76 mm) from the body.

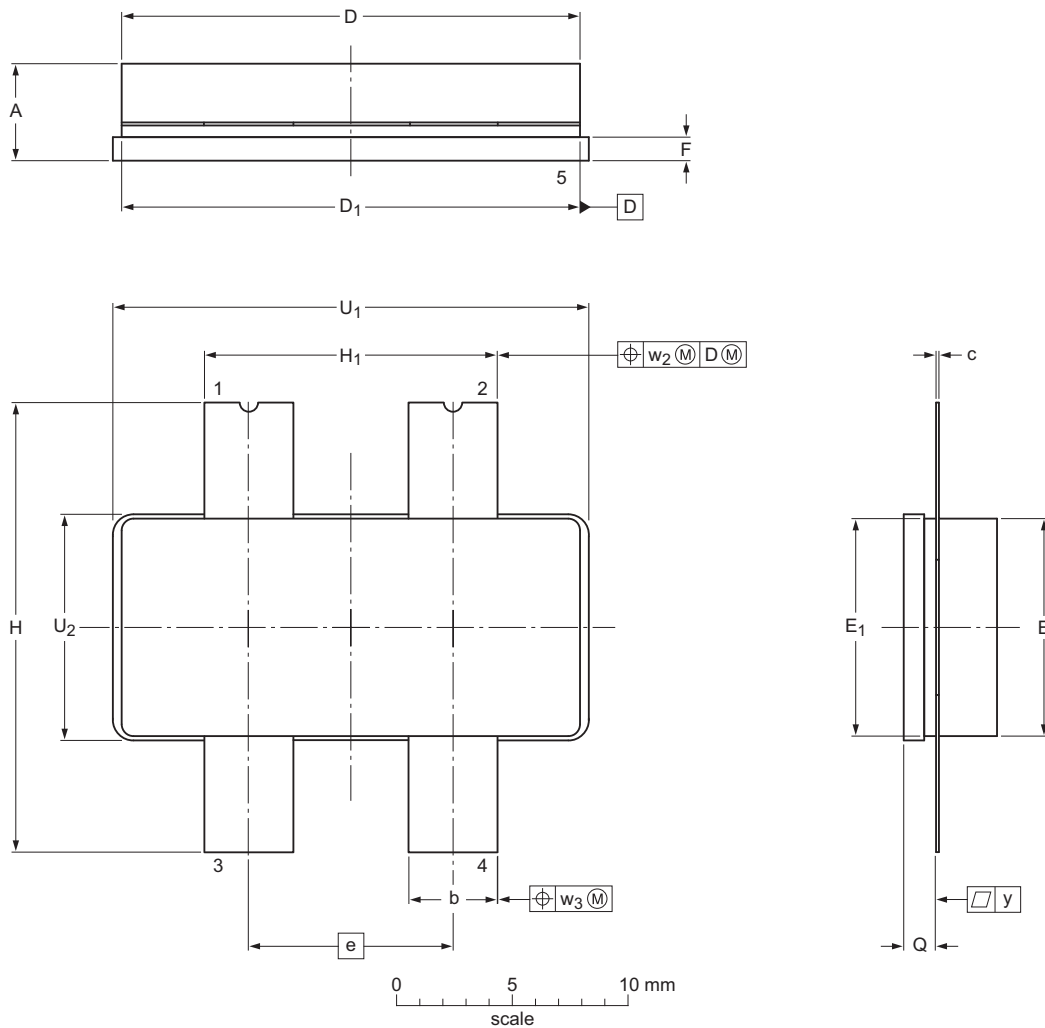
sot1121a_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1121A					09-10-12 10-02-02

Fig 14. Package outline SOT1121A

Earless flanged ceramic package; 4 leads

SOT1121B



Dimensions

Unit ⁽¹⁾	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	Q	U ₁	U ₂	w ₂	w ₃	y
mm	max	4.75	3.94	0.18	20.02	19.96	9.53	9.53	1.14	19.94	12.83	1.70	20.70	9.91	0.51	0.25	0.25
	nom					8.89	9.27	9.27	0.89	18.92	12.57	1.45	20.45	9.65			
inches	max	0.187	0.155	0.007	0.788	0.786	0.375	0.375	0.045	0.785	0.505	0.067	0.815	0.39	0.02	0.01	0.01
	nom					0.35	0.365	0.365	0.035	0.745	0.495	0.057	0.805	0.38			

Note

1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1121b_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1121B					09-12-14 12-06-07

Fig 15. Package outline SOT1121B

9. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CW	Continuous Wave
CCDF	Complementary Cumulative Distribution Function
DPCH	Dedicated Physical Channel
EDGE	Enhanced Data rates for GSM Evolution
ESD	ElectroStatic Discharge
GSM	Global System for Mobile Communications
IS-95	Interim Standard 95
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
RF	Radio Frequency
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

10. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF7G20L-90P_7G20LS-90P#3	20150901	Product data sheet	-	BLF7G20L-90P_7G20LS-90P v.2
Modifications:	<ul style="list-style-type: none"> The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. Legal texts have been adapted to the new company name where appropriate. 			
BLF7G20L-90P_7G20LS-90P v.2	20111020	Product data sheet	-	BLF7G20L-90P_7G20LS-90P v.1
BLF7G20L-90P_7G20LS-90P v.1	20100428	Product data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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