



20 Gbps Clocked COMPARATOR with RSECL OUTPUT STAGE

Typical Applications

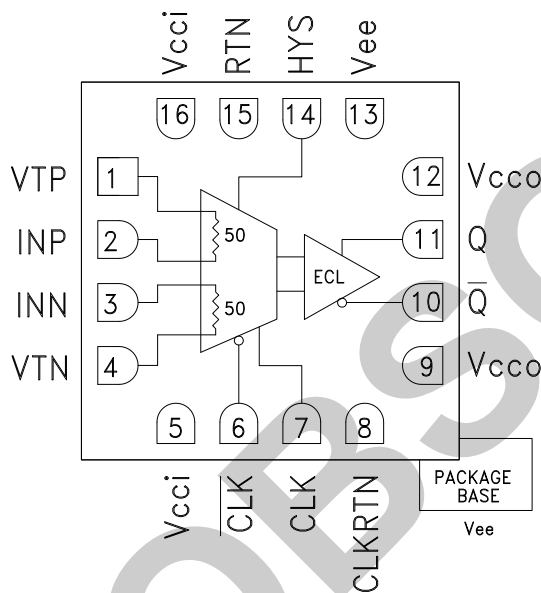
The HMC876LC3C is ideal for:

- ATE Applications
- High Speed Instrumentation
- Digital Receiver Systems
- Pulse Spectroscopy
- High Speed Trigger Circuits
- Clock & Data Restoration

Features

- Propagation Delay Clock to Output: 120 ps
- Overdrive & Slew Rate Dispersion: 10 ps
- Minimum Pulse Width: 60 ps
- Resistor Programmable Hysteresis
- Differential Clock Control
- Input Bandwidth: 10 GHz
- Power Dissipation: 150 mW
- RSCML and RSPECL Versions Available
- 16 Lead 3x3 mm SMT Package: 9 mm²

Functional Diagram



General Description

The HMC876LC3C is a SiGe monolithic, ultra fast comparator that features reduced swing ECL output drivers and clock inputs. The comparator supports 20 Gbps operation while providing 120 ps clock to data output delay and 60 ps minimum pulse width with 0.2 ps rms random jitter (RJ). 25 Gbps operation can be achieved with reduced output voltage swing. Overdrive and slew rate dispersion are typically 10 ps, making the device ideal for a wide range of applications from ATE to broadband communications. The reduced swing ECL output stage is designed to directly drive 400 mV into 50 ohms terminated to -2 V. The HMC876LC3C features high-speed latches with programmable hysteresis, and is configured to operate as a clocked comparator.

Electrical Specifications

$T_A = +25\text{ }^\circ\text{C}^{[1]}$, $V_{cc1} = +3.3\text{ V}$, $V_{cc0} = 0\text{ V}$, $\overline{CLK}/CLK = 1.6\text{ to }2.4\text{ V}$, $V_{ee} = -3\text{ V}$, $V_{TERM} = -2\text{ V}$

Parameter	Conditions	Min.	Typ.	Max	Units
Input Voltage Range	Maximum DC Input Current = 20 mA	-2		2	V
Input Differential Voltage		-1.75		1.75	V
Input Offset Voltage			±5		mV
Input Offset Voltage, Temperature Coefficient			15		µV / °C
Input Bias Current			15		µA
Input Bias Current Temperature Coefficient			50		nA / °C
Input Offset Current			4		µA
Input Impedance			50		Ω
Common Mode Input Impedance			350		KΩ
Differential Input Impedance			15		KΩ
Hysteresis	R _{hys} = ∞		±1		mV

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 Phone: 781-329-4700 • Order online at www.analog.com Application Support: Phone: 1-800-ANALOG-D



20 Gbps Clocked COMPARATOR with RSECL OUTPUT STAGE

Clock Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
Clock Input Impedance	Each Pin		50		Ω
Clock to Data Output Delay, tpd			120		ps
Clock Input Range		1.6	2.0	2.4	V
Clock Max Frequency, fmax			25		GHz

DC Output Characteristics, $V_{CC0} = 0\text{ V}$, $V_{TERM} = -2\text{ V}$

Parameter	Conditions	Min.	Typ.	Max	Units
Output Voltage High Level, Voh		-0.96		-0.89	V
Output Voltage Low Level, Vol		-1.30		-1.21	V
Output Voltage Differential Swing		320		340	mV

AC Performance

Parameter	Conditions	Min.	Typ.	Max	Units
VOD Dispersion	50mV < VOD < 1 V		10		ps
Tpd vs. Common Mode Dispersion, -1.75 V < Vcm < 1.75 V	VOD = 50 mV		8		ps
Equivalent Input Bandwidth ^[1]			11		GHz
Deterministic Jitter (pp)	Deterministic Jitter at 10 Gbps with $\pm 100\text{ mV}$ Overdrive		< 3		ps
Random Jitter (rms)	Random Jitter at 10 Gbps with $\pm 100\text{ mV}$ Overdrive		0.2		ps rms
Minimum Pulse Width			60		ps
Q / \bar{Q} Rise Time	From 20% to 80%		30		ps
Q / \bar{Q} Fall Time	From 20% to 80%		21		ps

Power Supply Requirements

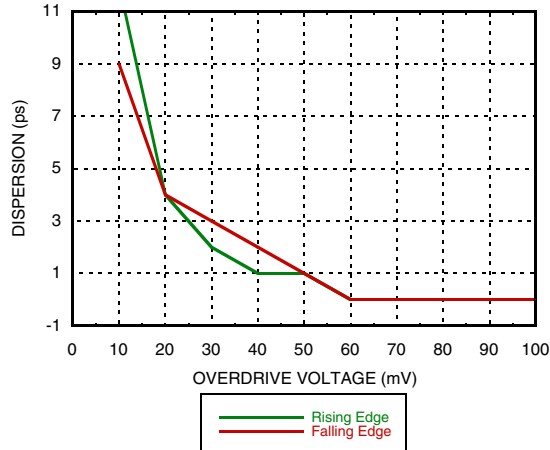
Parameter	Conditions	Min.	Typ.	Max	Units
Input Supply Current, IccI			13		mA
Output Supply Current, Icco			44		mA
Vee Current, Iee			20		mA
Power Dissipation, Pd			152		mW
PSRR, Vcci			38		dB
PSRR, Vee			38		dB

Note 1: Equivalent Input Bandwidth is calculated with the following formula: $B_{weq} = 0.22 / J$ (TRCOMP² - TRIN²) where TRIN is the 20%/80% transition time of a quasi-Gaussian signal applied to the comparator input, and TRCOMP is the effective transition time digitized by the comparator.

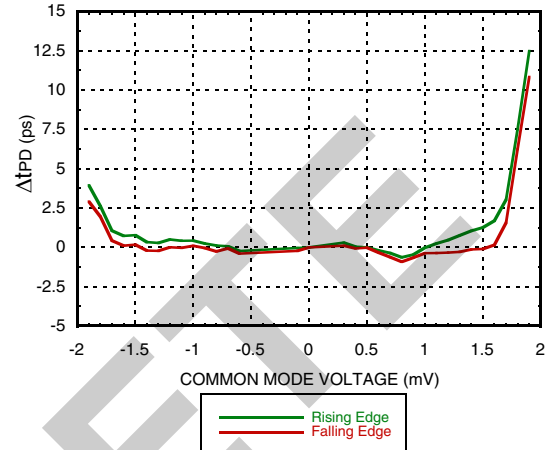


20 Gbps Clocked COMPARATOR with RSECL OUTPUT STAGE

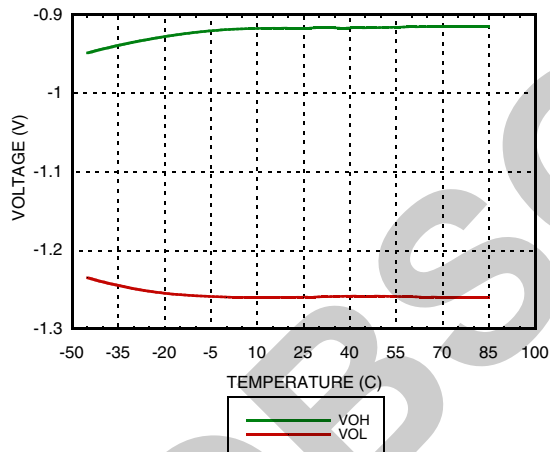
Dispersion vs. Overdrive Voltage



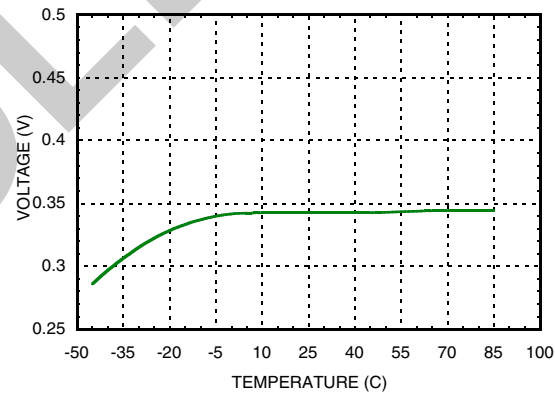
Propagation Delay vs. Input Common Mode Voltage^[1]



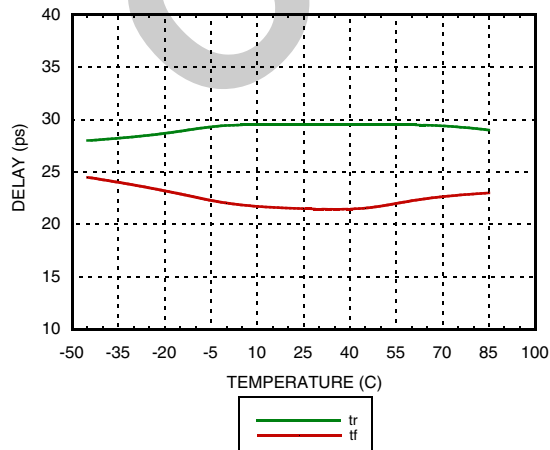
Output Voltage vs. Temperature



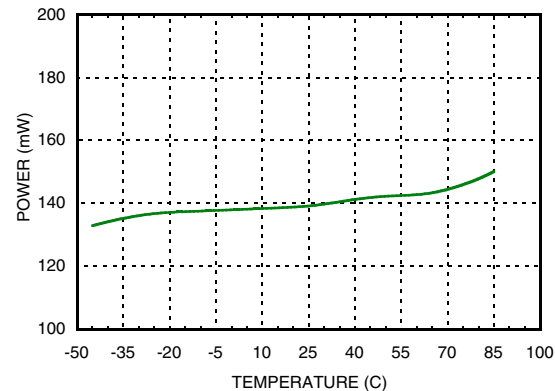
Voltage Swing vs. Temperature



Delay vs. Temperature



Power Dissipation vs. Temperature



[1] $V_{CCI} = +3.3\text{ V}$, $V_{CC0} = 0\text{ V}$, $V_{EE} = -3\text{ V}$, $V_{TERM} = -2\text{ V}$

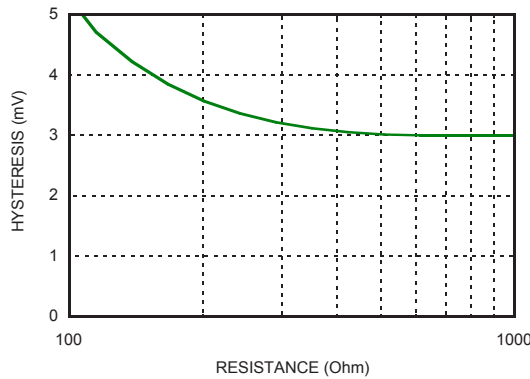
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 Phone: 781-329-4700 • Order online at www.analog.com Application Support: Phone: 1-800-ANALOG-D

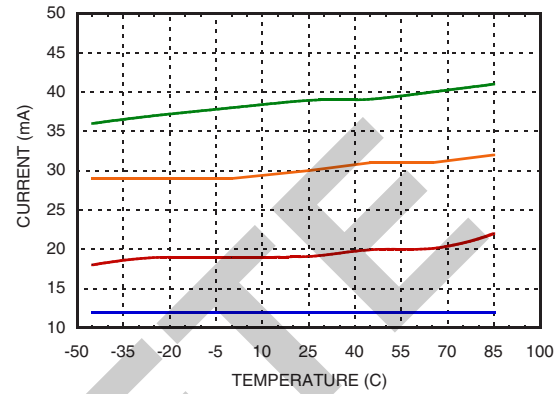


20 Gbps Clocked COMPARATOR with RSECL OUTPUT STAGE

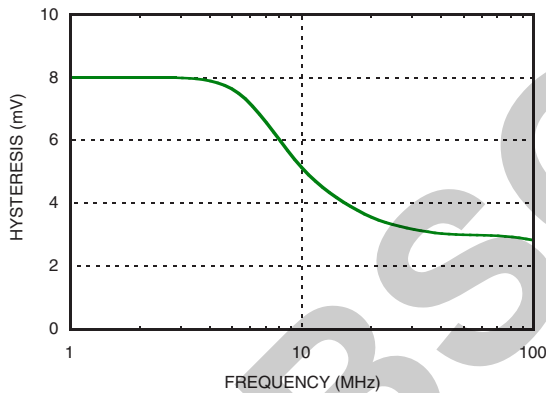
Comparator Hysteresis vs. Rhys Control Resistor



Currents vs. Temperature



Comparator Hysteresis vs. Clock Frequency (Rhys = ∞)



Eye Diagram



TJ(1E-12):	6.71 ps	DJ(6-5):	3.08 ps	RJ(rms):	265 fs
RJ(6-5):	310 fs	DDJ(p-p):	3.24 ps	DCD:	-----
PJ(rms)	0.0 s			ISI J(p-p)	3.24 ps

Absolute Maximum Ratings

Input Supply Voltage (Vcc1 to GND)	-0.5 V to +4 V
Output Supply Voltage (Vcco to GND)	-0.5 V to +4 V
Positive Supply Differential (Vcc1 - Vcco)	-0.5 V to +3.5 V
Input Voltage	-2 V to +2 V
Differential Input Voltage	-2 V to +2 V
Input Voltage, Clock	-0.5 V to Vcc1 +0.5 V
Applied Voltage (HYS)	Vee to GND
Maximum Input Current	±20 mA
Output Current	40 mA
Junction Temperature	125 °C
Continuous Pdiss (T = 85°C) (Derate 20.4 mW/°C above 85°C)	0.816 W
Thermal Resistance (Rth) (Junction to Lead)	49 °C/W
Storage Temperature	-65 °C to +150 °C
Operating Temperature	-40 °C to +85 °C
ESD Sensitivity (HBM)	Class 1A

Bit Rate	5.00000 Gb/s
Pat Length	127 Bits
Div. Ratio	1:8



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

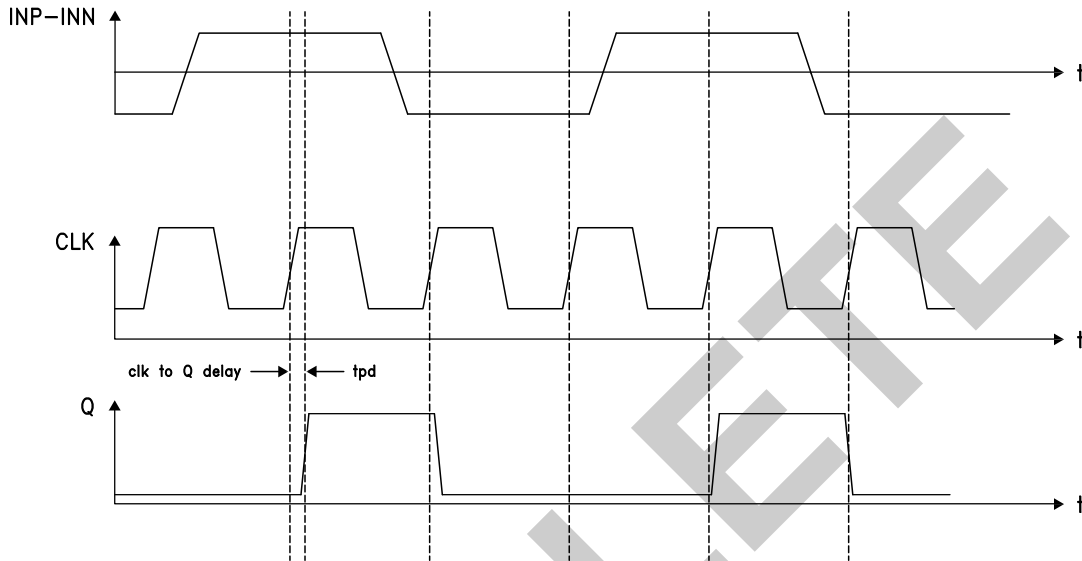
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D



**20 Gbps Clocked COMPARATOR
with RSECL OUTPUT STAGE**

Timing Diagram

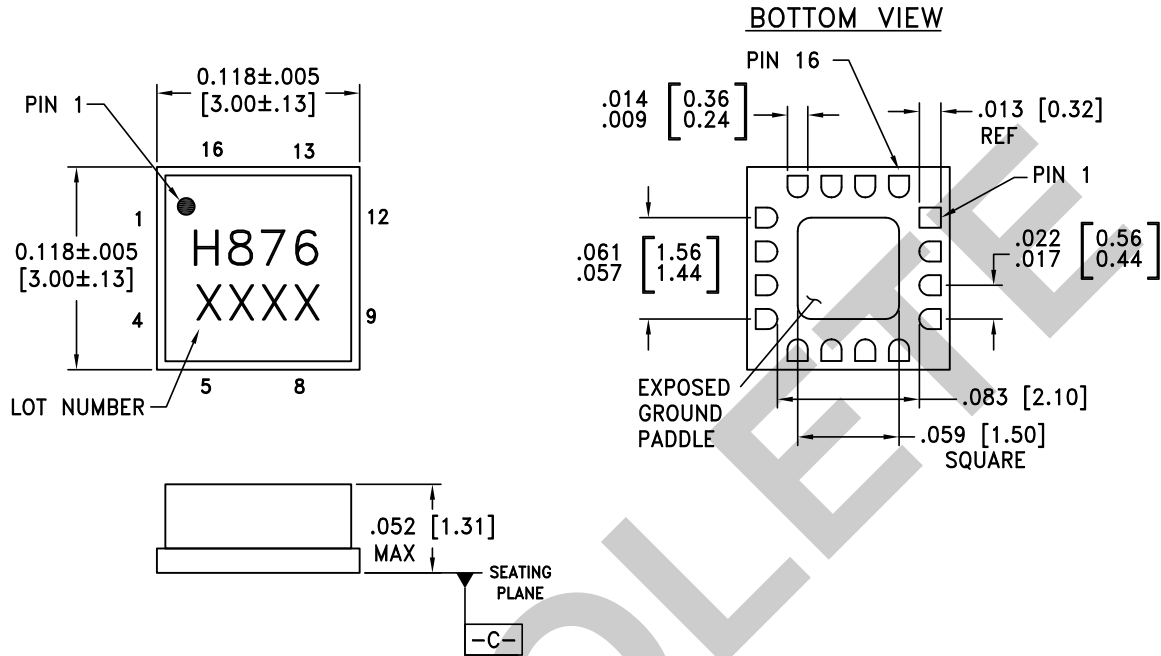


OBSOLETE

20 Gbps Clocked COMPARATOR with RSECL OUTPUT STAGE



Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST NOT BE DC GND. THERMAL DISSIPATION PATH ONLY.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking ^[2]
HMC876LC3C	Alumina, White	Gold over Nickel	MSL3 ^[1]	H876 XXXX

[1] Max peak reflow temperature of 260 °C

[2] 4-Digit lot number XXXX

20 Gbps Clocked COMPARATOR with RSECL OUTPUT STAGE



Pin Descriptions

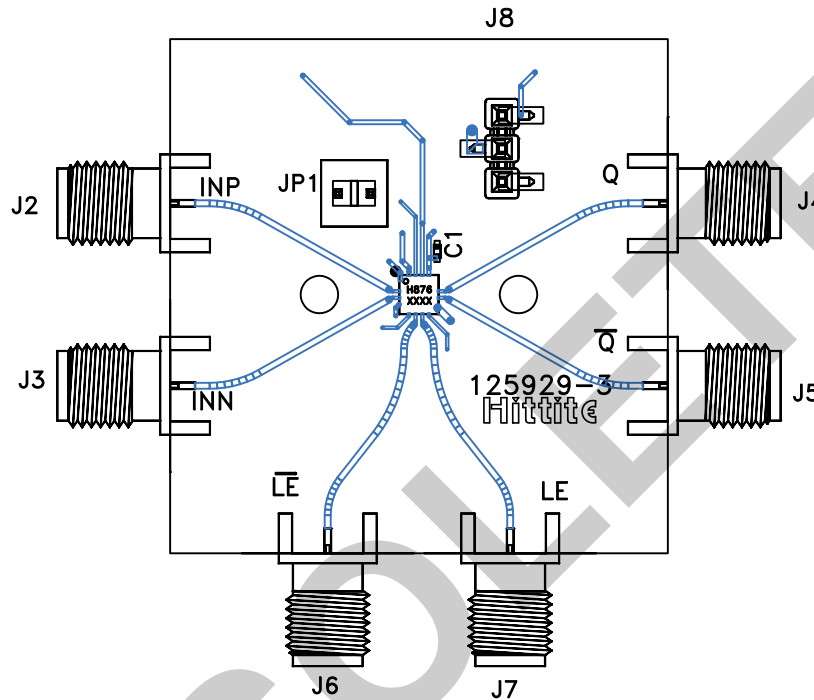
Pin Number	Function	Description	Interface Schematic
1	VTP	Termination resistor return pin for INP Input.	
2	INP	Non-Inverting analog input	
3	INN	Inverting analog input	
4	VTN	Termination resistor return pin for INN input	
5, 16	Vcci	Positive supply voltage input stage.	
6	$\overline{\text{CLK}}$	Clock input pin, inverting side.	
7	CLK	Clock input pin, non-inverting side.	
8	CLKRTN	Clock RTN pin, connect to GND.	
9, 12	Vcco	Positive supply voltage for the output stage.	
10	$\overline{\text{Q}}$	Inverting output. Q bar is at logic low if the analog voltage at the non-inverting input, INP, is greater than the analog voltage at the inverting input, INN, after a positive transition on CLK and negative transition on $\overline{\text{CLK}}$.	
11	Q	Non-inverting output. Q is at logic high if the analog voltage at the non-inverting input, INP, is greater than the analog voltage at the inverting input, INN, after a positive transition on CLK and negative transition on $\overline{\text{CLK}}$.	
14	HYS	Hysteresis Control pin. This pin should be left disconnected to minimize hysteresis. Connect to Vee with a resistor to add the desired amount of hysteresis.	
13	Vee	Negative power supply, -3V.	
15	RTN	Return for ESD protection, connect to GND.	
	Package Base	Do not DC GND. Thermal dissipation path only.	



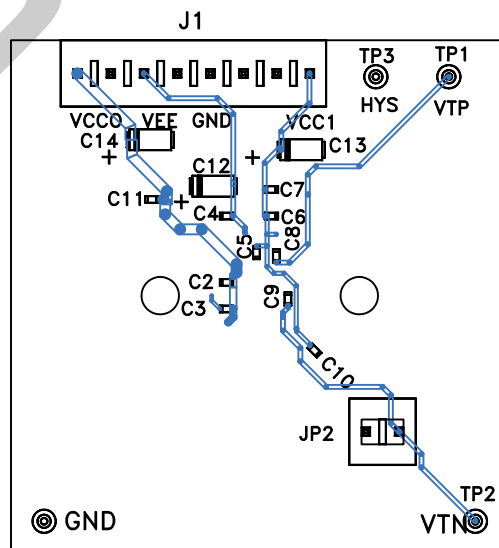
20 Gbps Clocked COMPARATOR with RSECL OUTPUT STAGE

Evaluation PCB

Front Side



Back Side



Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 Phone: 781-329-4700 • Order online at www.analog.com Application Support: Phone: 1-800-ANALOG-D



**20 Gbps Clocked COMPARATOR
with RSECL OUTPUT STAGE**

List of Materials for Evaluation PCB 125932 [1]

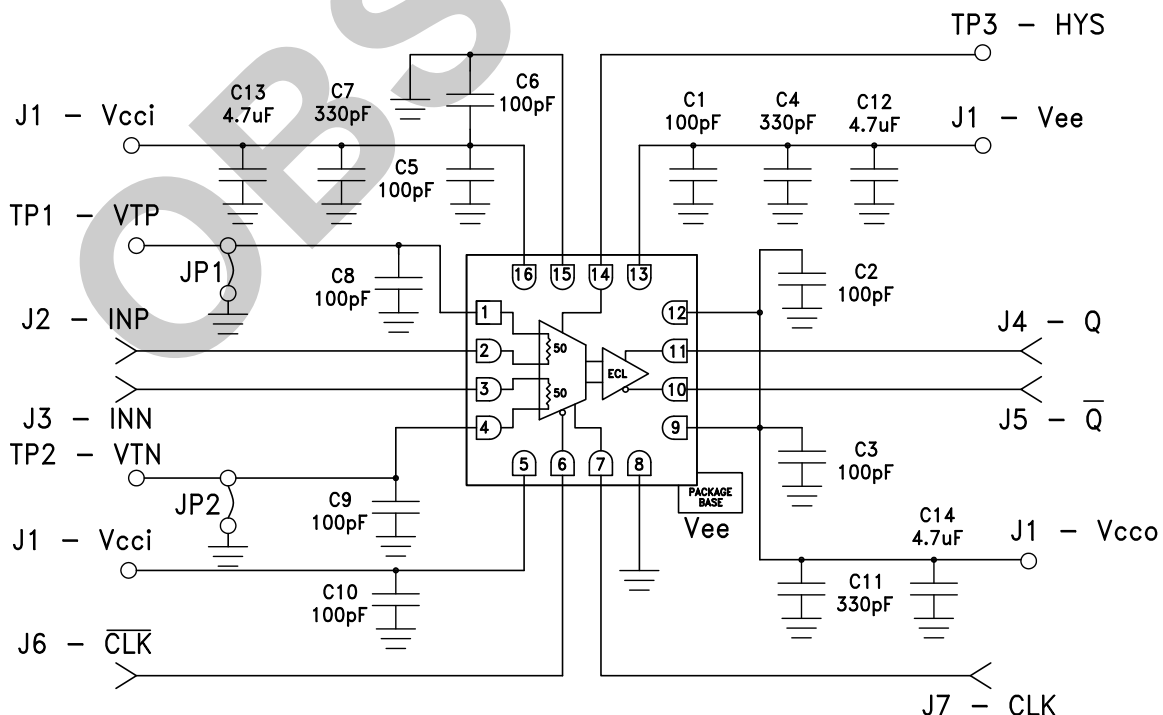
Item	Description
J1	8 Pos. Vertical TIN
J2 - J7	2.92 mm 40 GHz Jack
J8	Terminal Strip, Single Row 3 Pin SMT
JP1, JP2	2 Pos. Vertical TIN
C1 - C3, C5, C6, C8 - C10	100 pF Capacitor, 0402 Pkg.
C4, C7, C11	330 pF Capacitor, 0402 Pkg.
C11 - C13	4.7 uF Tantalum
TP1 - TP4	DC Pin, Swage Mount
U1	HMC876LC3C Comparator
PCB	125929 Evaluation PCB

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed paddle should not be electronically connected to DC GND, thermal dissipation path only. A sufficient number of via holes should be used to connect the top and bottom ground planes in order to provide good RF grounding to 25 GHz. The evaluation circuit board shown is available from Hittite upon request.

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25FR

Application Circuit



Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 Phone: 781-329-4700 • Order online at www.analog.com Application Support: Phone: 1-800-ANALOG-D



**20 Gbps Clocked COMPARATOR
with RSECL OUTPUT STAGE**

Application Circuits: CLK, $\overline{\text{CLK}}$ Interfacing

Figure A1: Resistor Network

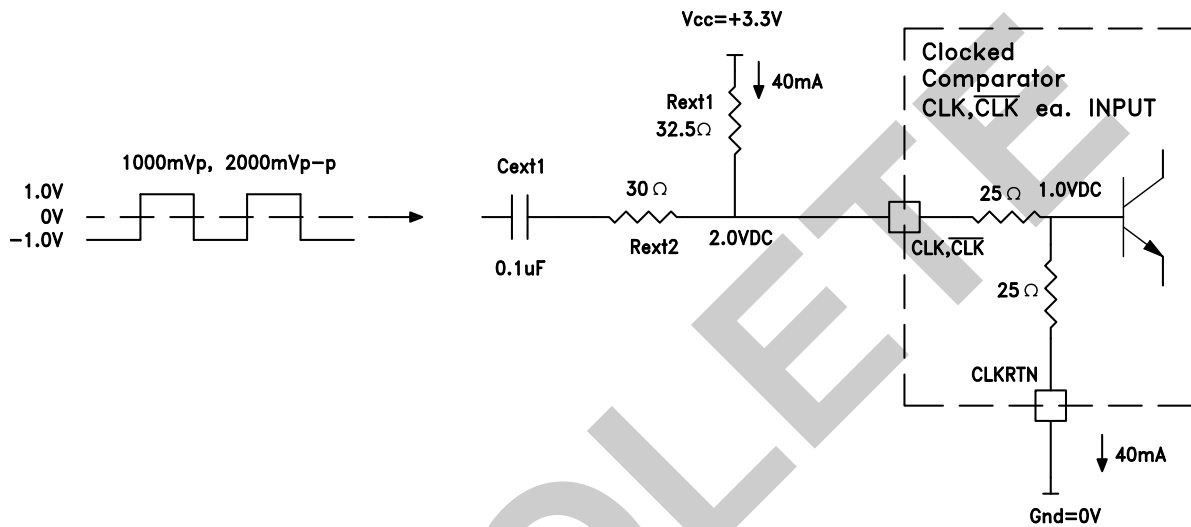
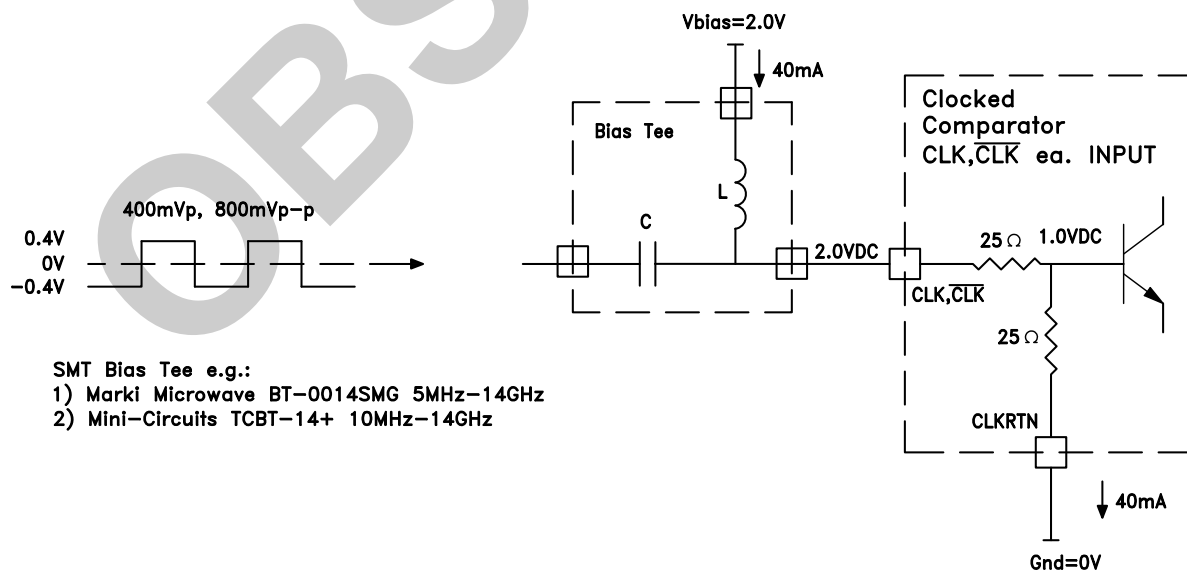


Figure A2: Bias Tee



- SMT Bias Tee e.g.:
- 1) Marki Microwave BT-0014SMG 5MHz-14GHz
 - 2) Mini-Circuits TCBT-14+ 10MHz-14GHz