

74F843

9-Bit Transparent Latch

General Description

The 74F843 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity.

Features

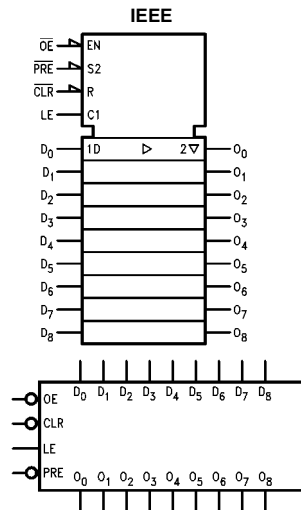
- 3-STATE output

Ordering Code:

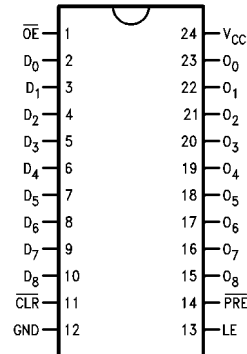
Order Number	Package Number	Package Description
74F843SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F843SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L.	Input I_{IH}/I_{IL}
		HIGH/LOW	Output I_{OH}/I_{OL}
D ₀ -D ₈	Data Inputs	1.0/1.0	20 μ A/-0.6 mA
\overline{OE}	Output Enable Input	1.0/1.0	20 μ A/-0.6 mA
LE	Latch Enable	1.0/1.0	20 μ A/-0.6 mA
\overline{CLR}	Clear	1.0/1.0	20 μ A/-0.6 mA
\overline{PRE}	Preset	1.0/1.0	20 μ A/-0.6 mA
O ₀ -O ₈	3-STATE Data Outputs	150/40	-3 mA/24 mA

Functional Description

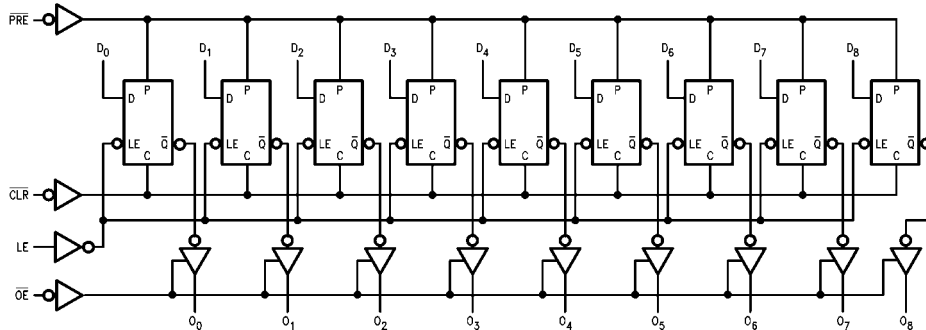
The 74F843 consists of nine D-type latches with 3-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH, the bus output is in the high impedance state. In addition to the LE and \overline{OE} pins, the 74F843 has a Clear (\overline{CLR}) pin and a Preset (\overline{PRE}). These pins are ideal for parity bus interfacing in high performance systems. When \overline{CLR} is LOW, the outputs are LOW if \overline{OE} is LOW. When \overline{CLR} is HIGH, data can be entered into the latch. When \overline{PRE} is LOW, the Outputs are HIGH if \overline{OE} is LOW. Preset overrides \overline{CLR} .

Function Table

Inputs					Internal	Output	Function
\overline{CLR}	\overline{PRE}	\overline{OE}	LE	D	Q	O	
H	H	X	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched
H	L	H	L	X	H	Z	Latched

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC} 10% V _{CC} 5% V _{CC} 5% V _{CC}	2.5 2.4 2.7 2.7		V	Min	I _{OH} = -1 mA I _{OH} = -3 mA I _{OH} = -1 mA I _{OH} = -3 mA
V _{OL}	Output LOW Voltage	10% V _{CC}		0.5	V	Min	I _{OL} = 24 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All other pins grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All other pins grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{OZH}	Output Leakage Current			50	μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current			-50	μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V
I _{CC}	Power Supply Current		65	90	mA	Max	

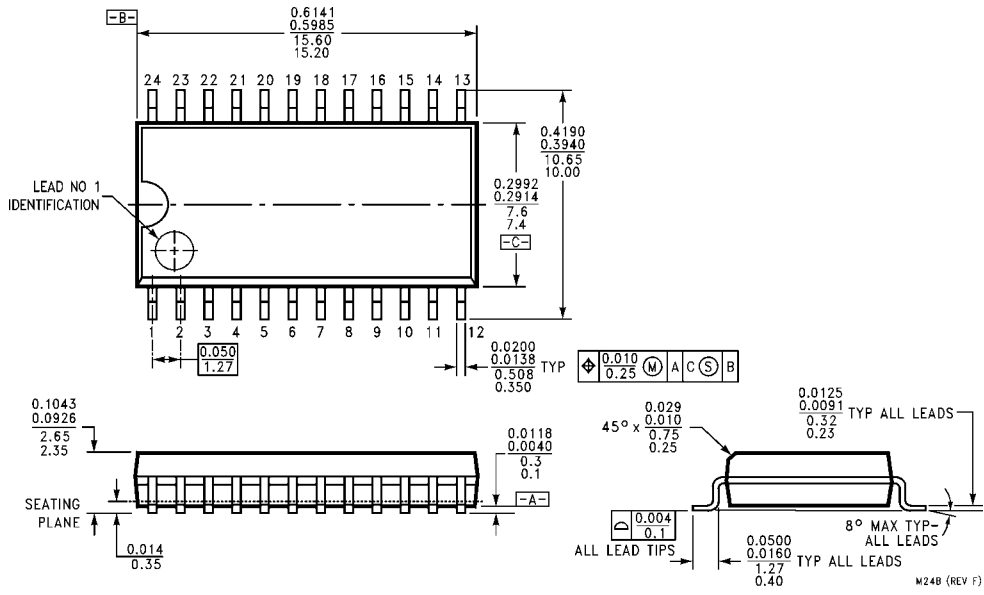
AC Electrical Characteristics

Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay	2.5	5.4	8.0	2.0	9.0	ns
t _{PHL}	D _n to O _n	1.5	4.2	6.5	1.5	7.0	
t _{PLH}	Propagation Delay	5.0	8.5	12.0	4.5	13.5	ns
t _{PHL}	LE to O _n	2.0	4.7	7.5	2.0	8.0	
t _{PLH}	Propagation Delay PRE to O _n	3.0	7.3	10.0	2.5	11.0	ns
t _{PHL}	Propagation Delay CLR to O _n	3.0	6.9	10.0	2.5	11.0	ns
t _{PZH}	Output Enable Time	2.5	5.0	8.5	2.0	9.5	ns
t _{PZL}	OE to O _n	2.5	6.1	9.0	2.0	10.0	
t _{PHZ}	Output Disable Time	1.0	3.6	6.5	1.0	7.5	ns
t _{PLZ}	OE to O _n	1.0	3.4	6.5	1.0	7.5	

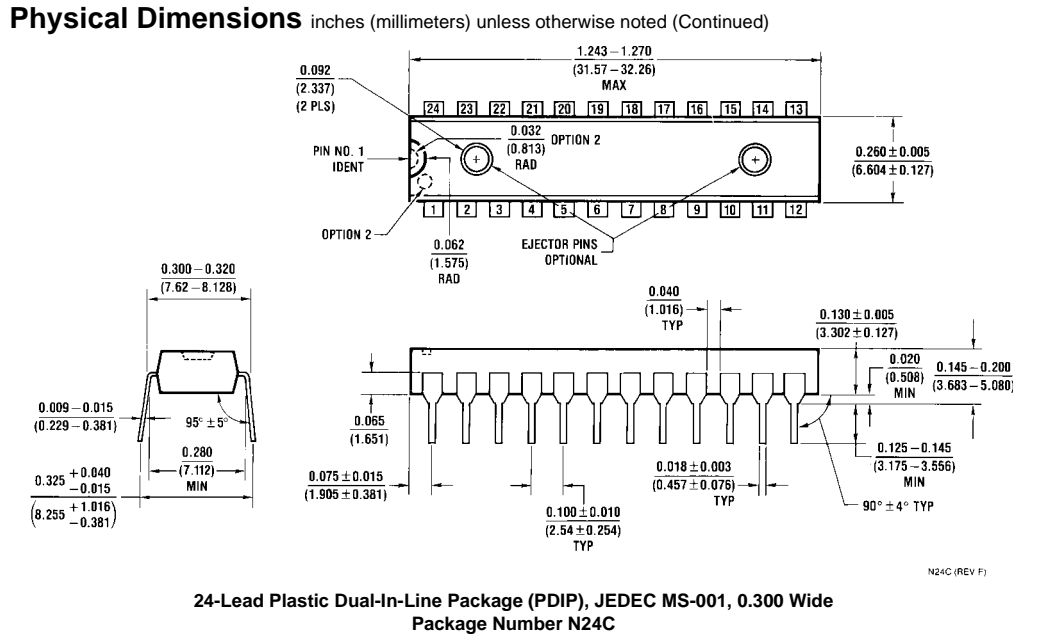
AC Operating Requirements

Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V		T _A = 0°C to +70°C V _{CC} = +5.0V		Units
		Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	2.0		2.5		ns
t _S (L)	D _n to LE	2.0		2.5		
t _H (H)	Hold Time, HIGH or LOW	2.5		3.0		ns
t _H (L)	D _n to LE	3.0		3.5		
t _W (H)	LE Pulse Width, HIGH	4.0		4.0		ns
t _W (L)	PRE Pulse Width, LOW	5.0		5.0		ns
t _W (L)	CLR Pulse Width, LOW	5.0		5.0		ns
t _{REC}	PRE Recovery Time	10.0		10.0		ns
t _{REC}	CLR Recovery Time	12.0		13.0		ns

Physical Dimensions inches (millimeters) unless otherwise noted



**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B**



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