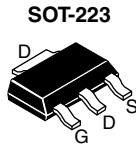


## Power MOSFET



P-Channel MOSFET

### FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dv/dt rating
- Repetitive avalanche rated
- P-channel
- Fast switching
- Ease of paralleling
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available

### DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-223 package is designed for surface-mount using vapor phase, infrared, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25 W is possible in a typical surface mount application.

Marking code: FF

PRODUCT SUMMARY		
$V_{DS}$ (V)	-100	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = -10$ V	1.2
$Q_g$ max. (nC)	8.7	
$Q_{gs}$ (nC)	2.2	
$Q_{gd}$ (nC)	4.1	
Configuration	Single	

ORDERING INFORMATION	
Package	SOT-223
Lead (Pb)-free and halogen-free	SiHFL9110TR-GE3 <sup>a</sup> IRFL9110TRPbF-BE3 <sup>a, b</sup>
Lead (Pb)-free	IRFL9110TRPbF <sup>a</sup>

#### Notes

- See device orientation
- “-BE3” denotes alternate manufacturing location

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	$V_{DS}$	-100	V	
Gate-source voltage	$V_{GS}$	$\pm 20$		
Continuous drain current	$V_{GS}$ at -10 V	$T_C = 25$ °C	-1.1	A
		$T_C = 100$ °C	-0.69	
Pulsed drain current <sup>a</sup>	$I_{DM}$	-8.8	W/°C	
Linear derating factor		0.025		
Linear derating factor (PCB mount) <sup>e</sup>		0.017		
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	100	mJ	
Avalanche current <sup>a</sup>	$I_{AR}$	-1.1	A	
Repetitive avalanche energy <sup>a</sup>	$E_{AR}$	0.31	mJ	
Maximum power dissipation	$P_D$	$T_C = 25$ °C	3.1	W
		$T_A = 25$ °C	2.0	
Peak diode recovery dv/dt <sup>c</sup>	dv/dt	-5.5	V/ns	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C	
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s	300		

#### Notes



- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = -25$  V, starting  $T_J = 25$  °C,  $L = 7.7$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = -4.4$  A (see fig. 12)
- $I_{SD} \leq -4.4$  A,  $di/dt \leq -75$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C
- 1.6 mm from case
- When mounted on 1" square PCB (FR-4 or G-10 material)



THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum junction-to-ambient (PCB mount) <sup>a</sup>	$R_{thJA}$	-	-	60	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	-	-	40	

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$		-100	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = -1\text{ mA}$		-	-0.091	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$		-2.0	-	-4.0	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}$		-	-	-100	$\mu\text{A}$
		$V_{DS} = -80\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	-500	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -0.66\text{ A}^b$	-	-	1.2	$\Omega$
Forward transconductance	$g_{fs}$	$V_{DS} = -50\text{ V}, I_D = -0.66\text{ A}$		0.82	-	-	S
<b>Dynamic</b>							
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = -25\text{ V},$ $f = 1.0\text{ MHz}$ , see fig. 5		-	200	-	pF
Output capacitance	$C_{oss}$			-	94	-	
Reverse transfer capacitance	$C_{rss}$			-	18	-	
Total gate charge	$Q_g$	$V_{GS} = -10\text{ V}$	$I_D = -4.0\text{ A}, V_{DS} = -80\text{ V},$ see fig. 6 and 13 <sup>b</sup>	-	-	8.7	nC
Gate-source charge	$Q_{gs}$			-	-	2.2	
Gate-drain charge	$Q_{gd}$			-	-	4.1	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -50\text{ V}, I_D = -4.0\text{ A},$ $R_g = 24\text{ }\Omega, R_D = 11\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	10	-	ns
Rise time	$t_r$			-	27	-	
Turn-off delay time	$t_{d(off)}$			-	15	-	
Fall time	$t_f$			-	17	-	
Internal drain inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.0	-	nH
Internal source inductance	$L_S$			-	6.0	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	-1.1	A
Pulsed diode forward current <sup>a</sup>	$I_{SM}$			-	-	-8.8	
Body diode voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = -1.1\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	-5.5	V
Body diode reverse recovery time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = -4.0\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	80	160	ns
Body diode reverse recovery charge	$Q_{rr}$			-	0.15	0.30	$\mu\text{C}$
Forward turn-on time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\text{ }\%$

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

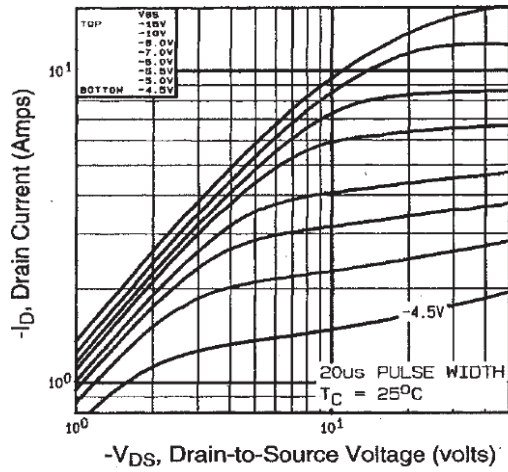


Fig. 1 - Typical Output Characteristics

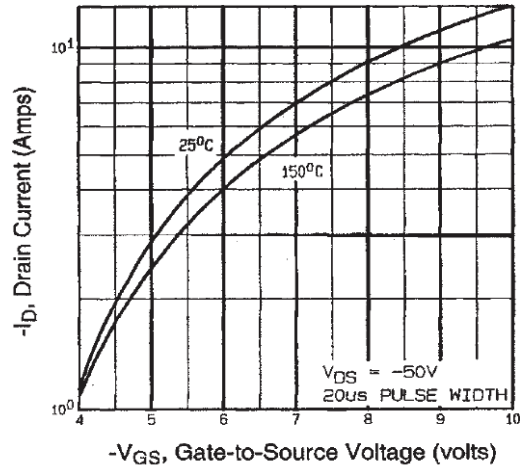


Fig. 3 - Typical Transfer Characteristics

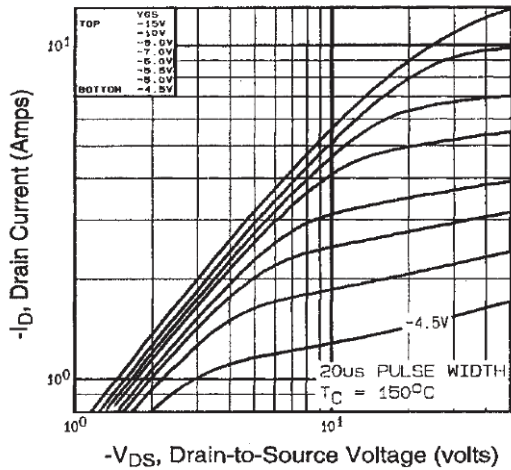


Fig. 2 - Typical Output Characteristics

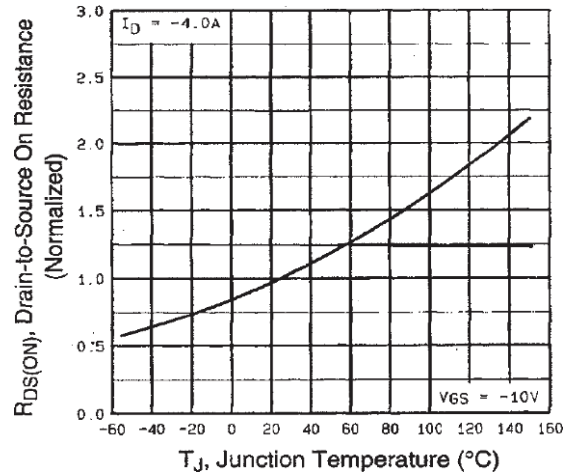


Fig. 4 - Normalized On-Resistance vs. Temperature

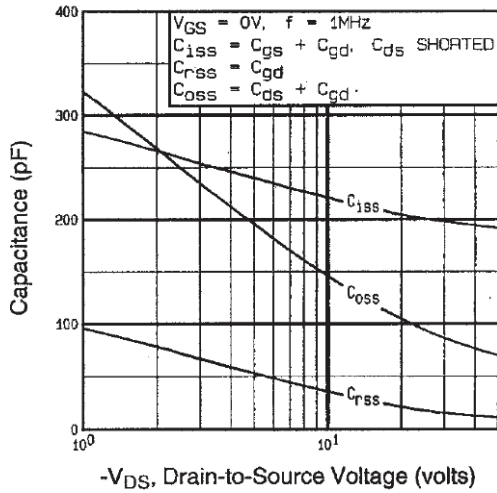


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

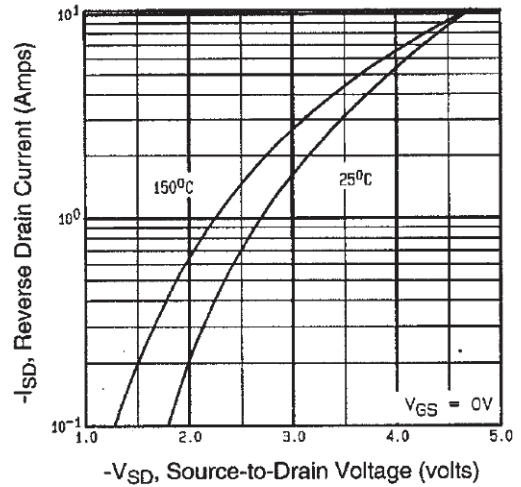


Fig. 7 - Typical Source-Drain Diode Forward Voltage



Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

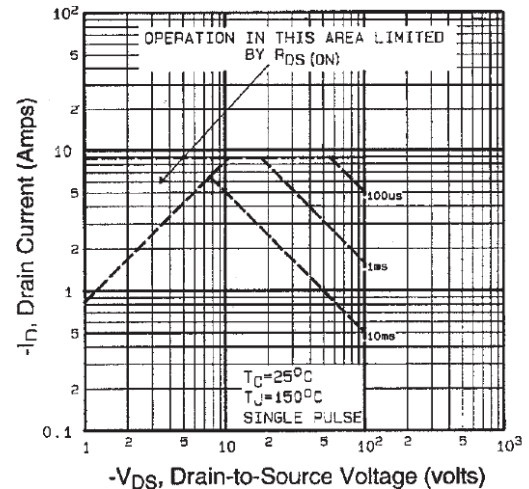


Fig. 8 - Maximum Safe Operating Area

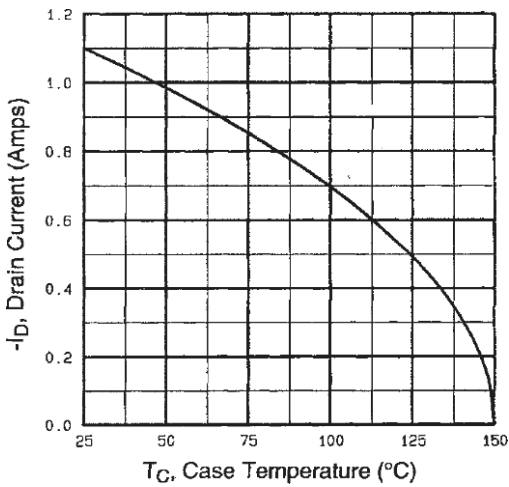


Fig. 9 - Maximum Drain Current vs. Case Temperature



Fig. 10a - Switching Time Test Circuit

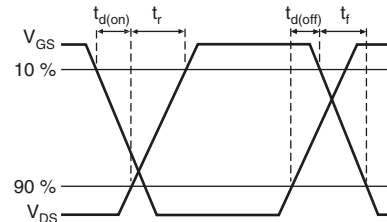


Fig. 10b - Switching Time Waveforms

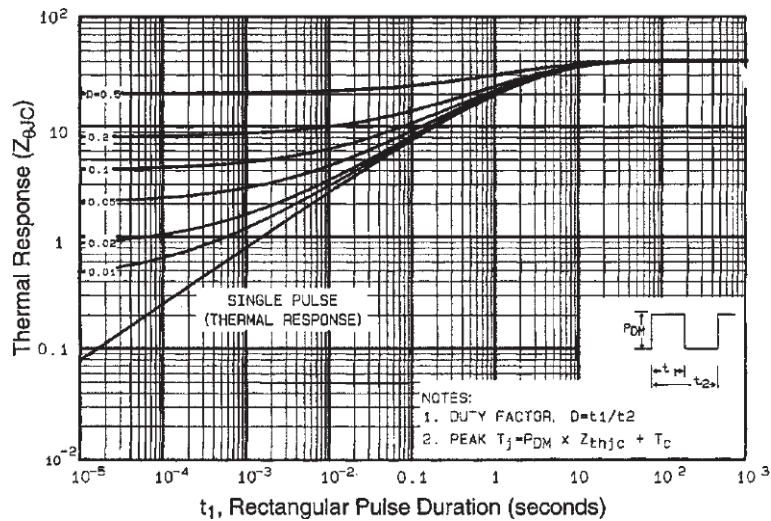


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

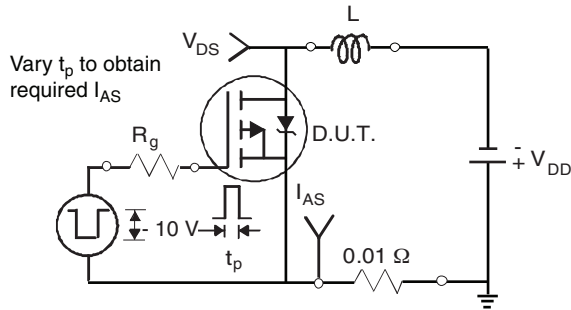


Fig. 12a - Unclamped Inductive Test Circuit

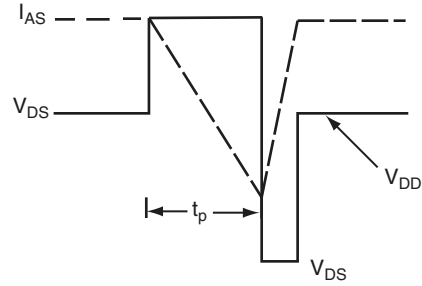


Fig. 12b - Unclamped Inductive Waveforms

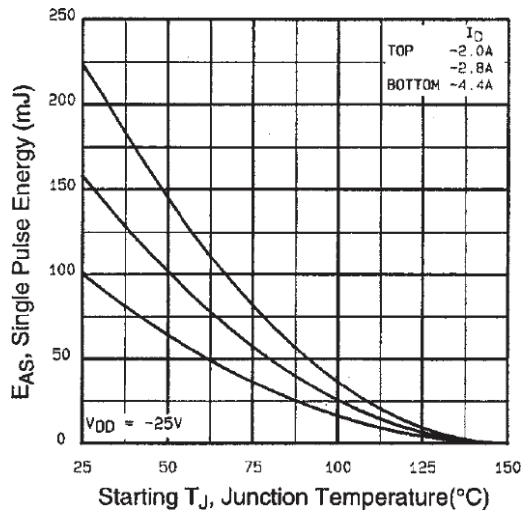


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

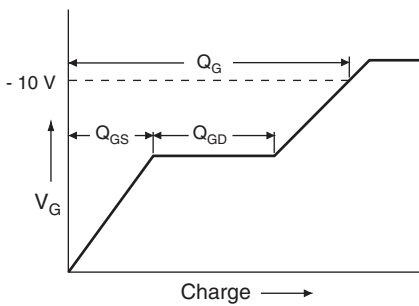


Fig. 13a - Basic Gate Charge Waveform

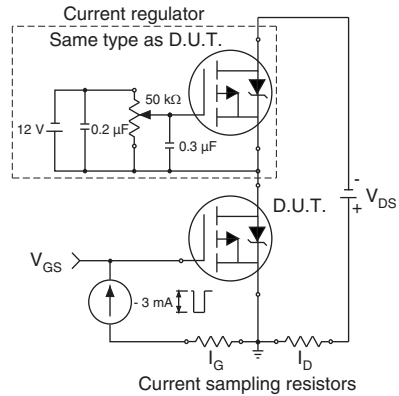
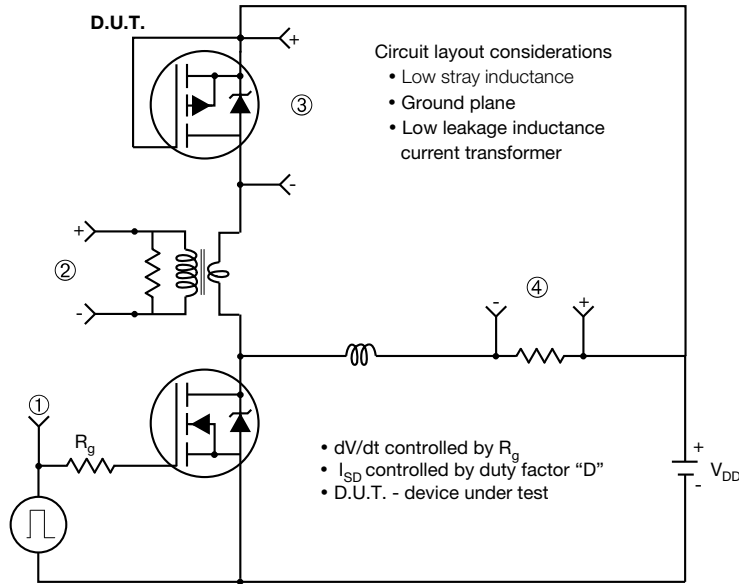


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



**Note**

- Compliment N-Channel of D.U.T. for driver



**Note**

a.  $V_{GS} = -5 V$  for logic level and  $-3 V$  drive devices

Fig. 14 - For P-Channel

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## SOT-223 (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.55	1.80	0.061	0.071
B	0.65	0.85	0.026	0.033
B1	2.95	3.15	0.116	0.124
C	0.25	0.35	0.010	0.014
D	6.30	6.70	0.248	0.264
E	3.30	3.70	0.130	0.146
e	2.30 BSC		0.0905 BSC	
e1	4.60 BSC		0.181 BSC	
H	6.71	7.29	0.264	0.287
L	0.91	-	0.036	-
L1	0.061 BSC		0.0024 BSC	
θ	-	10'	-	10'

ECN: S-82109-Rev. A, 15-Sep-08  
DWG: 5969

### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension do not include mold flash.
4. Outline conforms to JEDEC outline TO-261AA.





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