

CD4027BC

Dual J-K Master/Slave Flip-Flop with Set and Reset

General Description

The CD4027BC dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. Each flip-flop has independent J, K, set, reset, and clock inputs and buffered Q and \bar{Q} outputs. These flip-flops are edge sensitive to the clock input and change state on the positive-going transition of the clock pulses. Set or reset is independent of the clock and is accomplished by a high level on the respective input.

All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS} .

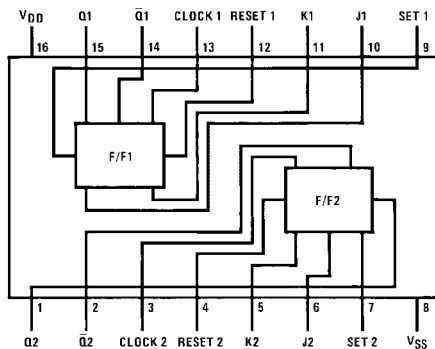
Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: $0.45 V_{DD}$ (typ.)
- Low power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS
- Low power: 50 nW (typ.)
- Medium speed operation: 12 MHz (typ.) with 10V supply

Ordering Code:

| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| CD4027BCM | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| CD4027BCN | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Connection Diagram



Top View

Truth Table

| CL (Note 3) | Inputs t_{n-1} (Note 1) | | | | | Outputs t_n (Note 2) | |
|----------------|------------------------------|---|---|---|---|---------------------------|-----------|
| | J | K | S | R | Q | Q | \bar{Q} |
| ↗ | 1 | X | 0 | 0 | 0 | 1 | 0 |
| ↘ | X | 0 | 0 | 0 | 1 | 1 | 0 |
| ↖ | 0 | X | 0 | 0 | 0 | 0 | 1 |
| ↙ | X | 1 | 0 | 0 | 1 | 0 | 1 |
| ↔ | X | X | 0 | 0 | X | (No Change) | |
| X | X | X | 1 | 0 | X | 1 | 0 |
| X | X | X | 0 | 1 | X | 0 | 1 |
| X | X | X | 1 | 1 | X | 1 | 1 |

1 = HIGH Level
0 = LOW Level
X = Don't Care
↗ = LOW-to-HIGH
↘ = HIGH-to-LOW

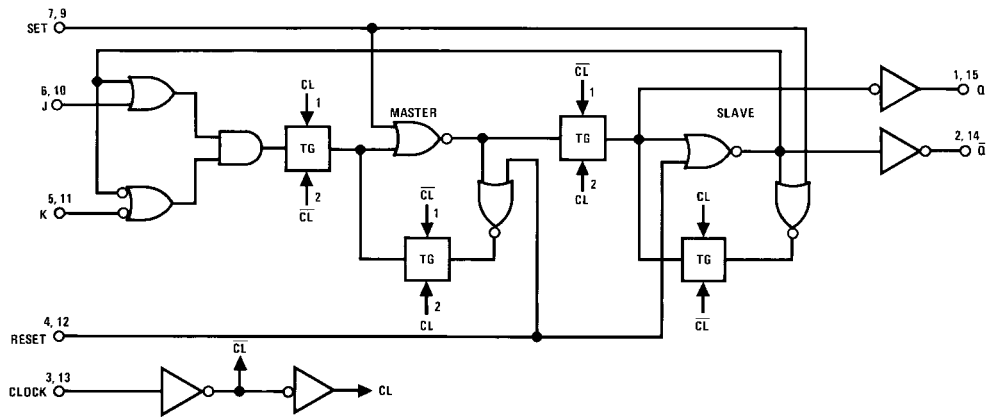
Note 1: t_{n-1} refers to the time interval prior to the positive clock pulse transition

Note 2: t_n refers to the time intervals after the positive clock pulse transition

Note 3: Level Change

CD4027BC

Logic Diagram



Absolute Maximum Ratings (Note 4)

(Note 5)

| | |
|-------------------------------------|---------------------------------|
| DC Supply Voltage (V_{DD}) | -0.5 V_{DC} to +18 V_{DC} |
| Input Voltage (V_{IN}) | -0.5V to V_{DD} +0.5 V_{DC} |
| Storage Temperature Range (T_S) | -65°C to +150°C |
| Power Dissipation (P_D) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Lead Temperature (T_L) | |
| (Soldering, 10 seconds) | 260°C |

Recommended Operating Conditions (Note 5)

| | |
|---------------------------------------|-------------------------|
| DC Supply Voltage (V_{DD}) | 3V to 15 V_{DC} |
| Input Voltage (V_{IN}) | 0V to V_{DD} V_{DC} |
| Operating Temperature Range (T_A) | -55°C to +125°C |

Note 4: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 5: $V_{SS} = 0V$ unless otherwise specified.

DC Electrical Characteristics (Note 6)

| Symbol | Parameter | Conditions | -55°C | | +25°C | | | +125°C | | Units |
|----------|------------------------------------|---|-------|------|-------|------------|------|--------|------|---------|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| I_{DD} | Quiescent Device Current | $V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS} | | 1 | | | 1 | | 30 | μA |
| | | $V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS} | | 2 | | | 2 | 60 | | |
| | | $V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS} | | 4 | | | 4 | 120 | | |
| V_{OL} | LOW Level Output Voltage | $ I_{OL} < 1 \mu A$ | | | | | | | | V |
| | | $V_{DD} = 5V$ | | 0.05 | | 0 | 0.05 | | 0.05 | |
| | | $V_{DD} = 10V$ | | 0.05 | | 0 | 0.05 | | 0.05 | |
| V_{OH} | HIGH Level Output Voltage | $ I_{OL} < 1 \mu A$ | | | | | | | | V |
| | | $V_{DD} = 5V$ | 4.95 | | 4.95 | 5 | | 4.95 | | |
| | | $V_{DD} = 10V$ | 9.95 | | 9.95 | 10 | | 9.95 | | |
| V_{IL} | LOW Level Input Voltage | $V_{DD} = 5V, V_O = 0.5V$ or $4.5V$ | | 1.5 | | | 1.5 | | 1.5 | V |
| | | $V_{DD} = 10V, V_O = 1V$ or $9V$ | | 3.0 | | | 3.0 | | 3.0 | |
| | | $V_{DD} = 15V, V_O = 1.5V$ or $13.5V$ | | 4.0 | | | 4.0 | | 4.0 | |
| V_{IH} | HIGH Level Input Voltage | $V_{DD} = 5V, V_O = 0.5V$ or $4.5V$ | 3.5 | | 3.5 | | | 3.5 | | V |
| | | $V_{DD} = 10V, V_O = 1V$ or $9V$ | 7.0 | | 7.0 | | | 7.0 | | |
| | | $V_{DD} = 15V, V_O = 1.5V$ or $13.5V$ | 11.0 | | 11.0 | | | 11.0 | | |
| I_{OL} | LOW Level Output Current (Note 7) | $V_{DD} = 5V, V_O = 0.4V$ | 0.64 | | 0.51 | 0.88 | | 0.36 | | mA |
| | | $V_{DD} = 10V, V_O = 0.5V$ | 1.6 | | 1.3 | 2.25 | | 0.9 | | |
| | | $V_{DD} = 15V, V_O = 1.5V$ | 4.2 | | 3.4 | 8.8 | | 2.4 | | |
| I_{OH} | HIGH Level Output Current (Note 7) | $V_{DD} = 5V, V_O = 4.6V$ | -0.64 | | -0.51 | -0.88 | | -0.36 | | mA |
| | | $V_{DD} = 10V, V_O = 9.5V$ | -1.6 | | -1.3 | -2.25 | | -0.9 | | |
| | | $V_{DD} = 15V, V_O = 13.5V$ | -4.2 | | -3.4 | -8.8 | | -2.4 | | |
| I_{IN} | Input Current | $V_{DD} = 15V, V_{IN} = 0V$ | | -0.1 | | -10^{-5} | -0.1 | | -1.0 | μA |
| | | $V_{DD} = 15V, V_{IN} = 15V$ | | 0.1 | | 10^{-5} | 0.1 | | 1.0 | |

Note 6: $V_{SS} = 0V$ unless otherwise specified.

Note 7: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 8)

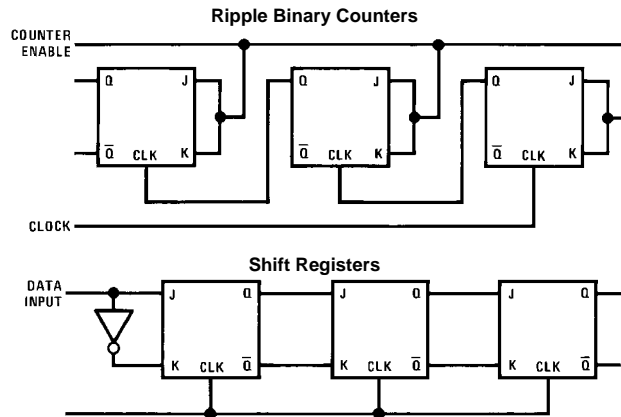
$T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $t_{rCL} = t_{fCL} = 20\text{ ns}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|------------------------|--|--|-------------------|-------------------|-------------------|---------------|
| t_{PHL} or t_{PLH} | Propagation Delay Time from Clock to Q or \bar{Q} | $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$ | | 200 80 65 | 400 160 130 | ns |
| t_{PHL} or t_{PLH} | Propagation Delay Time from Set to \bar{Q} or Reset to Q | $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$ | | 170 70 55 | 340 140 110 | ns |
| t_{PHL} or t_{PLH} | Propagation Delay Time from Set to Q or Reset to \bar{Q} | $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$ | | 110 50 40 | 220 100 80 | ns |
| t_S | Minimum Data Setup Time | $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$ | | 135 55 45 | 270 110 90 | ns |
| t_{THL} or t_{TLH} | Transition Time | $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$ | | 100 50 40 | 200 100 80 | ns |
| f_{CL} | Maximum Clock Frequency (Toggle Mode) | $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$ | 2.5 6.2 7.6 | 5 12.5 15.5 | | MHz |
| t_{rCL} or t_{fCL} | Maximum Clock Rise and Fall Time | $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$ | 15 10 5 | | | μs |
| t_W | Minimum Clock Pulse Width ($t_{WH} = t_{WL}$) | $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$ | | 100 40 32 | 200 80 65 | ns |
| t_{WH} | Minimum Set and Reset Pulse Width | $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$ | | 80 30 25 | 160 60 50 | ns |
| C_{IN} | Average Input Capacitance | Any Input | | 5 | 7.5 | pF |
| C_{PD} | Power Dissipation Capacity | Per Flip-Flop (Note 9) | | 35 | | pF |

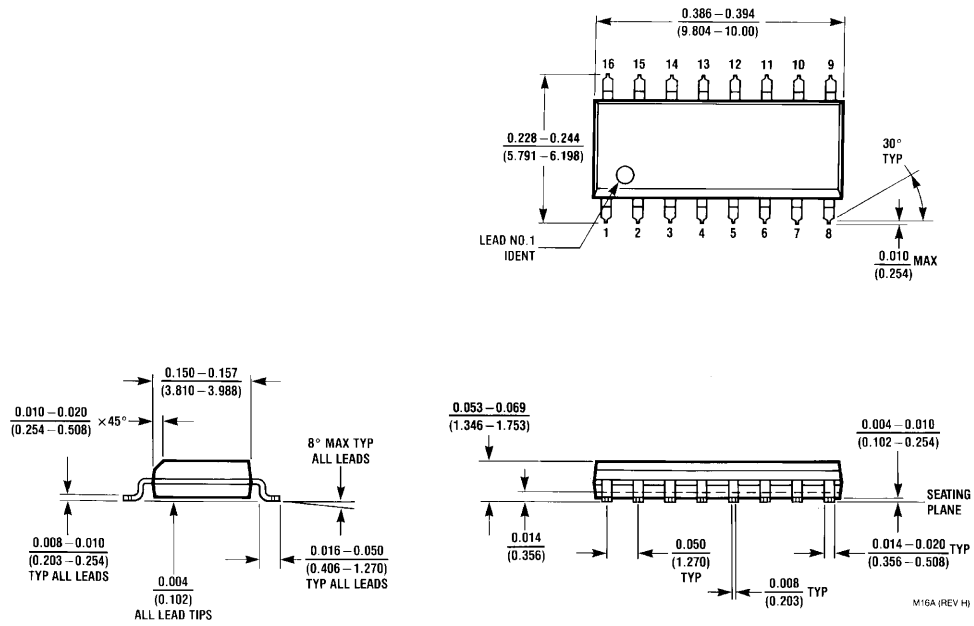
Note 8: AC Parameters are guaranteed by DC correlated testing.

Note 9: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 74C Family Characteristics application note, AN-90.

Typical Applications

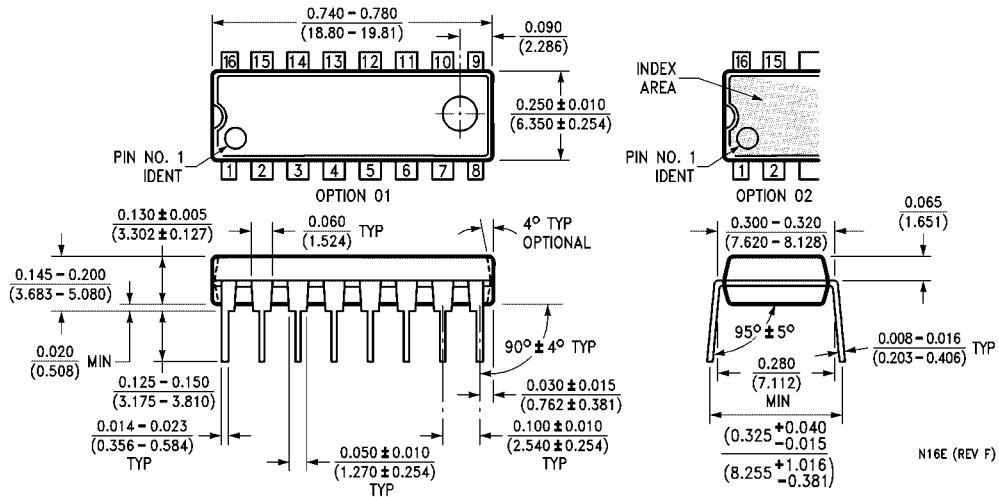


Physical Dimensions inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E**

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