

## FEATURES

**Conversion gain: 15 dB typical**  
**Sideband rejection: 22 dBc typical**  
**Output P1dB compression at maximum gain: 22 dBm typical**  
**Output IP3 at maximum gain: 35 dBm typical**  
**LO to RF isolation: 4 dB typical**  
**LO to IF isolation: 9 dB typical**  
**RF return loss: 20 dB typical**  
**LO return loss: 10 dB typical**  
**IF return loss: 20 dB typical**  
**Exposed paddle, 5 mm × 5 mm, 32-terminal, leadless chip carrier package**

## APPLICATIONS

**Point to point and point to multipoint radios**  
**Military radars, electronic warfare (EW), and electronic intelligence (ELINT)**  
**Satellite communications**  
**Sensors**

## GENERAL DESCRIPTION

The HMC6505A is a compact gallium arsenide (GaAs), pseudomorphic (pHEMT), monolithic microwave integrated circuit (MMIC) upconverter in a RoHS compliant package that operates from 5.5 GHz to 8.6 GHz. This device provides a small signal conversion gain of 15 dB with 22 dBc of sideband rejection. The HMC6505A uses a variable gain amplifier (VGA) preceded by an in-phase and quadrature (I/Q) mixer that is driven by an active local oscillator (LO). The IF1 and IF2 mixer inputs are provided, and an external 90° hybrid is needed to select the required sideband. The I/Q mixer topology reduces

## FUNCTIONAL BLOCK DIAGRAM

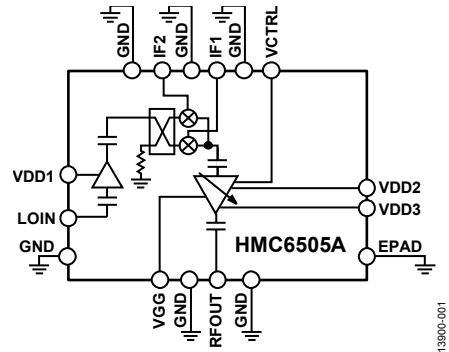


Figure 1.

the need for filtering of unwanted sideband. The HMC6505A is a smaller alternative to hybrid style single sideband (SSB) upconverter assemblies, and it eliminates the need for wire bonding by allowing the use of surface-mount manufacturing techniques.

The HMC6505A is available in 5 mm × 5 mm, 32-terminal leadless chip carrier (LCC) package and operates over a -40°C to +85°C temperature range. An evaluation board for the HMC6505A is also available upon request.

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## REVISION HISTORY

8/2017—Revision 0: Initial Version

## SPECIFICATIONS

$T_A = 25^\circ\text{C}$ ,  $IF = 350\text{ MHz}$ ,  $VDDx = 5\text{ V}$ ,  $VCTRL = -4\text{ V}$ ,  $LO\text{ power} = 4\text{ dBm}$ . Measurements performed with lower sideband selected and external  $90^\circ$  hybrid at the IF ports, unless otherwise noted.

Table 1.

| Parameter   | Symbol     | Min | Typ | Max  | Unit |
|---|------------|-----|-----|------|------|
| <b>OPERATING CONDITIONS</b>                       |            |     |     |      |      |
| Frequency Range                                   |            |     |     |      |      |
| Radio Frequency                                   | RF         | 5.5 |     | 8.6  | GHz  |
| Local Oscillator                                  | LO         | 2.5 |     | 11.6 | GHz  |
| Intermediate Frequency                            | IF         | DC  |     | 3    | GHz  |
| Control Voltage Range                             | VCTRL      | -4  |     | 0    | V    |
| LO Drive Range                                    |            | -2  | +4  | +6   | dBm  |
| <b>PERFORMANCE</b>                                |            |     |     |      |      |
| Conversion Gain                                   |            | 12  | 15  |      | dB   |
| Dynamic Range                                     |            | 20  | 25  |      | dB   |
| Sideband Rejection                                |            | 18  | 22  |      | dBc  |
| Output Power for 1 dB Compression at Maximum Gain | OP1dB      |     | 22  |      | dBm  |
| Output Third-Order Intercept at Maximum Gain      | OIP3       | 31  | 35  |      | dBm  |
| Isolation   |            |     |     |      |      |
| LO to RF  |            | -1  | +4  |      | dB   |
| LO to IF  |            |     | 9   |      | dB   |
| Noise Figure                                      | NF         |     | 15  |      | dB   |
| Return Loss                                       |            |     |     |      |      |
| RF  |            |     | 20  |      | dB   |
| LO  |            |     | 10  |      | dB   |
| IF  |            |     | 20  |      | dB   |
| <b>POWER SUPPLY</b>                               |            |     |     |      |      |
| Total Supply Current                              |            |     |     |      |      |
| LO Amplifier                                      | IDD1       |     | 125 |      | mA   |
| RF Amplifier                                      | IDD2, IDD3 |     | 120 |      | mA   |

## ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter  | Rating          |
|--|-----------------|
| Drain Bias Voltage (VDD1, VDD2, and VDD3)            | 5.5 V           |
| Gate Bias Voltage                                    |                 |
| VGG  | –3 V to 0 V     |
| VCTRL  | –5 V to +0.3 V  |
| Input Power  |                 |
| LO   | 10 dBm          |
| IF   | 20 dBm          |
| Moisture Sensitivity Level (MSL) Rating <sup>1</sup> | MSL3            |
| Maximum Junction Temperature                         | 175°C           |
| Storage Temperature Range                            | –65°C to +150°C |
| Operating Temperature Range                          | –40°C to +85°C  |
| Reflow Temperature                                   | 260°C           |
| Electrostatic Discharge Sensitivity                  |                 |
| Human Body Model (HBM)                               | 500 V           |
| Field Induced Charged Device Model (FICDM)           | 750 V           |

<sup>1</sup> See the Ordering Guide.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 3. Thermal Resistance

| Package Type        | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---------------------|---------------|---------------|------|
| E-32-1 <sup>1</sup> | 66.7          | 54.6          | °C/W |

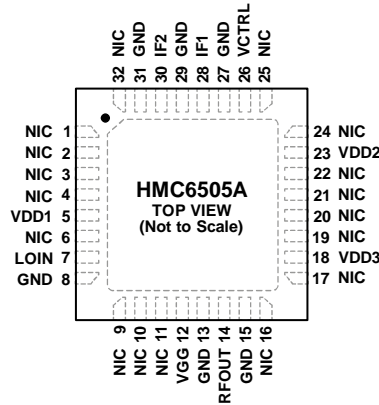
<sup>1</sup> Thermal impedance simulated values are based on JEDEC 252P test board with 5 × 5 thermal vias. Refer to JEDEC standard JESD51-2 for additional information.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES**
1. NOT INTERNALLY CONNECTED. THESE PINS ARE NOT CONNECTED INTERNALLY. HOWEVER, PINS MAY BE CONNECTED TO RF/DC GROUND WITHOUT AFFECTING PERFORMANCE.
  2. EXPOSED PAD. CONNECT TO A LOW IMPEDANCE THERMAL AND ELECTRICAL GROUND PLANE.

13900-002

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

| Pin No.  | Mnemonic   | Description  |
|--|------------|--|
| 1 to 4, 6, 9 to 11, 16, 17, 19 to 22, 24, 25, 32 | NIC        | Not Internally Connected. These pins are not connected internally. However, pins may be connected to RF/dc ground without affecting performance.   |
| 5  | VDD1       | Power Supply Voltage for LO Amplifier. See Figure 3 for the interface schematic. Refer to the typical application circuit (see Figure 103) for the required external components.   |
| 7  | LOIN       | Local Oscillator Input. See Figure 4 for the interface schematic. This pin is ac-coupled and matched to 50 Ω.  |
| 8, 13, 15, 27, 29, 31                            | GND        | Ground Connect. See Figure 5 for the interface schematic. These pins and package bottom must be connected to RF/dc ground.   |
| 12   | VGG        | Gate Voltage for the Variable Gain Amplifier. See Figure 6 for the interface schematic. Refer to the typical application circuit (see Figure 103) for the required external components.  |
| 14   | RFOUT      | Radio Frequency Output. See Figure 7 for the interface schematic. This pin is ac-coupled and matched to 50 Ω.  |
| 18, 23   | VDD3, VDD2 | Power Supply Voltage for the Variable Gain Amplifier. See Figure 8 for the interface schematic. Refer to the typical application circuit (see Figure 103) for the required external components.  |
| 26   | VCTRL      | Gain Control Voltage for the Variable Gain Amplifier. See Figure 9 for the interface schematic. Refer to the typical application circuit (see Figure 103) for the required external components.  |
| 28, 30   | IF1, IF2   | Quadrature Intermediate Frequency Inputs. See Figure 10 for the interface schematic. For applications not requiring operation to dc, use an off chip dc blocking capacitor. For operation to dc, these pins must not source or sink more than ±3 mA of current or device malfunction and failure can result. |
|  | EPAD       | Exposed Pad. Connect to a low impedance thermal and electrical ground plane.   |

INTERFACE SCHEMATICS

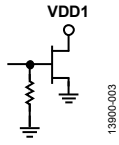


Figure 3. VDD1 Interface

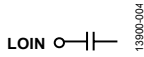


Figure 4. LOIN Interface



Figure 5. GND Interface

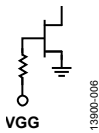


Figure 6. VGG Interface

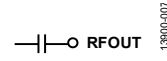


Figure 7. RFOUT Interface

VDD2, VDD3

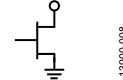


Figure 8. VDD2, VDD3 Interface

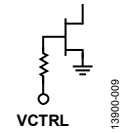


Figure 9. VCTRL Interface

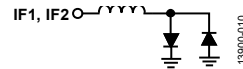


Figure 10. IF1, IF2 Interface

# TYPICAL PERFORMANCE CHARACTERISTICS

IF = 350 MHz, IF INPUT POWER = -6 dBm, LOWER SIDEBAND (HIGH-SIDE LO)

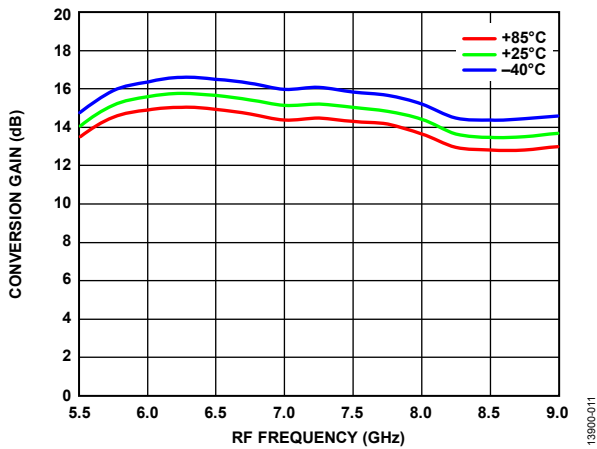


Figure 11. Conversion Gain vs. RF Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V

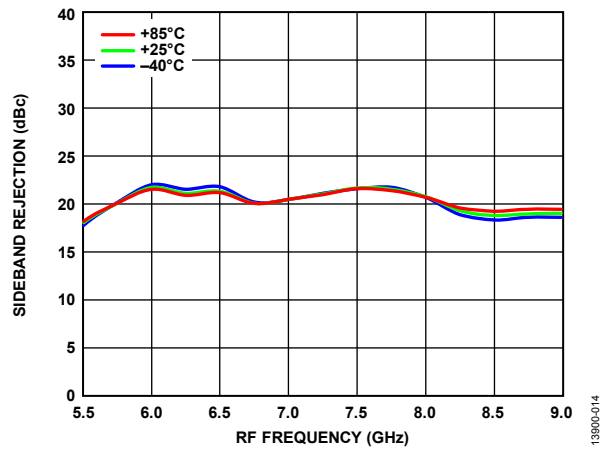


Figure 14. Sideband Rejection vs. RF Frequency over Temperatures, Voltage Control = -4 V

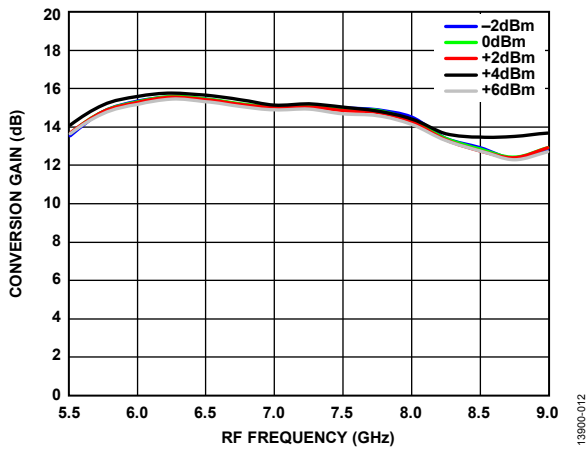


Figure 12. Conversion Gain vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V

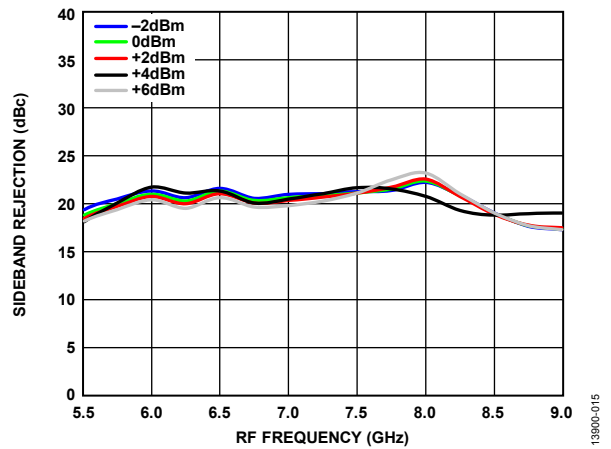


Figure 15. Sideband Rejection vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V

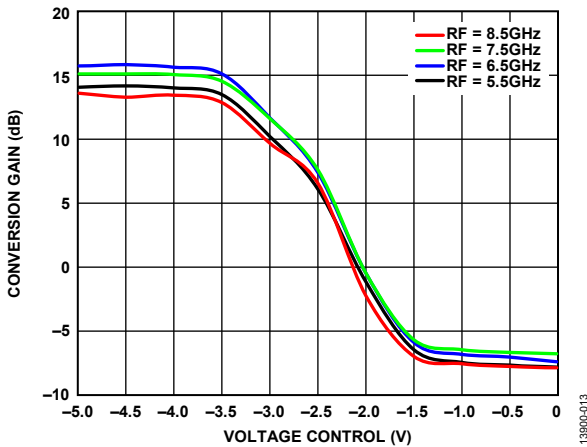


Figure 13. Conversion Gain vs. Voltage Control over RF, T<sub>A</sub> = 25°C, LO Power = 4 dBm

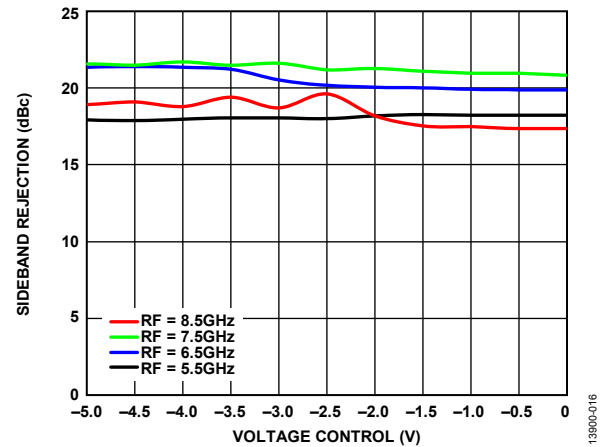
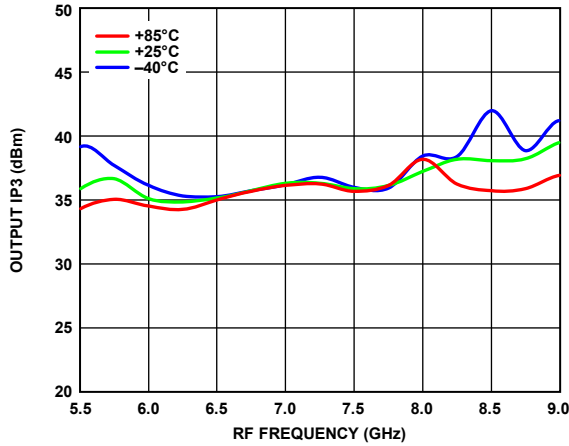
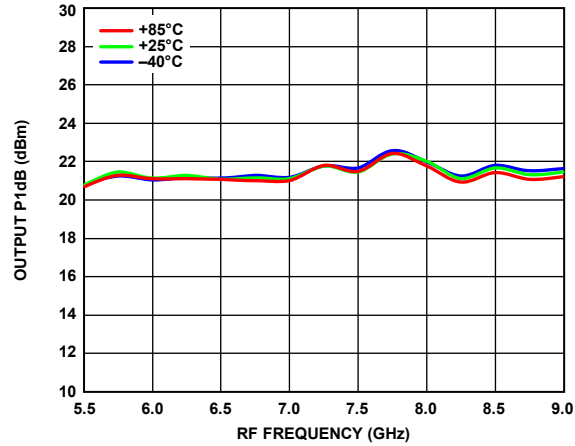


Figure 16. Sideband Rejection vs. Voltage Control over RF, T<sub>A</sub> = 25°C, LO Power = 4 dBm



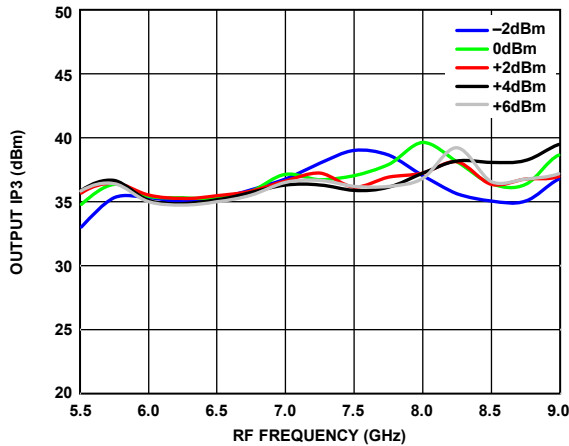
13900-017

Figure 17. Output IP3 vs. RF Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V



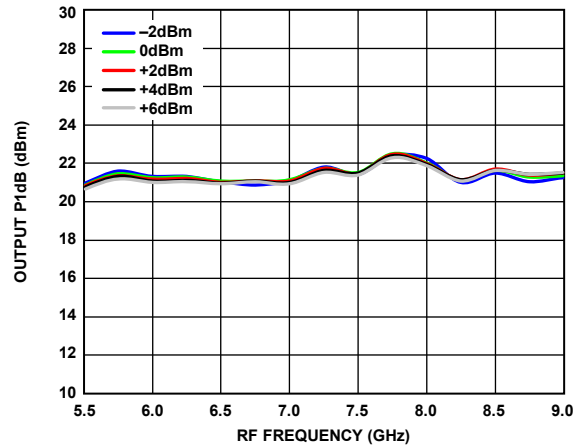
13900-020

Figure 20. Output P1dB vs. RF Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V



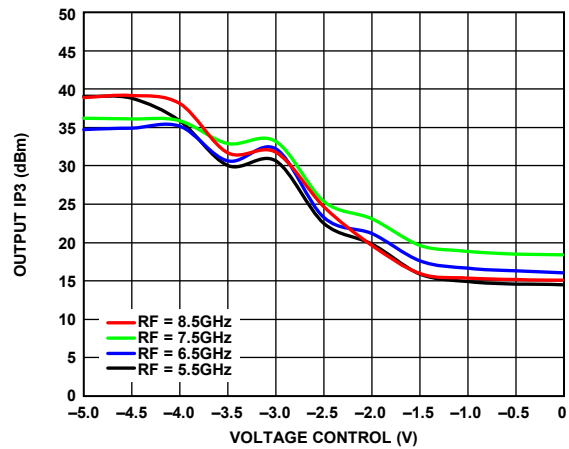
13900-018

Figure 18. Output IP3 vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V



13900-021

Figure 21. Output P1dB vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V



13900-019

Figure 19. Output IP3 vs. Voltage Control over RF Frequencies, T<sub>A</sub> = 25°C, LO Power = 4 dBm



**IF = 1000 MHz, IF INPUT POWER = -6 dBm, LOWER SIDEBAND (HIGH-SIDE LO)**

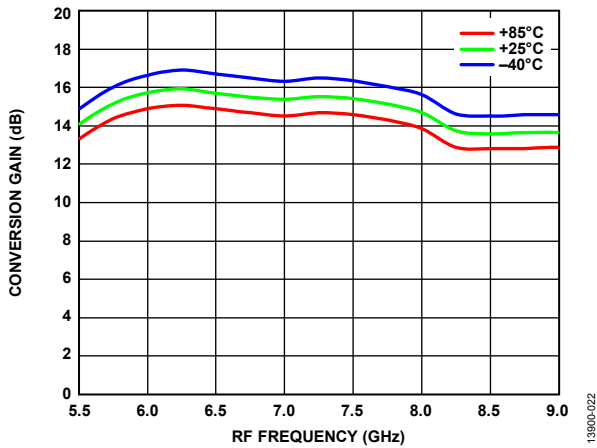


Figure 22. Conversion Gain vs. RF Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V

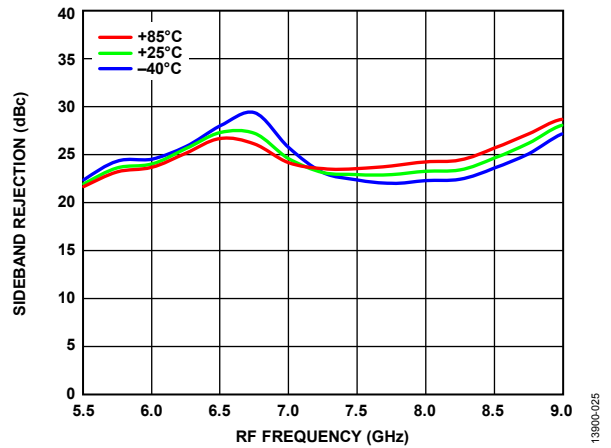


Figure 25. Sideband Rejection vs. RF Frequency over Temperatures, Voltage Control = -4 V

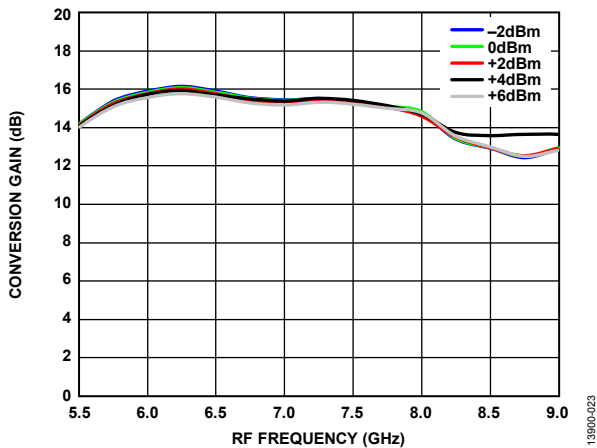


Figure 23. Conversion Gain vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V

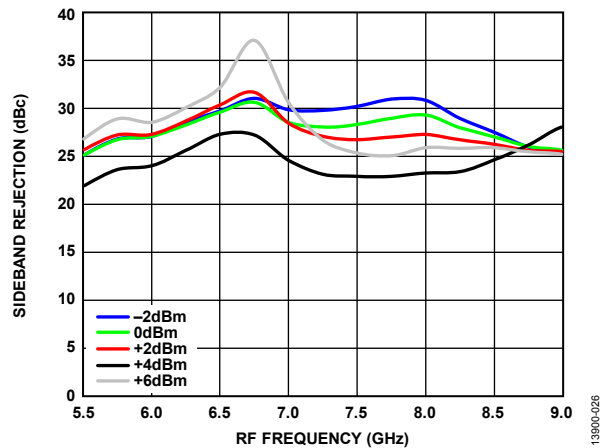


Figure 26. Sideband Rejection vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V

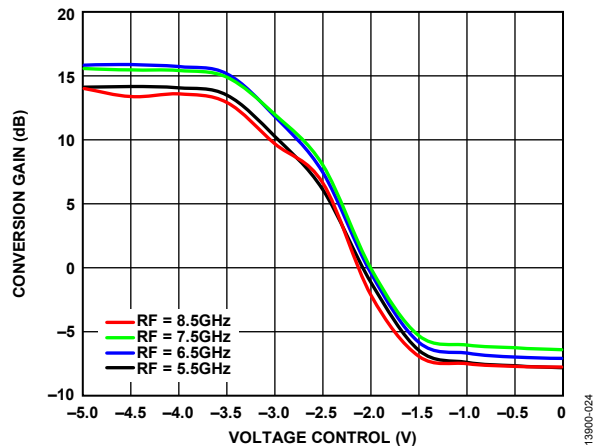


Figure 24. Conversion Gain vs. Voltage Control over RF, T<sub>A</sub> = 25°C, LO Power = 4 dBm

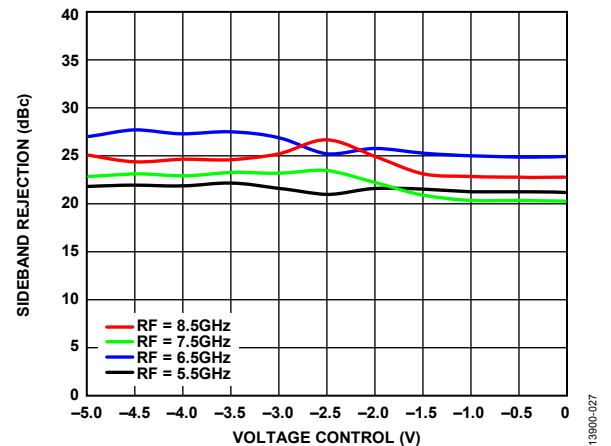


Figure 27. Sideband Rejection vs. Voltage Control over RF, T<sub>A</sub> = 25°C, LO Power = 4 dBm

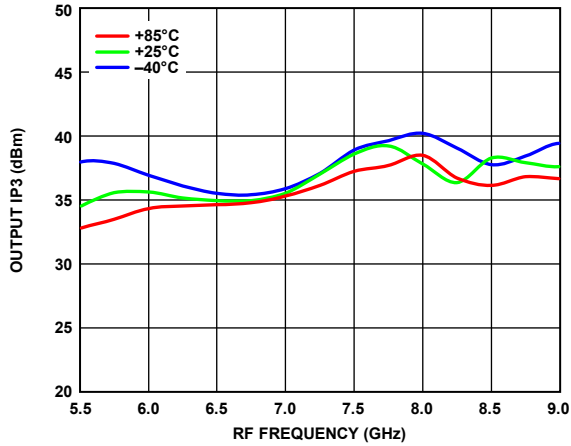


Figure 28. Output IP3 vs. RF Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V

13900-028

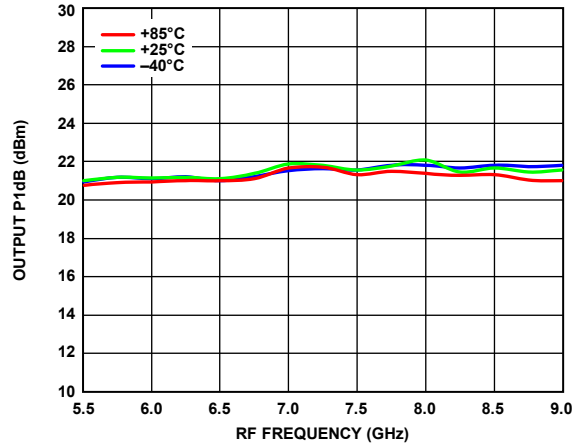


Figure 31. Output P1dB vs. RF Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V

13900-031

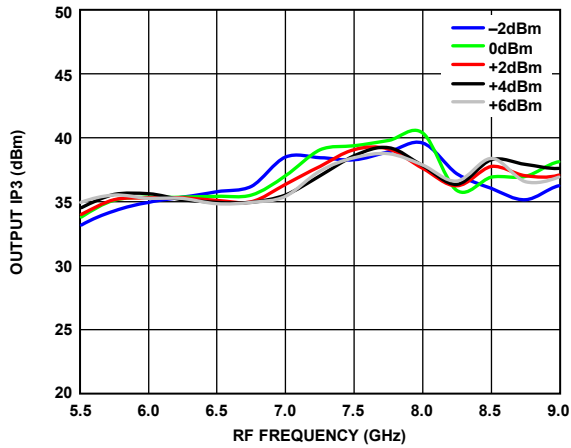


Figure 29. Output IP3 vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V

13900-029

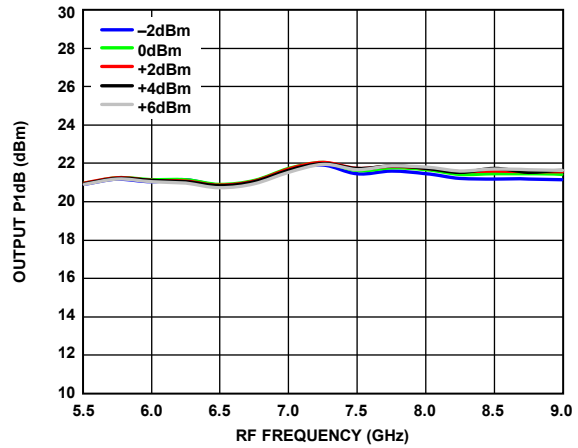


Figure 32. Output P1dB vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V

13900-032

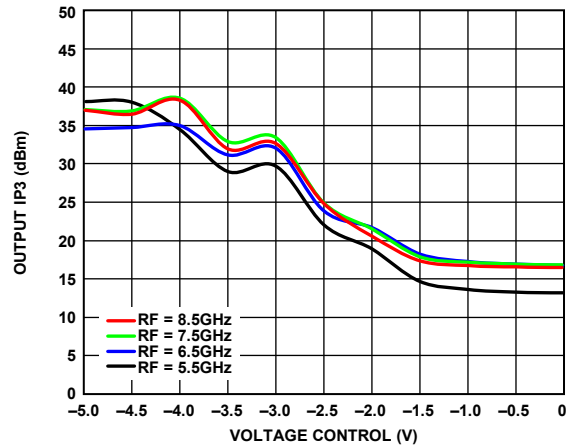


Figure 30. Output IP3 vs. Voltage Control over RF, T<sub>A</sub> = 25°C, LO Power = 4 dBm

13900-030

IF = 2500 MHz, IF INPUT POWER = -6 dBm, LOWER SIDEBAND (HIGH-SIDE LO)

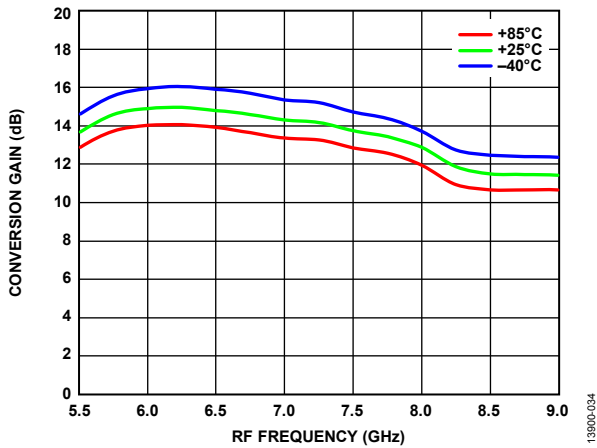


Figure 33. Conversion Gain vs. RF Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V

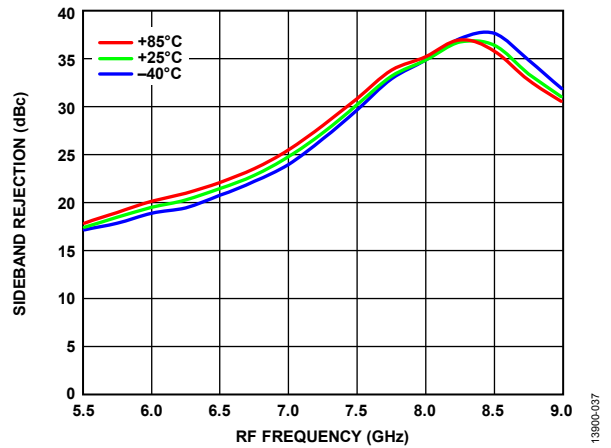


Figure 36. Sideband Rejection vs. RF Frequency over Temperatures, Voltage Control = -4 V

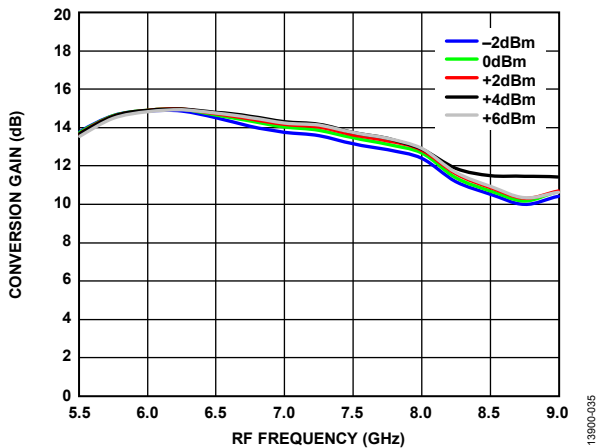


Figure 34. Conversion Gain vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V

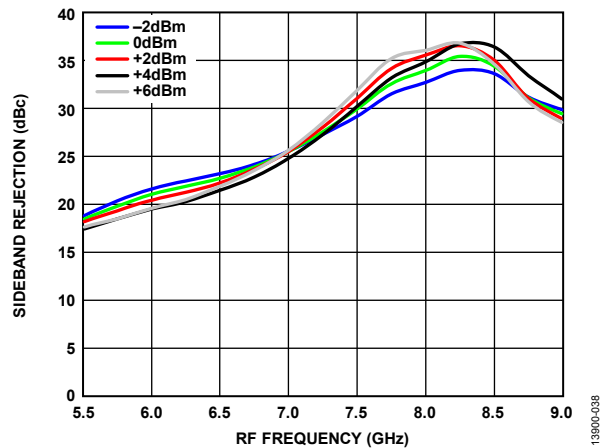


Figure 37. Sideband Rejection vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V

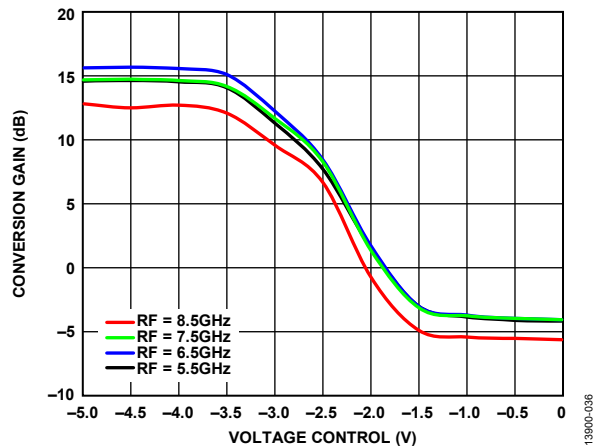


Figure 35. Conversion Gain vs. Voltage Control over RF, T<sub>A</sub> = 25°C, LO Power = 4 dBm

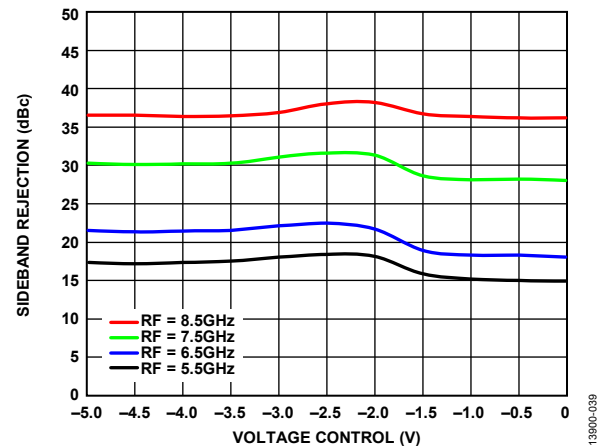
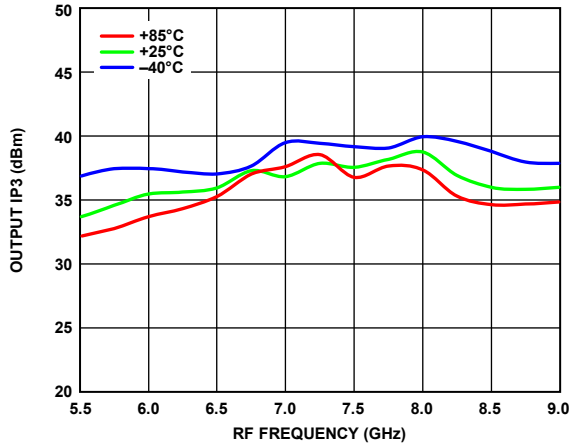
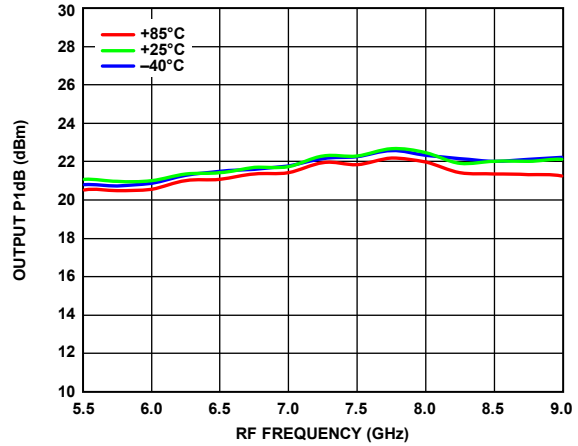


Figure 38. Sideband Rejection vs. Voltage Control over RF, T<sub>A</sub> = 25°C, LO Power = 4 dBm



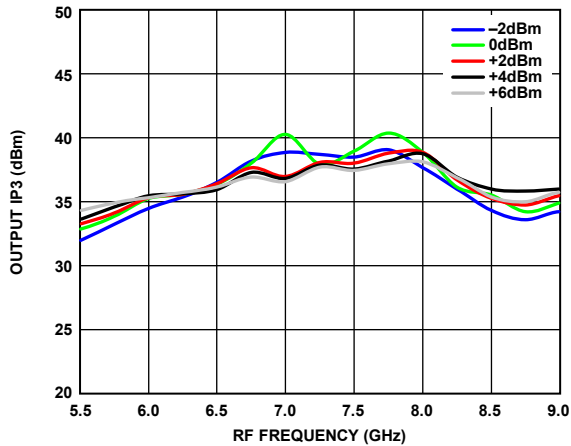
13900-040

Figure 39. Output IP3 vs. RF Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V



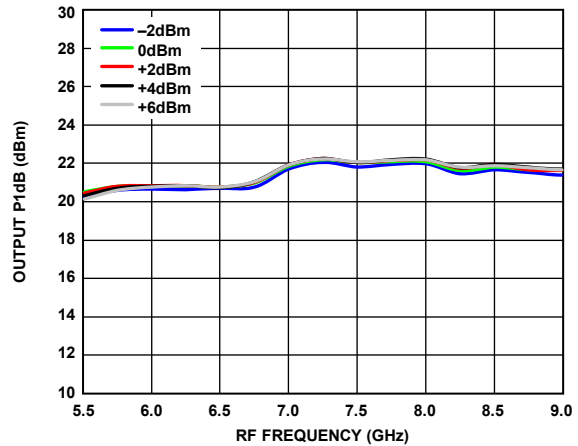
13900-043

Figure 42. Output P1dB vs. RF Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V



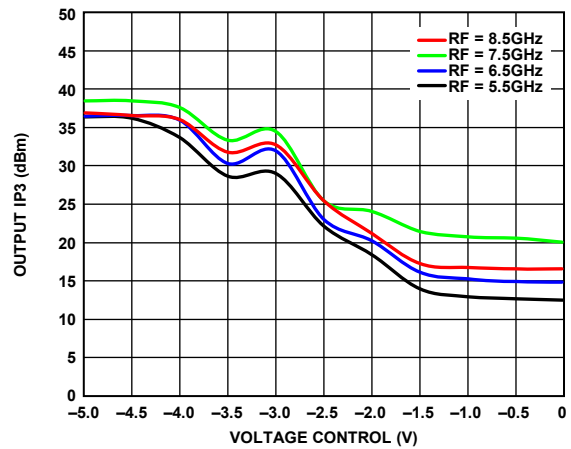
13900-041

Figure 40. Output IP3 vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V



13900-044

Figure 43. Output P1dB vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V



13900-042

Figure 41. Output IP3 vs. Voltage Control over RF, T<sub>A</sub> = 25°C, LO Power = 4 dBm

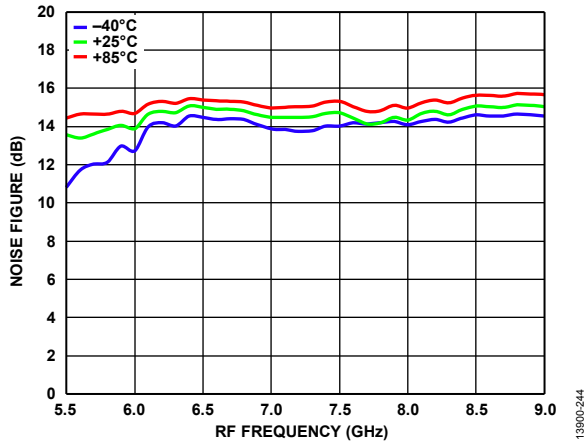


Figure 44. Noise Figure vs. RF Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V

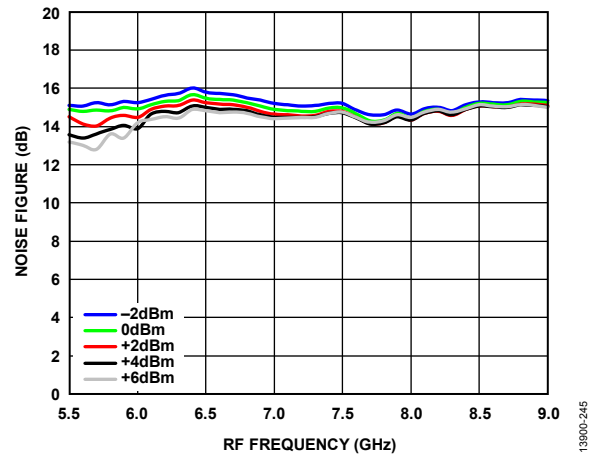
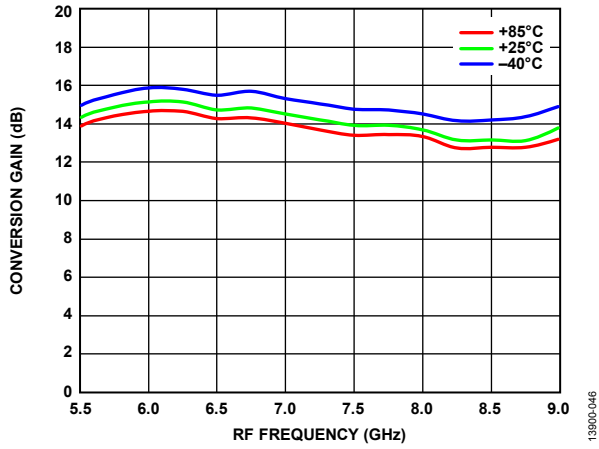


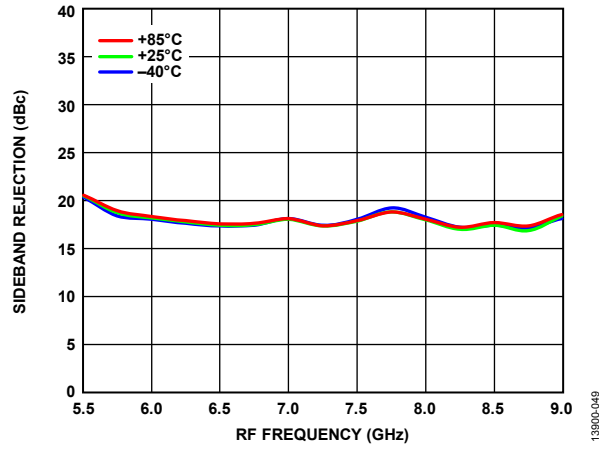
Figure 45. Noise Figure vs. RF Frequency over LO Powers  $T_A = 25^\circ\text{C}$ , Voltage Control = -4 V

IF = 350 MHz, IF INPUT POWER = -6 dBm, UPPER SIDEBAND (LOW-SIDE LO)



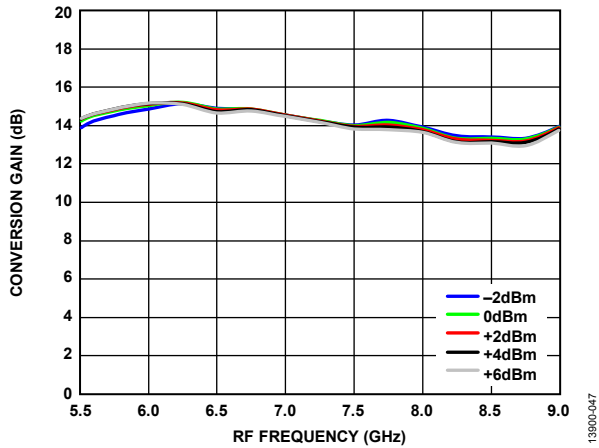
13900-046

Figure 46. Conversion Gain vs. RF Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V



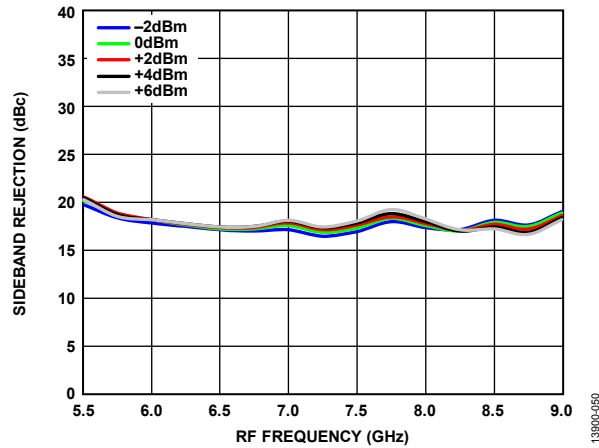
13900-049

Figure 49. Sideband Rejection vs. RF Frequency over Temperatures, Voltage Control = -4 V



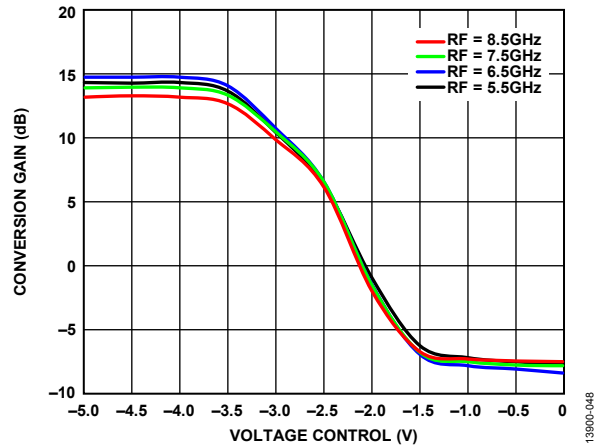
13900-047

Figure 47. Conversion Gain vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V



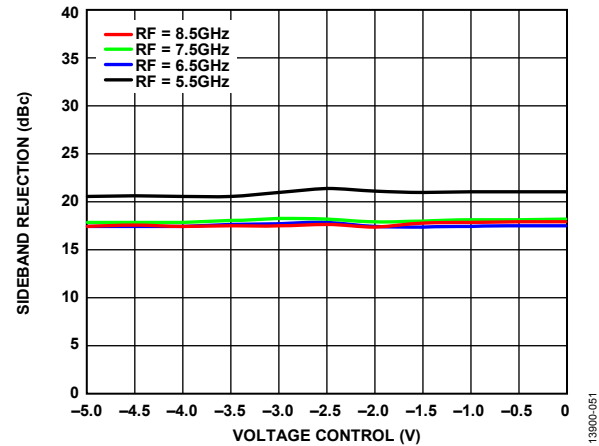
13900-050

Figure 50. Sideband Rejection vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V



13900-048

Figure 48. Conversion Gain vs. Voltage Control over RF, T<sub>A</sub> = 25°C, LO Power = 4 dBm



13900-051

Figure 51. Sideband Rejection vs. Voltage Control over RF, T<sub>A</sub> = 25°C, LO Power = 4 dBm

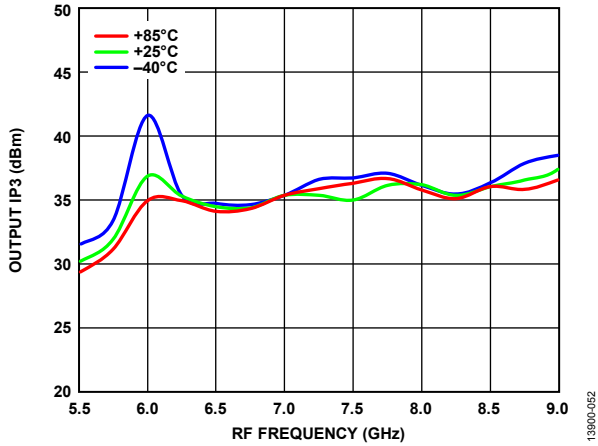


Figure 52. Output IP3 vs. RF Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V

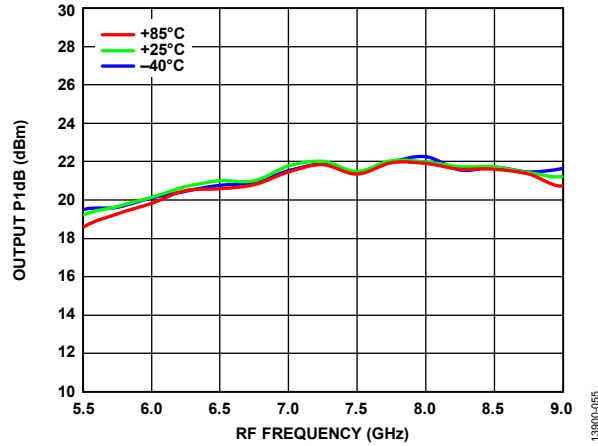


Figure 55. Output P1dB vs. RF Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V

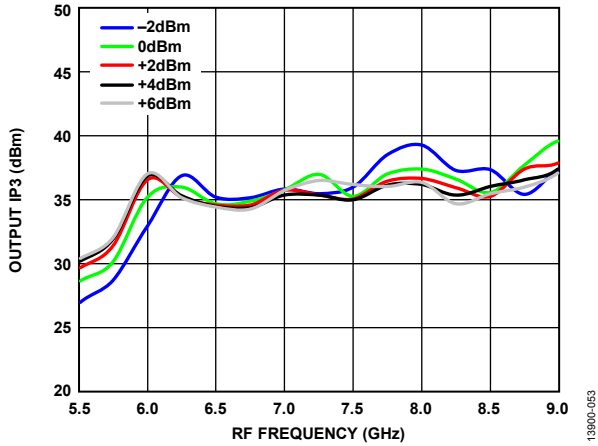


Figure 53. Output IP3 vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V

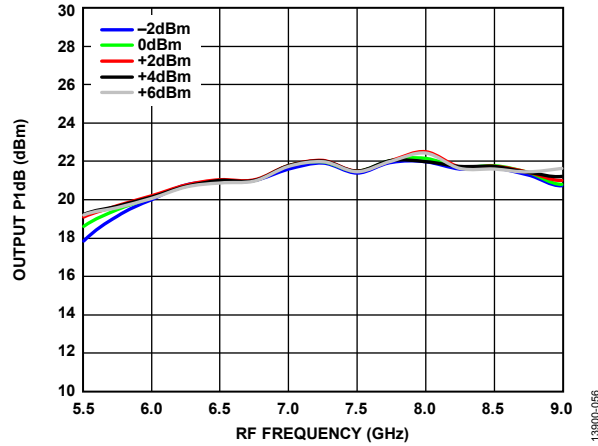


Figure 56. Output P1dB vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V

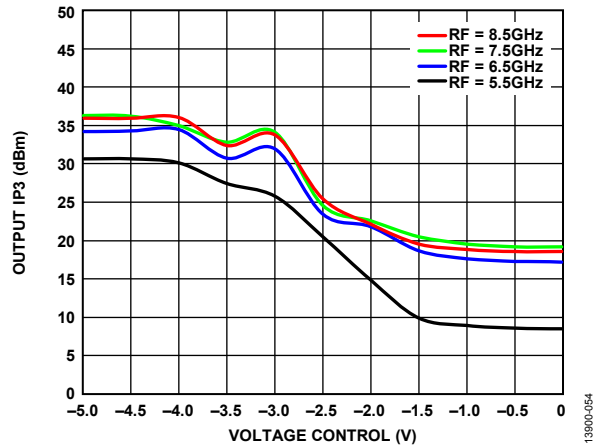


Figure 54. Output IP3 vs. Voltage Control over RF, T<sub>A</sub> = 25°C, LO Power = 4 dBm

13900-052

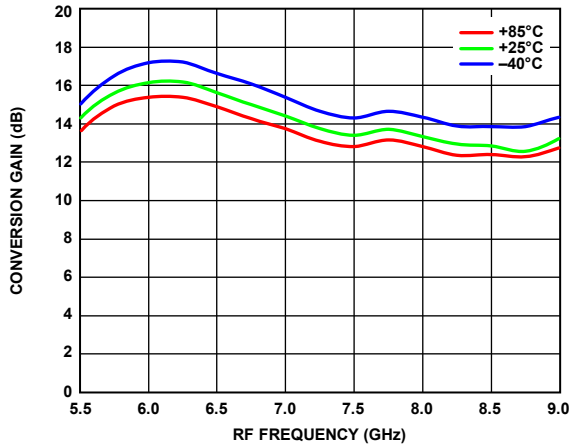
13900-055

13900-053

13900-056

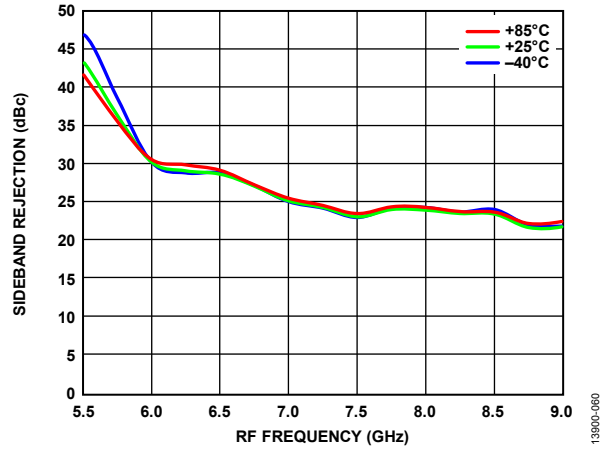
13900-054

IF = 1000 MHz, IF INPUT POWER = -6 dBm, UPPER SIDEBAND (LOW-SIDE LO)



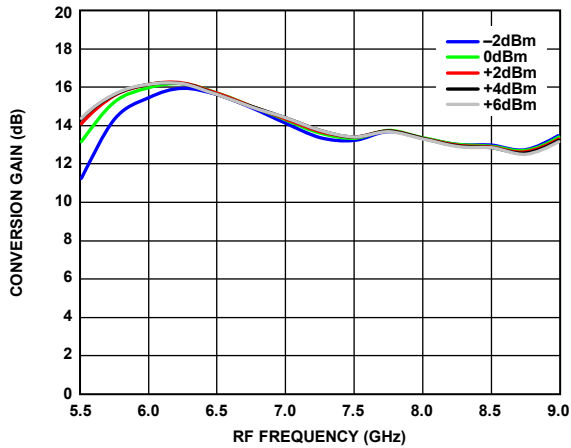
13900-057

Figure 57. Conversion Gain vs. RF Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V



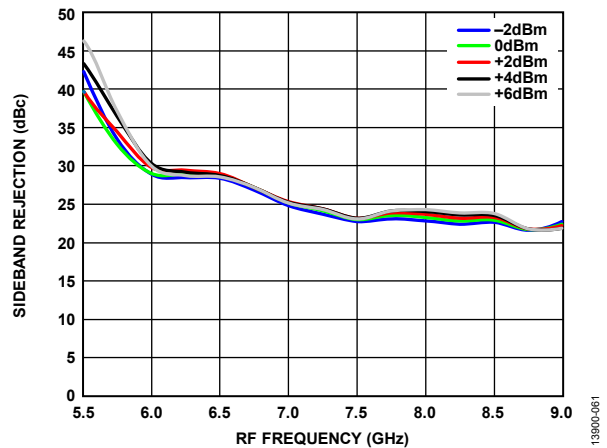
13900-060

Figure 60. Sideband Rejection vs. RF Frequency over Temperatures, Voltage Control = -4 V



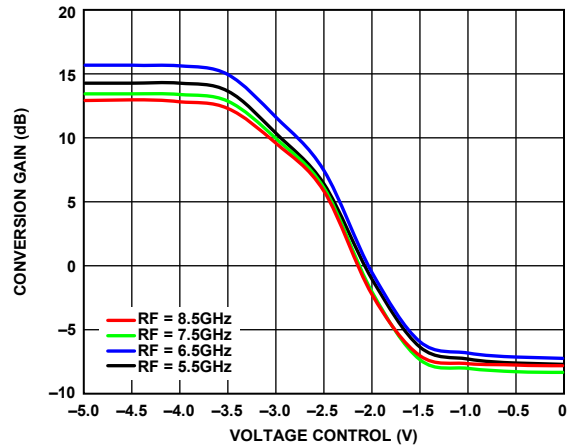
13900-058

Figure 58. Conversion Gain vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V



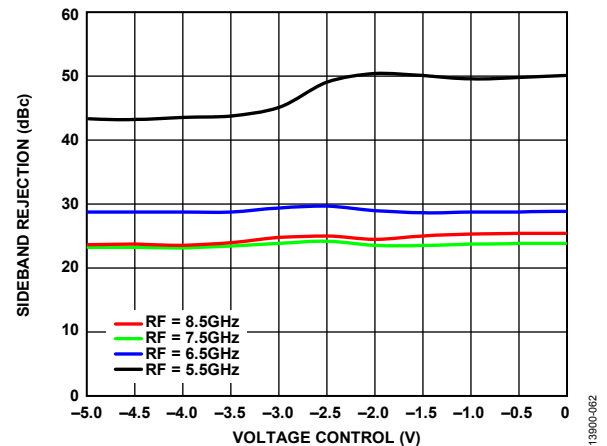
13900-061

Figure 61. Sideband Rejection vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V



13900-059

Figure 59. Conversion Gain vs. Voltage Control over RF, T<sub>A</sub> = 25°C, LO Power = 4 dBm



13900-062

Figure 62. Sideband Rejection vs. Voltage Control over RF, T<sub>A</sub> = 25°C, LO Power = 4 dBm



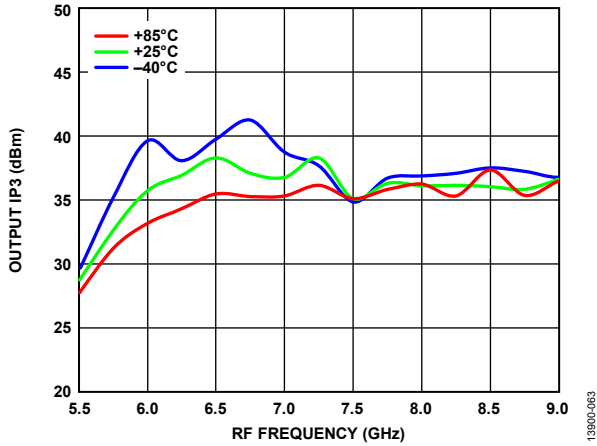


Figure 63. Output IP3 vs. RF Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V

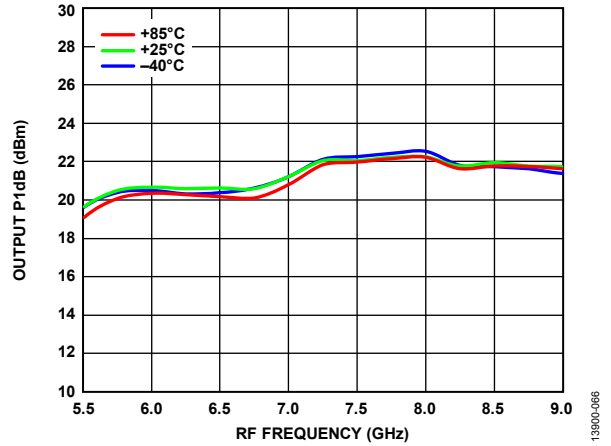


Figure 66. Output P1dB vs. RF Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V

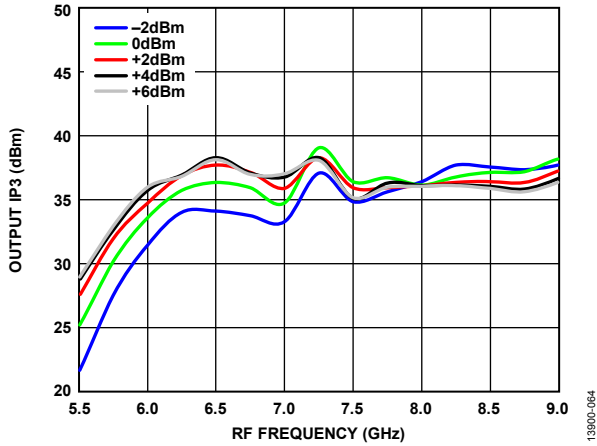


Figure 64. Output IP3 vs. RF Frequency over LO Powers,  $T_A = 25^\circ\text{C}$ , Voltage Control = -4 V

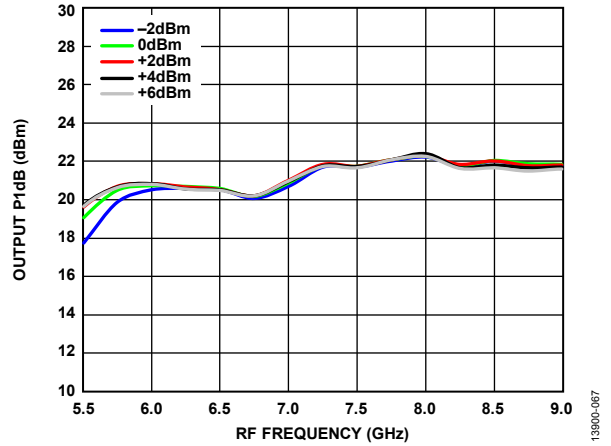


Figure 67. Output P1dB vs. RF Frequency over LO Powers,  $T_A = 25^\circ\text{C}$ , Voltage Control = -4 V

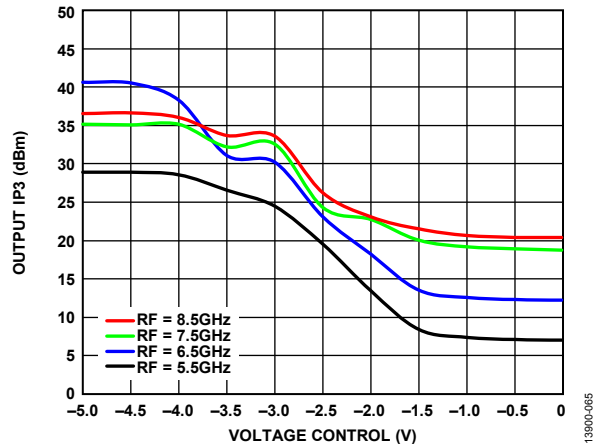


Figure 65. Output IP3 vs. Voltage Control over RF,  $T_A = 25^\circ\text{C}$ , LO Power = 4 dBm

13900-063

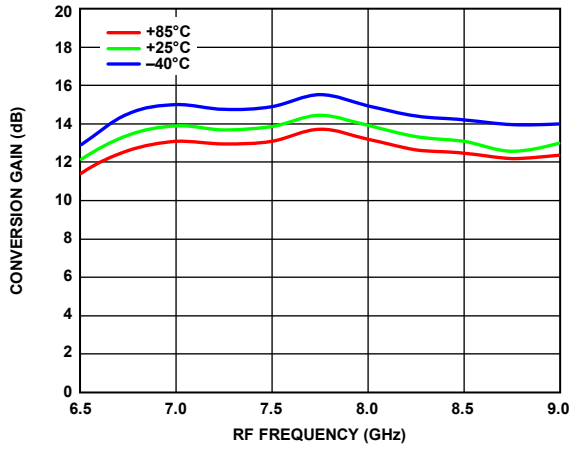
13900-066

13900-064

13900-067

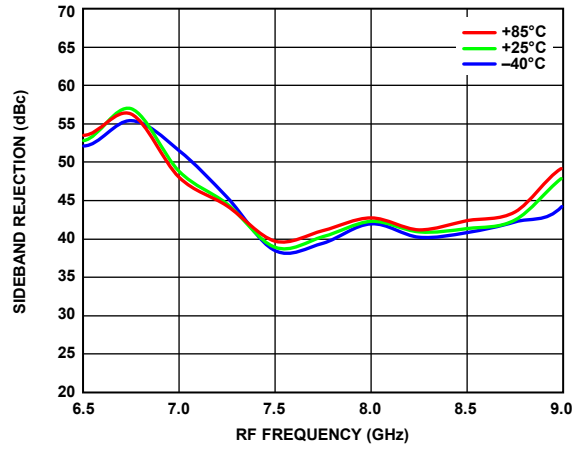
13900-065

IF = 2500 MHz, IF INPUT POWER = -6 dBm, UPPER SIDEBAND (LOW-SIDE LO)



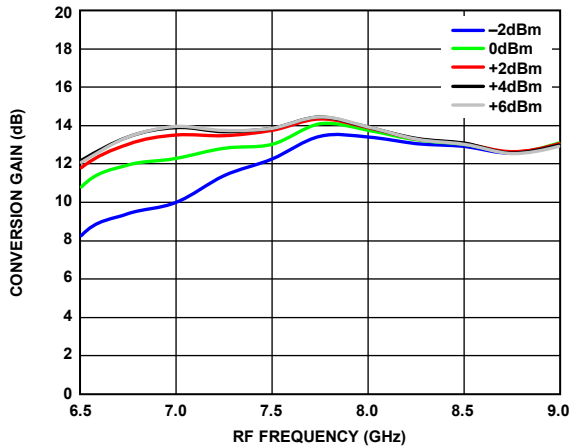
13900-068

Figure 68. Conversion Gain vs. RF Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V



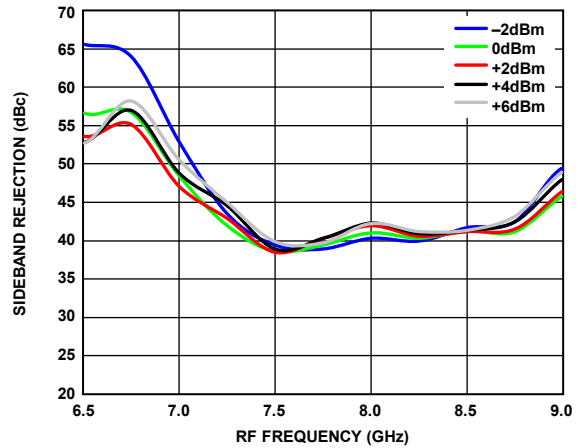
13900-071

Figure 71. Sideband Rejection vs. RF Frequency over Temperatures, Voltage Control = -4 V



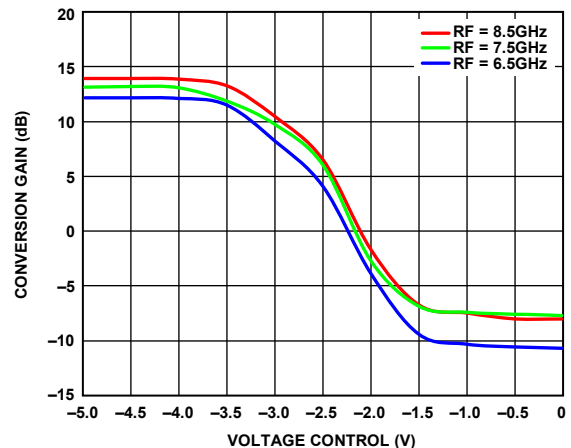
13900-069

Figure 69. Conversion Gain vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V



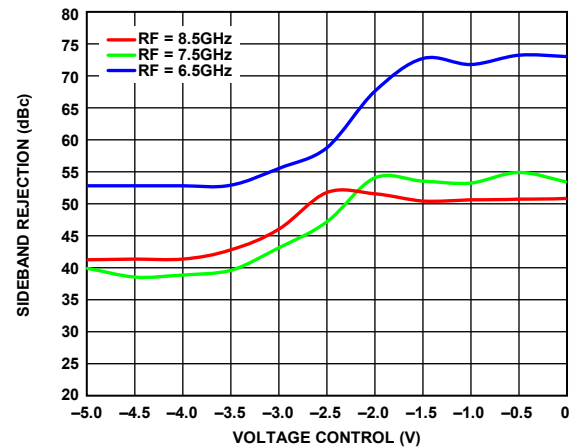
13900-072

Figure 72. Sideband Rejection vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V



13900-070

Figure 70. Conversion Gain vs. Voltage Control over RF, T<sub>A</sub> = 25°C, LO Power = 4 dBm



13900-073

Figure 73. Sideband Rejection vs. Voltage Control over RF, T<sub>A</sub> = 25°C, LO Power = 4 dBm

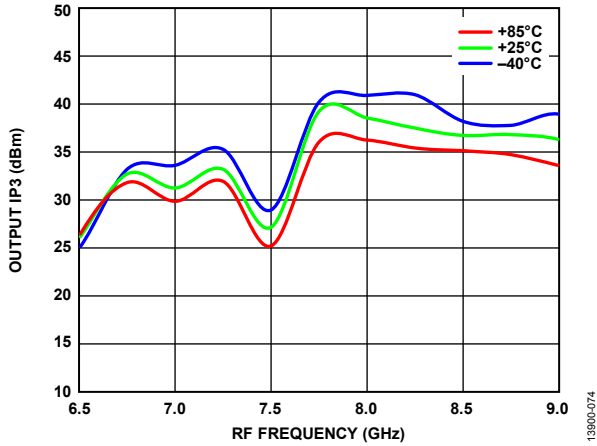


Figure 74. Output IP3 vs. RF Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V

13890-074

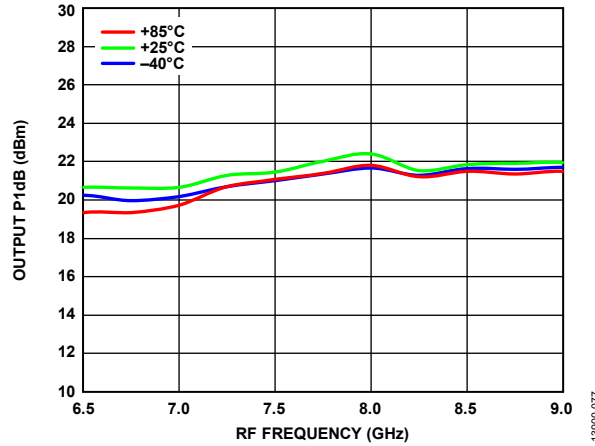


Figure 77. Output P1dB vs. RF Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V

13890-077

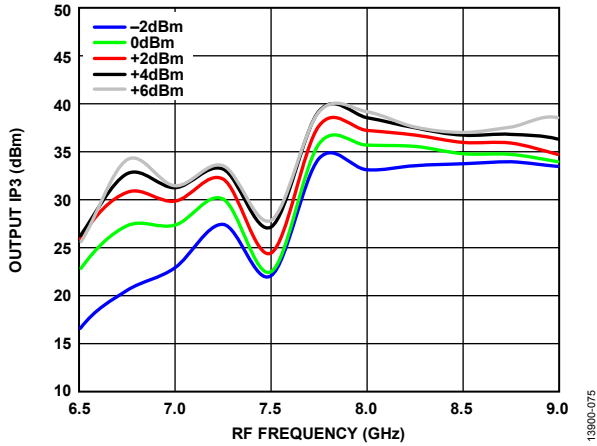


Figure 75. Output IP3 vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V

13890-075

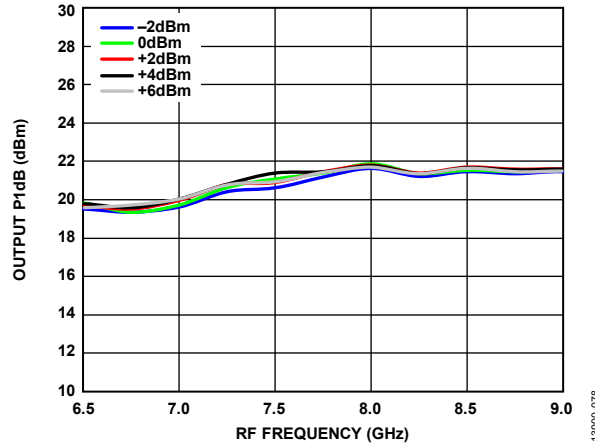


Figure 78. Output P1dB vs. RF Frequency over LO Powers, T<sub>A</sub> = 25°C, Voltage Control = -4 V

13890-078

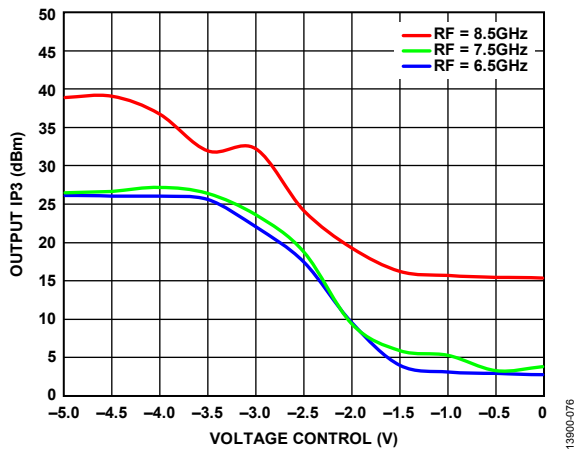


Figure 76. Output IP3 vs. Voltage Control over RF, T<sub>A</sub> = 25°C, LO Power = 4 dBm

13890-076

ISOLATION AND RETURN LOSS

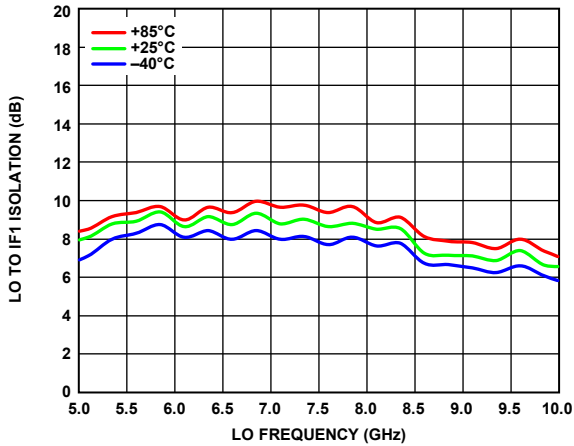


Figure 79. LO to IF1 Isolation vs. LO Frequency over Temperatures, IF = 350 MHz, LO Power = 4 dBm, Voltage Control = -4 V

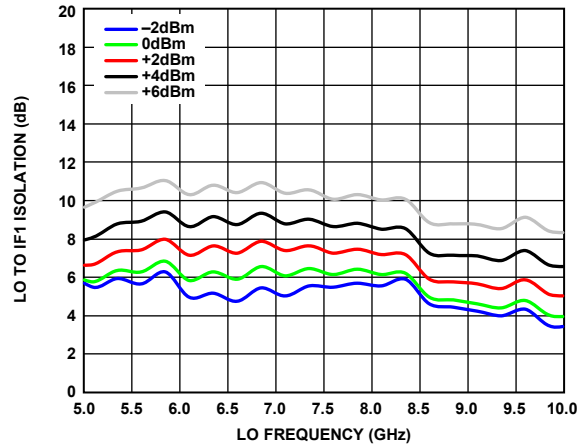


Figure 82. LO to IF1 Isolation vs. LO Frequency over LO Powers,  $T_A = 25^\circ\text{C}$ , Voltage Control = -4 V

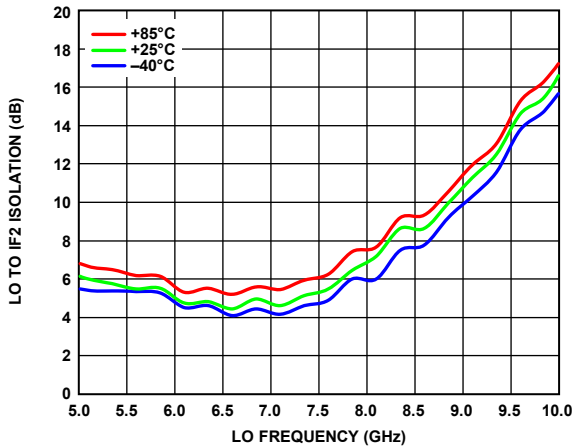


Figure 80. LO to IF2 Isolation vs. LO Frequency over Temperatures, IF = 350 MHz, LO Power = 4 dBm, Voltage Control = -4 V

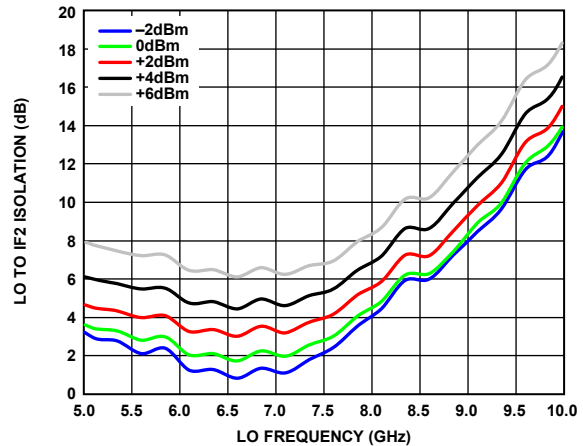


Figure 83. LO to IF2 Isolation vs. LO Frequency over LO Powers,  $T_A = 25^\circ\text{C}$ , Voltage Control = -4 V

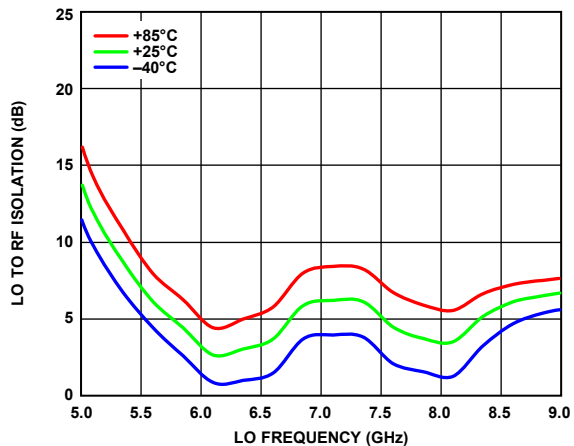


Figure 81. LO to RF Isolation vs. LO Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V

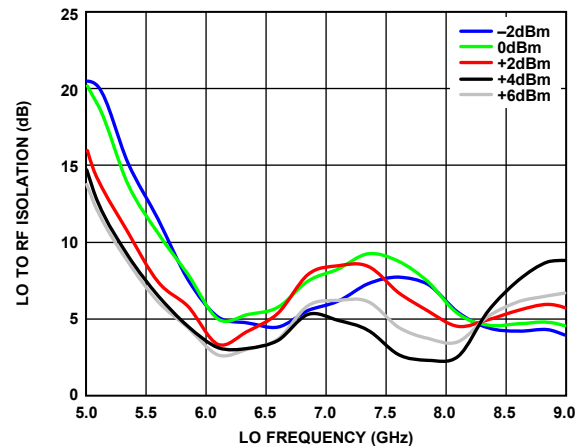


Figure 84. LO to RF Isolation vs. LO Frequency over LO Powers,  $T_A = 25^\circ\text{C}$ , Voltage Control = -4 V

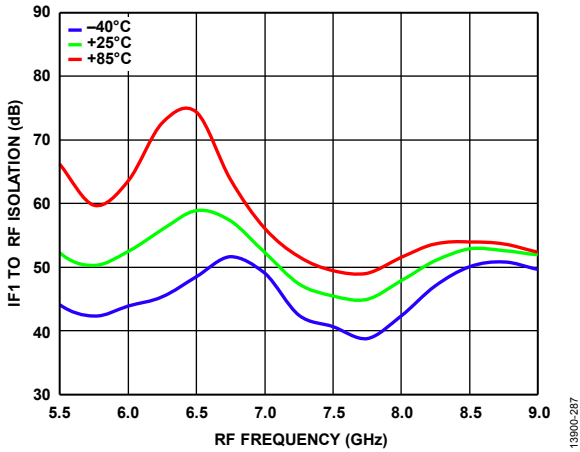


Figure 85. IF1 to RF Isolation vs. RF Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V

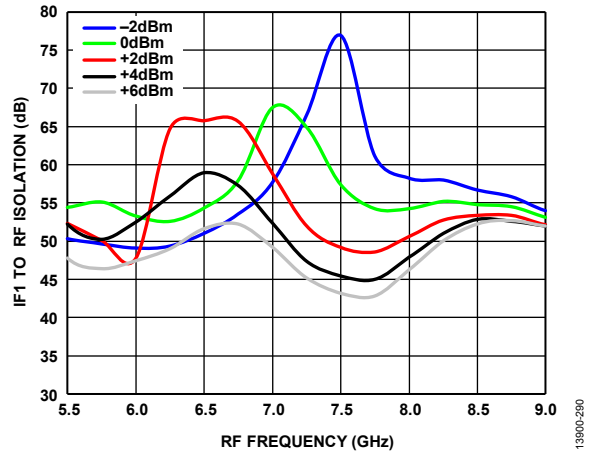


Figure 88. IF1 to RF Isolation vs. RF Frequency over LO Powers,  $T_A = 25^\circ\text{C}$ , Voltage Control = -4 V

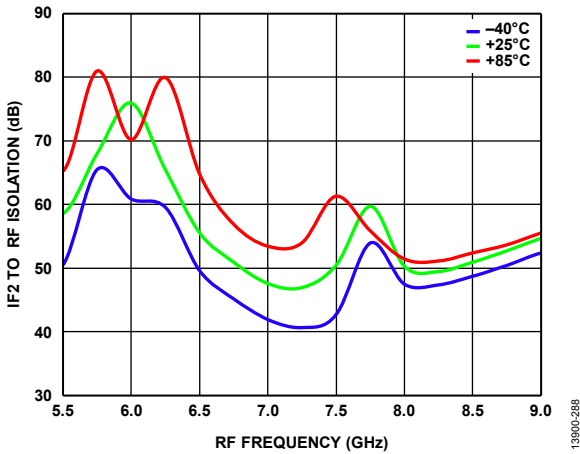


Figure 86. IF2 to RF Isolation vs. RF Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V

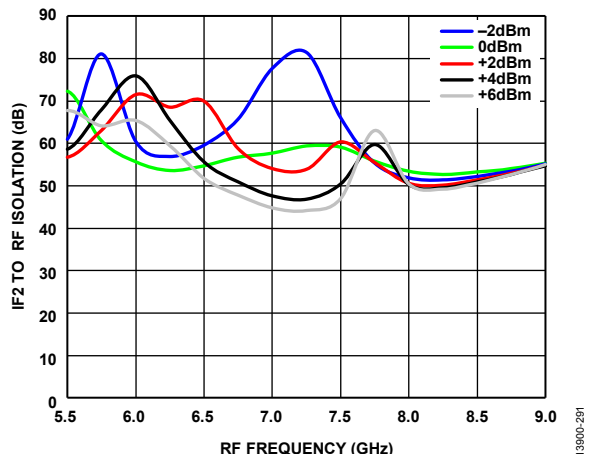


Figure 89. IF2 to RF Isolation vs. RF Frequency over LO Powers,  $T_A = 25^\circ\text{C}$ , Voltage Control = -4 V

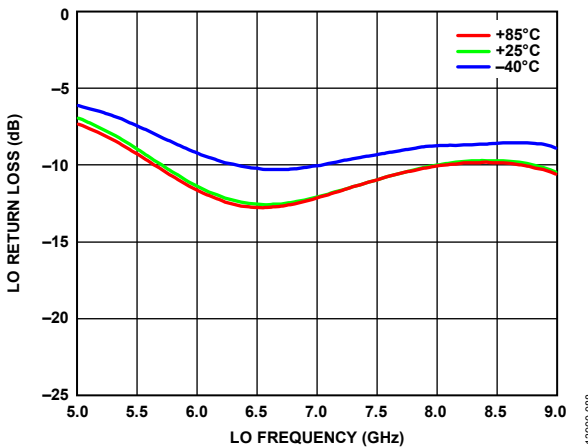


Figure 87. LO Return Loss vs. LO Frequency over Temperatures, LO Power = 4 dBm, Voltage Control = -4 V

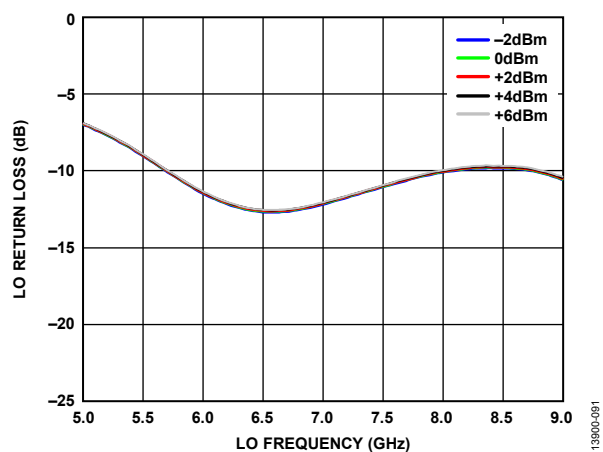
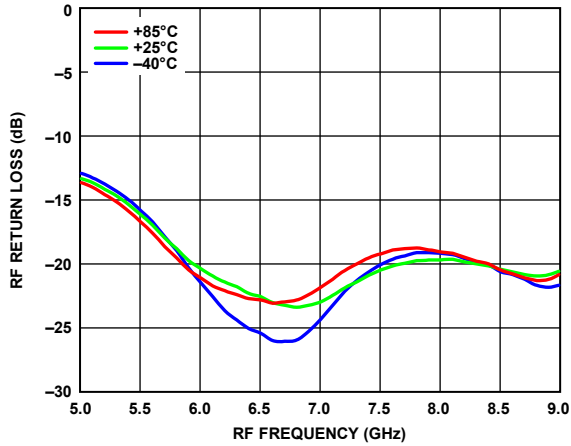
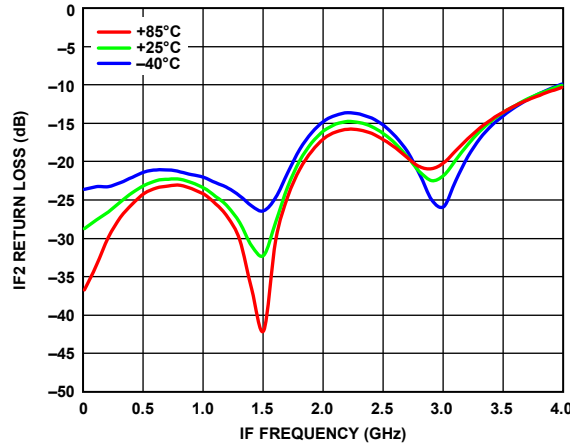


Figure 90. LO Return Loss vs. LO Frequency over LO Powers,  $T_A = 25^\circ\text{C}$ , Voltage Control = -4 V



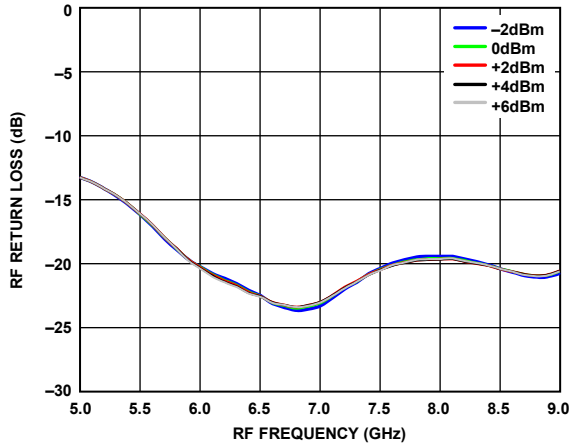
13900-089

Figure 91. RF Return Loss vs. RF Frequency over Temperatures, LO Frequency = 7 GHz, LO Power = 4 dBm, Voltage Control = -4 V



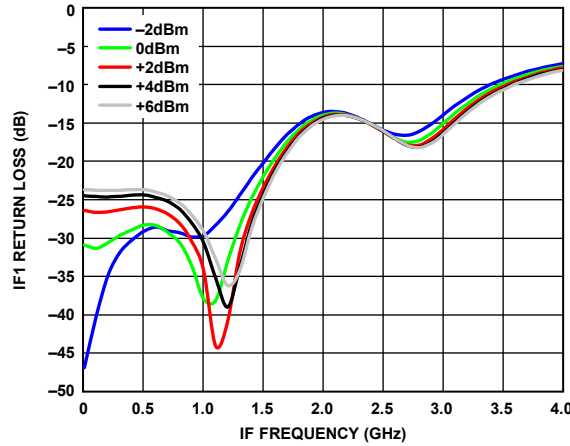
13900-084

Figure 94. IF2 Return Loss vs. IF Frequency over Temperatures, LO Frequency = 7 GHz, LO Power = 4 dBm, Voltage Control = -4 V



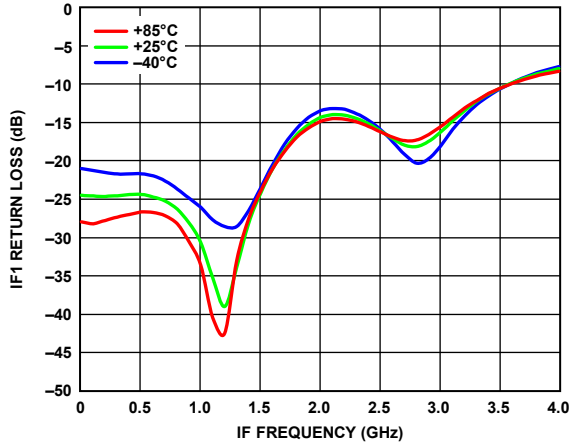
13900-092

Figure 92. RF Return Loss vs. RF Frequency over LO Powers, LO Frequency = 7 GHz, T<sub>A</sub> = 25°C, Voltage Control = -4 V



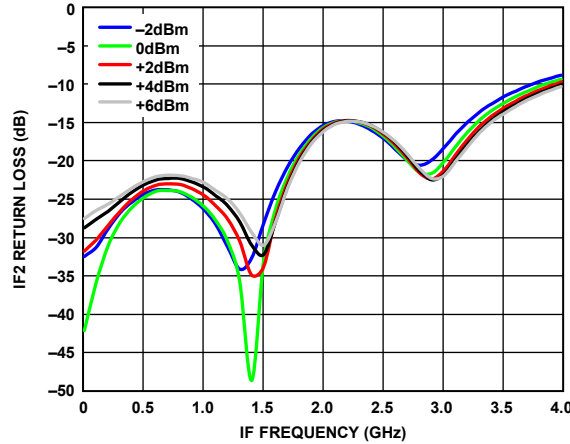
13900-095

Figure 95. IF1 Return Loss vs. IF Frequency over LO Powers, LO Frequency = 7 GHz, T<sub>A</sub> = 25°C, Voltage Control = -4 V



13900-093

Figure 93. IF1 Return Loss vs. IF Frequency over Temperatures, LO Frequency = 7 GHz, LO Power = 4 dBm, Voltage Control = -4 V



13900-096

Figure 96. IF2 Return Loss vs. IF Frequency over LO Powers, LO Frequency = 7 GHz, T<sub>A</sub> = 25°C, Voltage Control = -4 V

**IF BANDWIDTH PERFORMANCE: LOWER SIDEBAND (HIGH-SIDE LO)**

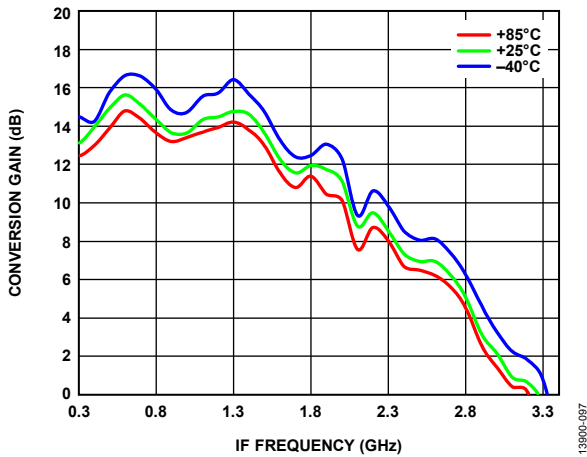


Figure 97. Conversion Gain vs. IF Frequency over Temperatures, LO Frequency = 7 GHz, LO Power = 4 dBm, Voltage Control = -4 V

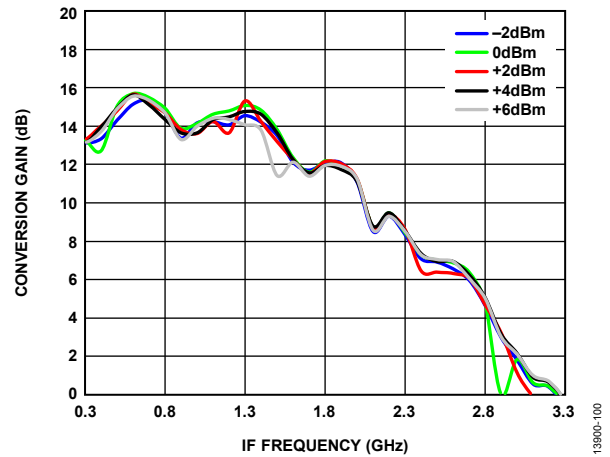


Figure 100. Conversion Gain vs. IF Frequency over LO Powers, LO Frequency = 7 GHz,  $T_A = 25^\circ\text{C}$ , Voltage Control = -4 V

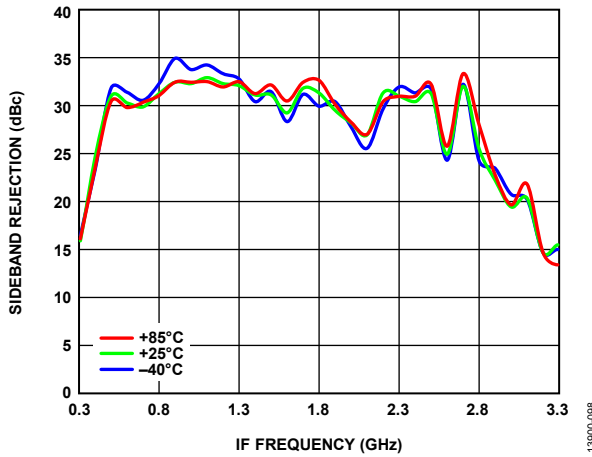


Figure 98. Sideband Rejection vs. IF Frequency over Temperatures, LO Frequency = 7 GHz, LO Power = 4 dBm, Voltage Control = -4 V

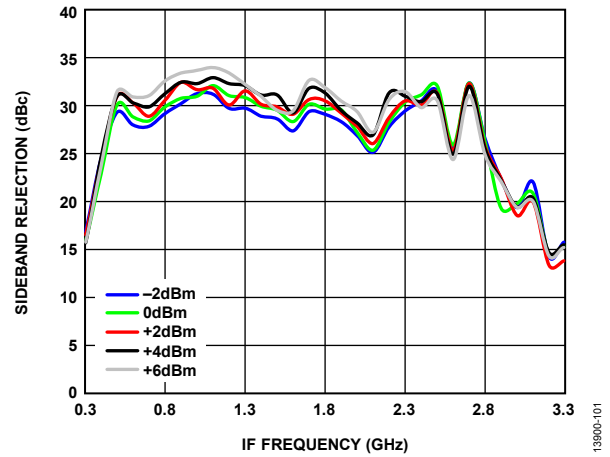


Figure 101. Sideband Rejection vs. IF Frequency over LO Powers, LO Frequency = 7 GHz,  $T_A = 25^\circ\text{C}$ , Voltage Control = -4 V

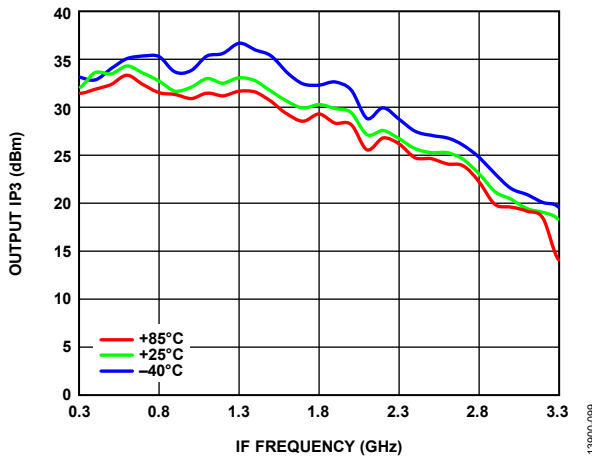


Figure 99. Output IP3 vs. IF Frequency over Temperatures, LO Frequency = 7 GHz, LO Power = 4 dBm, Voltage Control = -4 V

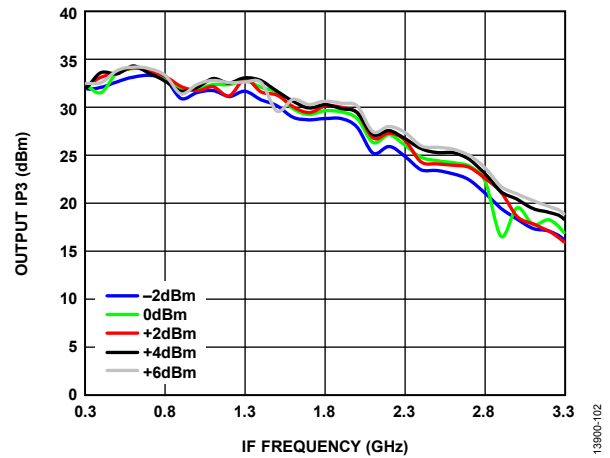


Figure 102. Output IP3 vs. IF Frequency over LO Powers, LO Frequency = 7 GHz,  $T_A = 25^\circ\text{C}$ , Voltage Control = -4 V

**SPURIOUS PERFORMANCE**

Mixer spurious products are measured in dBc from the RF output power level. Spur values are  $(M \times IF) - (N \times LO)$ . N/A means not applicable.

**$M \times N$  Spurious Outputs,  $IF = 350$  MHz**

RF = 5500 MHz, LO frequency = 5850 MHz at LO input power = 4 dBm, IF input power = -6 dBm.

|        |   | N x LO |     |     |    |     |     |
|--------|---|--------|-----|-----|----|-----|-----|
|        |   | 0      | 1   | 2   | 3  | 4   | 5   |
| M x IF | 0 | N/A    | 11  | 3   | 18 | 41  | 53  |
|        | 1 | 75     | 0   | 38  | 36 | 50  | 62  |
|        | 2 | 79     | 51  | 34  | 61 | 60  | 81  |
|        | 3 | 100    | 73  | 78  | 60 | 87  | 81  |
|        | 4 | 101    | 88  | 80  | 94 | 86  | 111 |
|        | 5 | 121    | 102 | 108 | 98 | 111 | 101 |

RF = 7000 MHz, LO frequency = 7350 MHz at LO input power = 4 dBm, IF input power = -6 dBm.

|        |   | N x LO |    |     |     |     |     |
|--------|---|--------|----|-----|-----|-----|-----|
|        |   | 0      | 1  | 2   | 3   | 4   | 5   |
| M x IF | 0 | N/A    | 13 | 8   | 44  | 51  | 57  |
|        | 1 | 79     | 0  | 43  | 39  | 73  | 75  |
|        | 2 | 78     | 51 | 34  | 73  | 67  | 94  |
|        | 3 | 105    | 72 | 86  | 65  | 98  | 87  |
|        | 4 | 118    | 82 | 96  | 105 | 93  | 103 |
|        | 5 | 122    | 91 | 107 | 111 | 108 | 105 |

RF = 8500 MHz, LO frequency = 8850 MHz at LO input power = 4 dBm, IF input power = -6 dBm. N/A is not applicable.

|        |   | N x LO |    |     |     |     |     |
|--------|---|--------|----|-----|-----|-----|-----|
|        |   | 0      | 1  | 2   | 3   | 4   | 5   |
| M x IF | 0 | N/A    | 8  | 21  | 53  | 53  | N/A |
|        | 1 | 76     | 0  | 27  | 56  | 68  | N/A |
|        | 2 | 81     | 50 | 36  | 61  | 83  | N/A |
|        | 3 | 104    | 95 | 79  | 71  | 92  | N/A |
|        | 4 | 114    | 83 | 101 | 105 | 99  | N/A |
|        | 5 | 120    | 92 | 111 | 108 | 103 | N/A |

**$M \times N$  Spurious Output,  $IF = 1000$  MHz**

RF = 5500 MHz, LO frequency = 6500 MHz at LO input power = 4 dBm, IF input power = -6 dBm.

|        |   | N x LO |     |     |     |     |     |
|--------|---|--------|-----|-----|-----|-----|-----|
|        |   | 0      | 1   | 2   | 3   | 4   | 5   |
| M x IF | 0 | N/A    | 7   | 8   | 57  | 43  | 59  |
|        | 1 | 49     | 0   | 37  | 39  | 66  | 72  |
|        | 2 | 63     | 55  | 33  | 60  | 66  | 90  |
|        | 3 | 83     | 82  | 69  | 65  | 84  | 90  |
|        | 4 | 95     | 120 | 100 | 97  | 91  | 104 |
|        | 5 | 112    | 121 | 109 | 113 | 108 | 108 |

RF = 7000 MHz, LO frequency = 8000 MHz at LO input power = 4 dBm, IF input power = -6 dBm.

|        |   | N x LO |    |    |     |     |     |
|--------|---|--------|----|----|-----|-----|-----|
|        |   | 0      | 1  | 2  | 3   | 4   | 5   |
| M x IF | 0 | N/A    | 7  | 11 | 43  | 59  | 71  |
|        | 1 | 50     | 0  | 40 | 43  | 74  | 79  |
|        | 2 | 66     | 44 | 35 | 68  | 73  | 91  |
|        | 3 | 88     | 85 | 71 | 67  | 98  | 92  |
|        | 4 | 80     | 80 | 81 | 100 | 96  | 104 |
|        | 5 | 85     | 88 | 79 | 101 | 113 | 107 |

RF = 8500 MHz, LO frequency = 9500 MHz at LO input power = 4 dBm, IF input power = -6 dBm. N/A is not applicable.

|        |   | N x LO |     |     |     |     |     |
|--------|---|--------|-----|-----|-----|-----|-----|
|        |   | 0      | 1   | 2   | 3   | 4   | 5   |
| M x IF | 0 | N/A    | 8   | 41  | 63  | 66  | N/A |
|        | 1 | 50     | 0   | 31  | 77  | 88  | N/A |
|        | 2 | 66     | 44  | 38  | 63  | 81  | N/A |
|        | 3 | 101    | 82  | 74  | 72  | 93  | N/A |
|        | 4 | 105    | 105 | 108 | 107 | 102 | N/A |
|        | 5 | 120    | 118 | 112 | 109 | 107 | N/A |



**M × N Spurious Outputs, IF = 2500 MHz**

RF = 5500 MHz, LO frequency = 8000 MHz at LO input power = 4 dBm, IF input power = -6 dBm.

|        |   | N × LO |     |     |     |     |     |
|--------|---|--------|-----|-----|-----|-----|-----|
|        |   | 0      | 1   | 2   | 3   | 4   | 5   |
| M × IF | 0 | N/A    | 6   | 10  | 41  | 57  | 70  |
|        | 1 | 43     | 0   | 34  | 42  | 70  | 79  |
|        | 2 | 57     | 64  | 34  | 64  | 78  | 93  |
|        | 3 | 76     | 113 | 80  | 65  | 87  | 92  |
|        | 4 | 97     | 115 | 94  | 96  | 94  | 107 |
|        | 5 | 116    | 115 | 119 | 112 | 110 | 113 |

RF = 8500 MHz, LO frequency = 11000 MHz at LO input power = 4 dBm, IF input power = -6 dBm. N/A is not applicable.

|        |   | N × LO |     |     |     |     |     |
|--------|---|--------|-----|-----|-----|-----|-----|
|        |   | 0      | 1   | 2   | 3   | 4   | 5   |
| M × IF | 0 | N/A    | 7   | 59  | 46  | N/A | N/A |
|        | 1 | 47     | 0   | 39  | 80  | N/A | N/A |
|        | 2 | 50     | 54  | 40  | 73  | 97  | N/A |
|        | 3 | 92     | 83  | 83  | 77  | 98  | N/A |
|        | 4 | 109    | 120 | 105 | 108 | 104 | N/A |
|        | 5 | 113    | 120 | 115 | 109 | 104 | N/A |

RF = 7000 MHz, LO frequency = 9500 MHz at LO input power = 4 dBm, IF input power = -6 dBm. N/A is not applicable.

|        |   | N × LO |     |     |     |     |     |
|--------|---|--------|-----|-----|-----|-----|-----|
|        |   | 0      | 1   | 2   | 3   | 4   | 5   |
| M × IF | 0 | N/A    | 7   | 41  | 62  | 67  | N/A |
|        | 1 | 46     | 0   | 36  | 73  | 84  | N/A |
|        | 2 | 57     | 56  | 37  | 63  | 103 | N/A |
|        | 3 | 108    | 87  | 83  | 69  | 104 | 101 |
|        | 4 | 100    | 122 | 101 | 112 | 101 | 101 |
|        | 5 | 115    | 121 | 118 | 112 | 111 | 106 |

## THEORY OF OPERATION

The HMC6505A is a GaAs, pHEMT, MMIC I/Q upconverter with an integrated LO buffer that upconverts IF between dc to 3 GHz to RF between 5.5 GHz and 8.6 GHz. LO buffer amplifiers are included on chip to allow LO drive range of up to 6 dBm for full performance. The LO path feeds a quadrature splitter followed by on-chip baluns that drive the I and Q singly balanced cores of the passive mixers. The RF output of the I and

Q mixers are then summed through an on-chip Wilkinson power combiner and relatively matched to provide a single-ended, 50  $\Omega$  output signal that is amplified by the RF amplifiers to produce a dc-coupled and 50  $\Omega$  matched RF output signal at the RFOUT port. A voltage attenuator precedes the RF amplifiers for desired gain control.

# APPLICATIONS INFORMATION

## TYPICAL APPLICATION CIRCUIT

Figure 103 shows the typical application circuit for the HMC6505A. To select the appropriate sideband, an external 90° hybrid is required. For applications not requiring operation to dc, use an off chip dc blocking capacitor. For applications that require the LO signal at the output to be suppressed, use a bias tee or RF feed. Ensure that the source or sink current used for LO suppression is <3 mA for each IF port to prevent damage to the device. The common-mode voltage for each IF port is 0 V.

To select the upper sideband, connect the IF1 pin to the 90° port of the hybrid and the IF2 pin to the 0° port of the hybrid. To select the lower sideband, connect the IF1 pin to the 0° port of the hybrid and the IF2 pin to the 90° port of the hybrid.

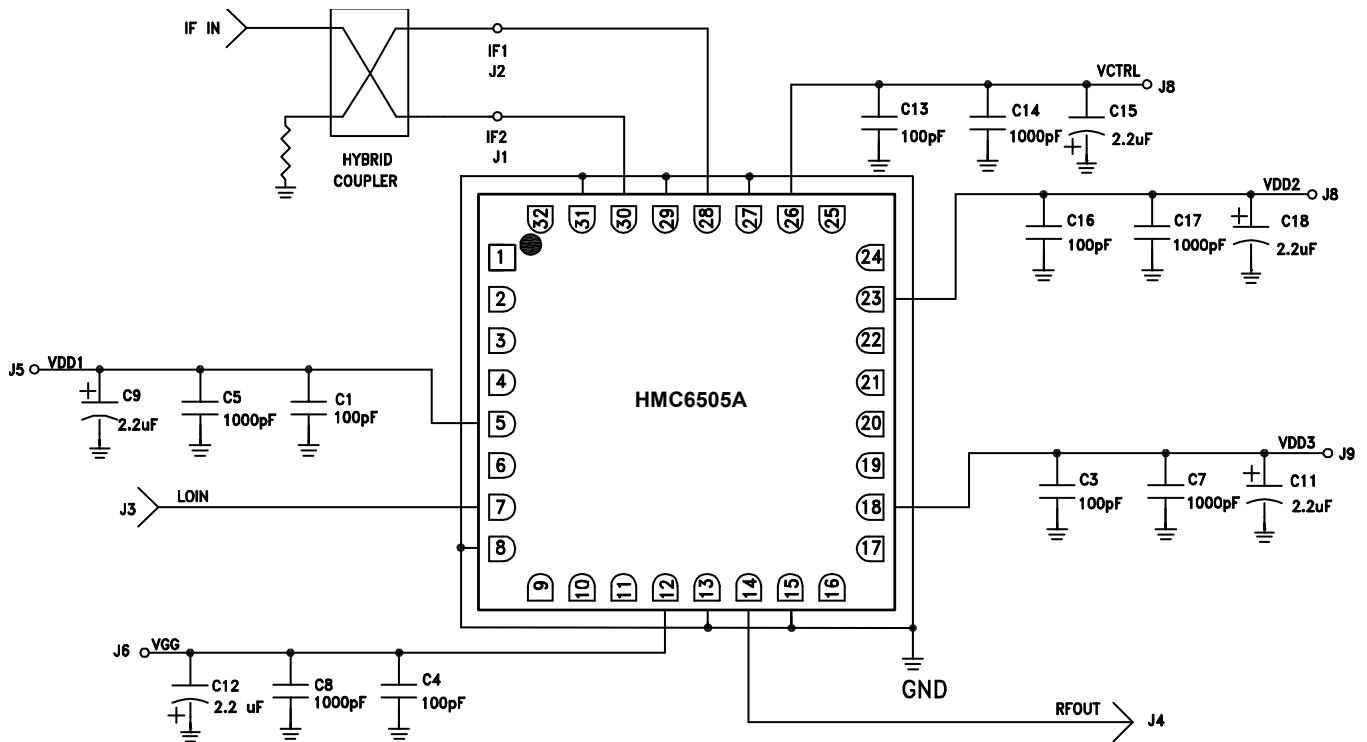


Figure 103. Typical Application Circuit

13890-103

**EVALUATION BOARD INFORMATION**

The circuit board used in the application must use RF circuit design techniques. Signal lines must have 50 Ω impedance and connect the package ground leads and exposed pad directly to the ground plane similarly to that shown in Figure 104. Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation board shown in Figure 106 is available from Analog Devices upon request.

**EV1HMC6505ALC5 Power-On Sequence**

To set up the EV1HMC6505ALC5, take the following steps:

1. Power up VGG with a -2 V supply.
2. Power up VDD1 with a 5 V supply.
3. Power up VDD2 and VDD3 with another 5 V supply.
4. Power up VCTRL with a -4 V supply (for maximum conversion gain).
5. Adjust the VGG supply between -2 V to 0 V until the total RF supply current (IDD2 + IDD3) = 120 mA.
6. Connect LOIN to the LO signal generator with an LO power of 4 dBm.
7. Apply the IF1 and IF2 signals.

**EV1HMC6505ALC5 Power Off Sequence**

To turn off the EV1HMC6505ALC5, take the following steps:

1. Turn off the LO and IF signals.
2. Set VGG to -2 V.
3. Set VCTRL to 0 V.
4. Set the VDD1, VDD2, and VDD3 supplies to 0 V and then turn them off.
5. Turn off the VGG supply.

**Layout**

Solder the exposed pad on the underside of the HMC6505A to a low thermal and electrical impedance ground plane. This pad is typically soldered to an exposed opening in the solder mask on the evaluation board. Connect these ground vias to all other ground layers on the evaluation board to maximize heat dissipation from the device package. Figure 104 and Figure 105 show the printed circuit board land pattern footprint for the HMC6505A and the solder paste stencil for the HMC6505A evaluation board.

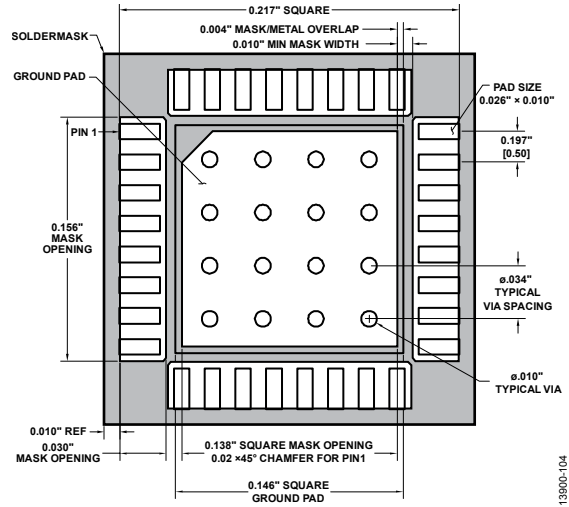


Figure 104. Printed Circuit Board Land Pattern Footprint

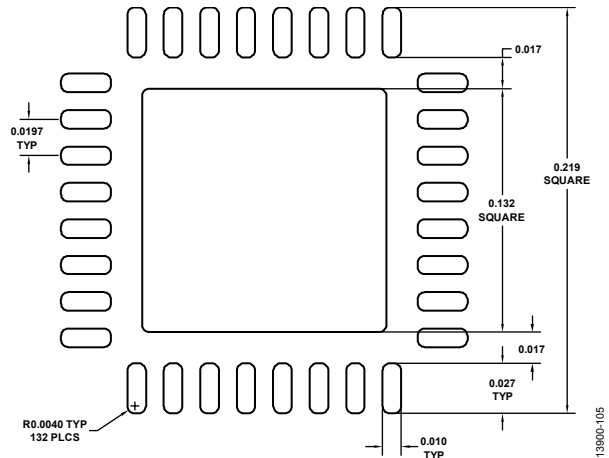


Figure 105. Solder Paste Stencil

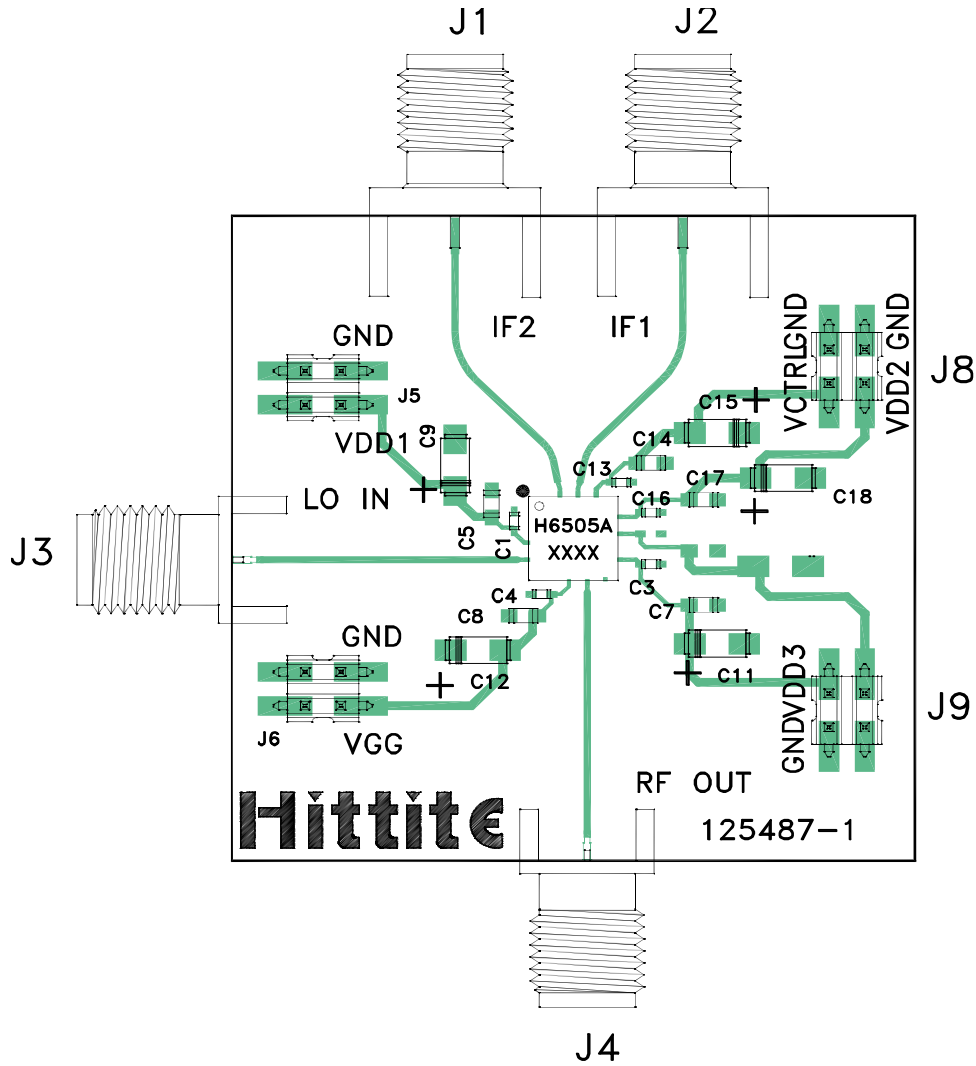


Figure 106. HMC6505A Evaluation Board Top Layer

13800-006

Table 5. Bill of Materials for the EV1HMC6505ALC5 Evaluation Board PCB

| Quantity | Reference Designator   | Description  | Manufacturer                     | Part Number        |
|----------|------------------------|--|----------------------------------|--------------------|
| 1        | Not applicable         | PCB, EV1HMC6505ALC5; circuit board material: Rogers 4350 | Analog Devices supplied          | 125487             |
| 1        | Not applicable         | MCH, evaluation heatsink, aluminum                       | Analog Devices supplied          | 104635             |
| 2        | J1, J2                 | Johnson SMA connectors                                   | Johnson Components               | 142-0701-851       |
| 4        | J5, J6, J8, J9         | 2 mm, four vertical position connector headers           | Molex                            | 87832-0420         |
| 2        | J3, J4                 | SRI K connectors   | SRI Connector Gage Company       | 25-146-1000-92     |
| 5        | C1, C3, C4, C13, C16   | Ceramic capacitors, 100 pF, 5%, 50 V, C0G, 0402          | Murata Manufacturing             | GRM188R71H102KA01D |
| 5        | C5, C7, C8, C14, C17   | Ceramic capacitors, 1000 pF, 50 V, 10%, X7R, 0603        | Keystone Electronics Corporation | 5019               |
| 5        | C9, C11, C12, C15, C18 | Tantalum capacitors, 2.2 μF, 25 V, 10%, SMD, Case A      | AVX                              | TAJA225K025R       |
| 1        | HMC6505A               | Device under test (DUT)                                  | Analog Devices                   | HMC6505A           |

OUTLINE DIMENSIONS

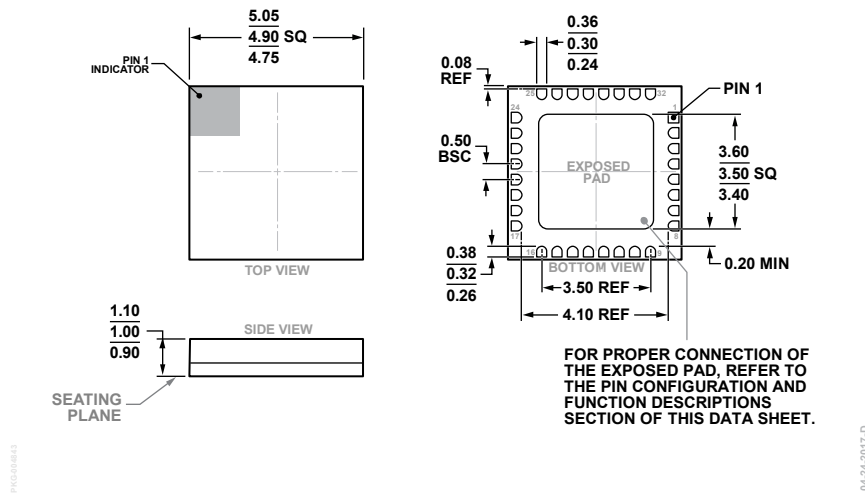


Figure 107. 32-Terminal Ceramic Leadless Chip Carrier (LCC), (E-32-1)  
Dimensions shown in millimeters

ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Body Material | Lead Finish      | Package Description     | MSL Rating <sup>2</sup> | Package Option | Package Marking <sup>3</sup> |
|--------------------|-------------------|-----------------------|------------------|-------------------------|-------------------------|----------------|------------------------------|
| HMC6505ALC5        | -40°C to +85°C    | Alumina Ceramic       | Gold over Nickel | 32-Terminal LCC         | MSL3                    | E-32-1         | H6505A<br>XXXX               |
| HMC6505ALC5TR      | -40°C to +85°C    | Alumina Ceramic       | Gold over Nickel | 32-Terminal LCC         | MSL3                    | E-32-1         | H6505A<br>XXXX               |
| HMC6505ALC5TR-R5   | -40°C to +85°C    | Alumina Ceramic       | Gold over Nickel | 32-Terminal LCC         | MSL3                    | E-32-1         | H6505A<br>XXXX               |
| EV1HMC6505ALC5     |                   |                       |                  | Evaluation PCB Assembly |                         |                |                              |

<sup>1</sup> The HMC6505ALC5, the HMC6505ALC5TR, and HMC6505ALC5TR-R5 are RoHS Compliant Parts.

<sup>2</sup> See the Absolute Maximum Ratings section.

<sup>3</sup> The HMC6505ALC5, the HMC6505ALC5TR, and HMC6505ALC5TR-R5 have a four-digit lot number.