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FGB3236_F085 / FGI3236_F085

EcoSPARK™ 320mJ, 360V, N-Channel Ignition IGBT

Features

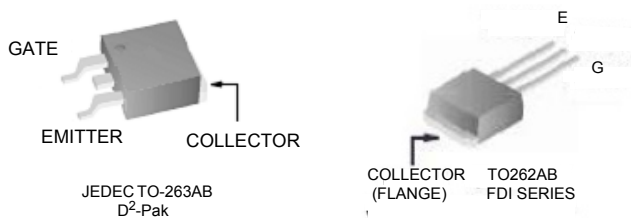
- Industry Standard D²-Pak package
- SCIS Energy = 320mJ at T_J = 25°C
- Logic Level Gate Drive
- Qualified to AEC Q101
- RoHS Compliant

Applications

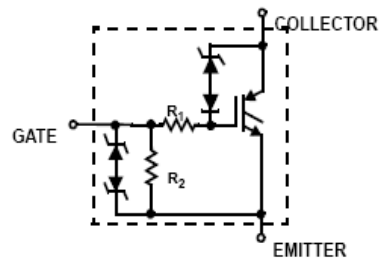
- Automotive Ignition Coil Driver Circuits
- Coil On Plug Applications



Package



Symbol



FGB3236_F085 / FGI3236_F085 320mJ, 360V, N-Channel Ignition IGBT

Device Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
BV_{CER}	Collector to Emitter Breakdown Voltage ($I_C = 1\text{mA}$)	360	V
BV_{ECS}	Emitter to Collector Voltage - Reverse Battery Condition ($I_C = 10\text{mA}$)	24	V
E_{SCIS25}	Self Clamping Inductive Switching Energy ($I_{SCIS} = 14.7\text{A}$, $L = 3.0\text{mH}$, $T_J = 25^\circ\text{C}$)	320	mJ
$E_{SCIS150}$	Self Clamping Inductive Switching Energy ($I_{SCIS} = 10.4\text{A}$, $L = 3.0\text{mH}$, $T_J = 150^\circ\text{C}$)	160	mJ
I_{C25}	Collector Current Continuous, at $V_{GE} = 4.0\text{V}$, $T_C = 25^\circ\text{C}$	44	A
I_{C110}	Collector Current Continuous, at $V_{GE} = 4.0\text{V}$, $T_C = 110^\circ\text{C}$	27	A
V_{GEM}	Gate to Emitter Voltage Continuous	± 10	V
P_D	Power Dissipation Total, at $T_C = 25^\circ\text{C}$	187	W
	Power Dissipation Derating, for $T_C > 25^\circ\text{C}$	1.25	W/ $^\circ\text{C}$
T_J	Operating Junction Temperature Range	-40 to +175	$^\circ\text{C}$
T_{STG}	Storage Junction Temperature Range	-40 to +175	$^\circ\text{C}$
T_L	Max. Lead Temp. for Soldering (Leads at 1.6mm from case for 10s)	300	$^\circ\text{C}$
T_{PKG}	Max. Lead Temp. for Soldering (Package Body for 10s)	260	$^\circ\text{C}$
ESD	Electrostatic Discharge Voltage at 100pF, 1500 Ω	4	kV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FGB3236	FGB3236_F085	TO263	330mm	24mm	800 units
FGI3236	FGI3236_F085	TO262	Tube	NA	50 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off State Characteristics

BV_{CER}	Collector to Emitter Breakdown Voltage	$I_{CE} = 2\text{mA}$, $V_{GE} = 0$, $R_{GE} = 1\text{K}\Omega$, See Fig. 15 $T_J = -40$ to 150°C	330	363	390	V	
BV_{CES}	Collector to Emitter Breakdown Voltage	$I_{CE} = 10\text{mA}$, $V_{GE} = 0\text{V}$, $R_{GE} = 0$, $T_J = -40$ to 150°C	350	378	410	V	
BV_{ECS}	Emitter to Collector Breakdown Voltage	$I_{CE} = -75\text{mA}$, $V_{GE} = 0\text{V}$, $T_C = 25^\circ\text{C}$	30	-	-	V	
BV_{GES}	Gate to Emitter Breakdown Voltage	$I_{GES} = \pm 2\text{mA}$	± 12	± 14	-	V	
I_{CES}	Collector to Emitter Leakage Current	$V_{CES} = 250\text{V}$, See Fig. 11	$T_C = 25^\circ\text{C}$	-	-	25	μA
			$T_C = 150^\circ\text{C}$	-	-	1	mA
I_{ECS}	Emitter to Collector Leakage Current	$V_{EC} = 24\text{V}$, See Fig. 11	$T_C = 25^\circ\text{C}$	-	-	1	mA
			$T_C = 150^\circ\text{C}$	-	-	40	
R_1	Series Gate Resistance		-	100	-	Ω	
R_2	Gate to Emitter Resistance		10K	-	30K	Ω	

On State Characteristics

$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	$I_{CE} = 6\text{A}$, $V_{GE} = 4\text{V}$,	$T_C = 25^\circ\text{C}$, See Fig. 3	-	1.14	1.4	V
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	$I_{CE} = 10\text{A}$, $V_{GE} = 4.5\text{V}$,	$T_C = 150^\circ\text{C}$, See Fig. 4	-	1.32	1.7	V
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	$I_{CE} = 15\text{A}$, $V_{GE} = 4.5\text{V}$,	$T_C = 150^\circ\text{C}$	-	1.61	2.05	V
$I_{CE(ON)}$	Collector to Emitter On State Current	$V_{GE} = 5\text{V}$, $V_{CE} = 5\text{V}$		50	-	-	A

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Dynamic Characteristics

$Q_{G(ON)}$	Gate Charge	$I_{CE} = 10\text{A}$, $V_{CE} = 12\text{V}$, $V_{GE} = 5\text{V}$, See Fig.14	-	20	-	nC
$V_{GE(TH)}$	Gate to Emitter Threshold Voltage	$I_{CE} = 1\text{mA}$, $V_{CE} = V_{GE}$, See Fig. 10	$T_C = 25^\circ\text{C}$ 1.3 1.6 2.2 $T_C = 150^\circ\text{C}$ 0.75 1.1 1.8		V	
V_{GEP}	Gate to Emitter Plateau Voltage	$V_{CE} = 12\text{V}$, $I_{CE} = 10\text{A}$	-	2.6	-	V

Switching Characteristics

$t_{d(ON)R}$	Current Turn-On Delay Time-Resistive	$V_{CE} = 14\text{V}$, $R_L = 1\Omega$	-	0.65	4	μs
t_{rR}	Current Rise Time-Resistive	$V_{GE} = 5\text{V}$, $R_G = 1\text{K}\Omega$ $T_J = 25^\circ\text{C}$, See Fig.12	-	1.7	7	μs
$t_{d(OFF)L}$	Current Turn-Off Delay Time-Inductive	$V_{CE} = 300\text{V}$, $L = 500\mu\text{Hy}$,	-	5.4	15	μs
t_{fL}	Current Fall Time-Inductive	$V_{GE} = 5\text{V}$, $R_G = 1\text{K}\Omega$ $T_J = 25^\circ\text{C}$, See Fig.12	-	1.64	15	μs
SCIS	Self Clamped inductive Switching	$T_J = 25^\circ\text{C}$, $L = 3.0\text{mHy}$, $I_{CE} = 14.7\text{A}$, $R_G = 1\text{K}\Omega$, $V_{GE} = 5\text{V}$, See Fig.1&2	-	-	320	mJ

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case	All Packages	-	-	0.8	$^\circ\text{C/W}$
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Typical Performance Curves

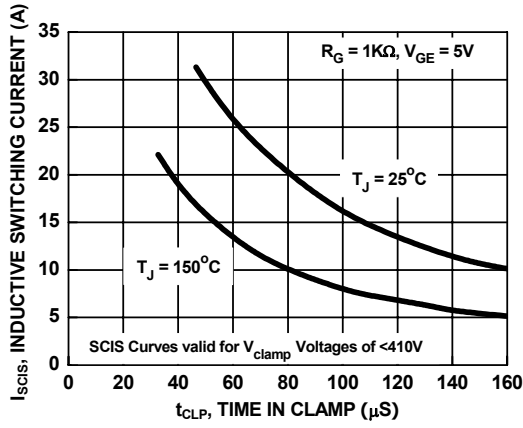


Figure 1. Self Clamped Inductive Switching Current vs. Time in Clamp

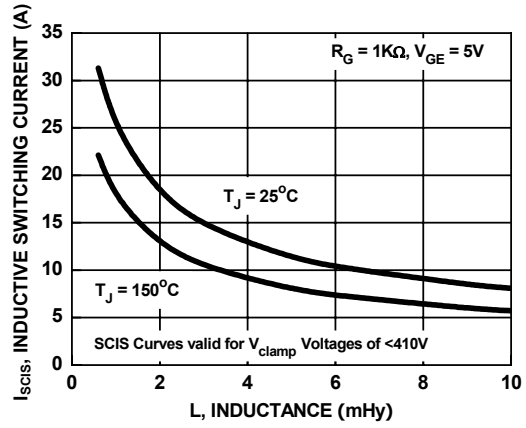


Figure 2. Self Clamped Inductive Switching Current vs. Inductance

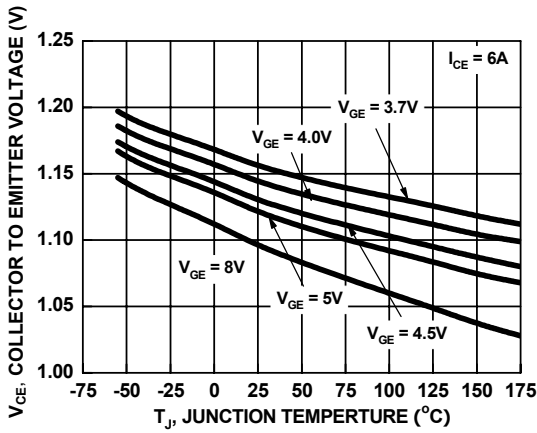


Figure 3. Collector to Emitter On-State Voltage vs. Junction Temperature

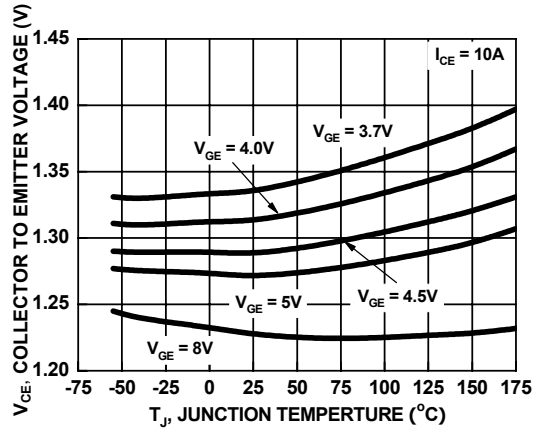


Figure 4. Collector to Emitter On-State Voltage vs. Junction Temperature

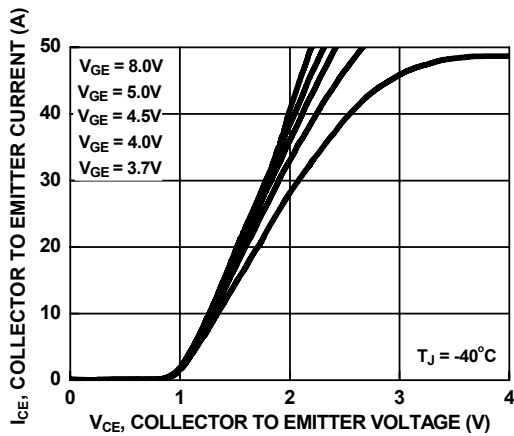


Figure 5. Collector to Emitter On-State Voltage vs. Collector Current

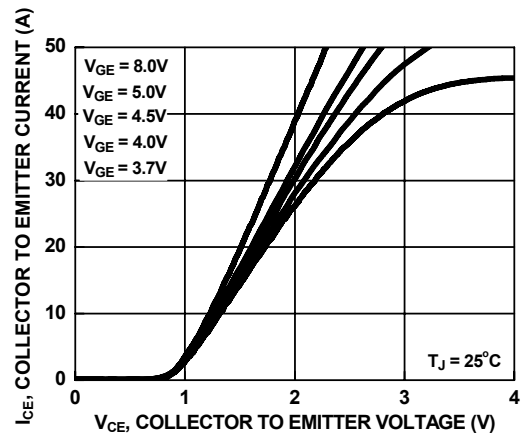


Figure 6. Collector to Emitter On-State Voltage vs. Collector Current

Typical Performance Curves (Continued)

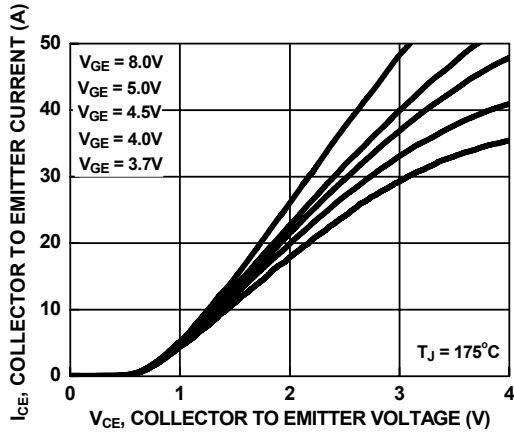


Figure 7. Collector to Emitter On-State Voltage vs. Collector Current

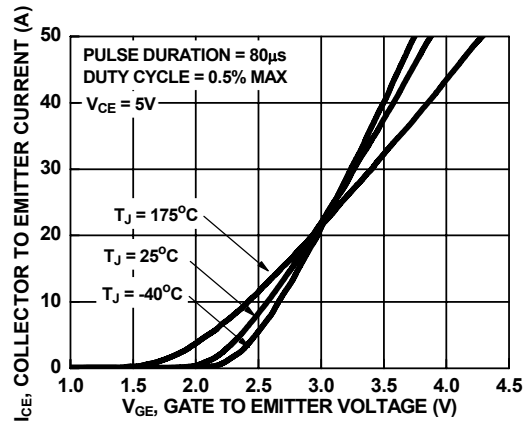


Figure 8. Transfer Characteristics

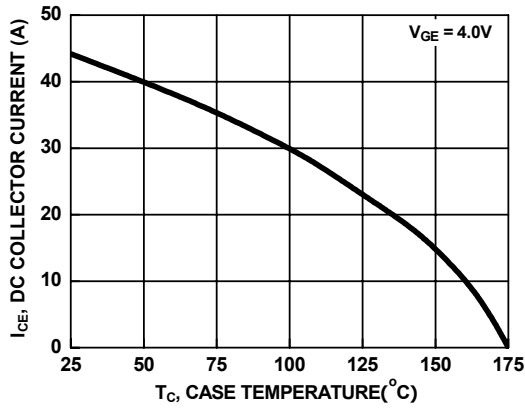


Figure 9. DC Collector Current vs. Case Temperature

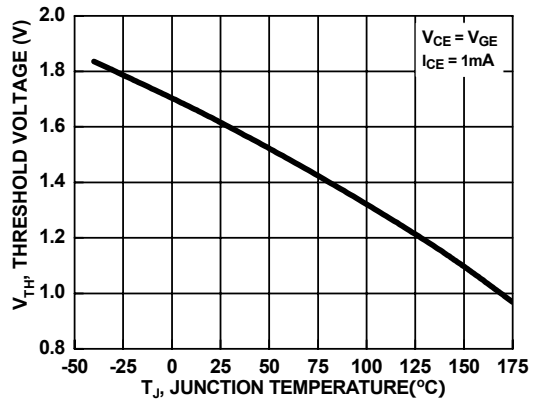


Figure 10. Threshold Voltage vs. Junction Temperature

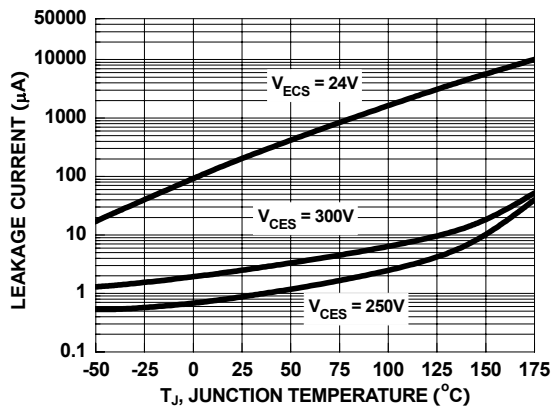


Figure 11. Leakage Current vs. Junction Temperature

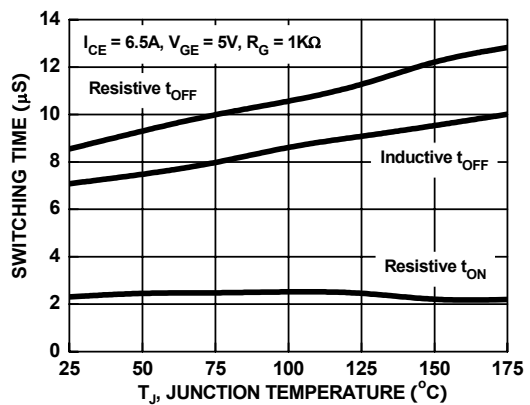


Figure 12. Switching Time vs. Junction Temperature

Typical Performance Curves (Continued)

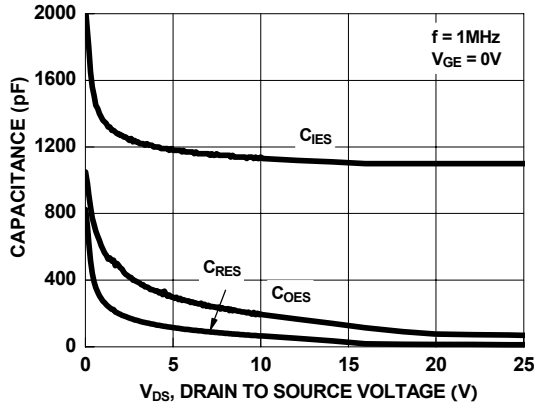


Figure 13. Capacitance vs. Collector to Emitter Voltage

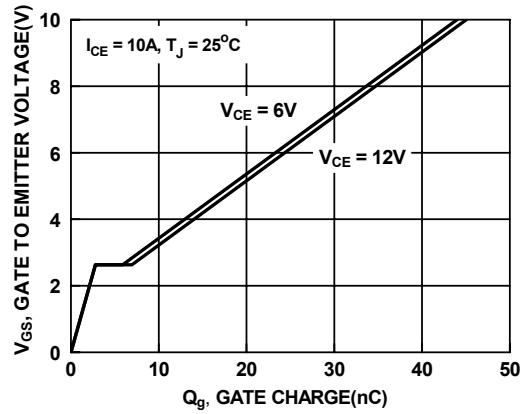


Figure 14. Gate Charge

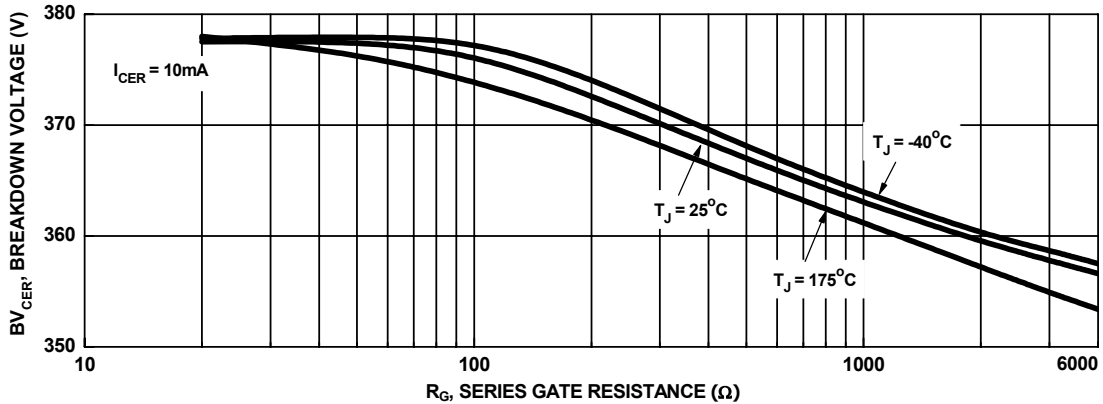


Figure 15. Break Down Voltage vs. Series Gate Resistance

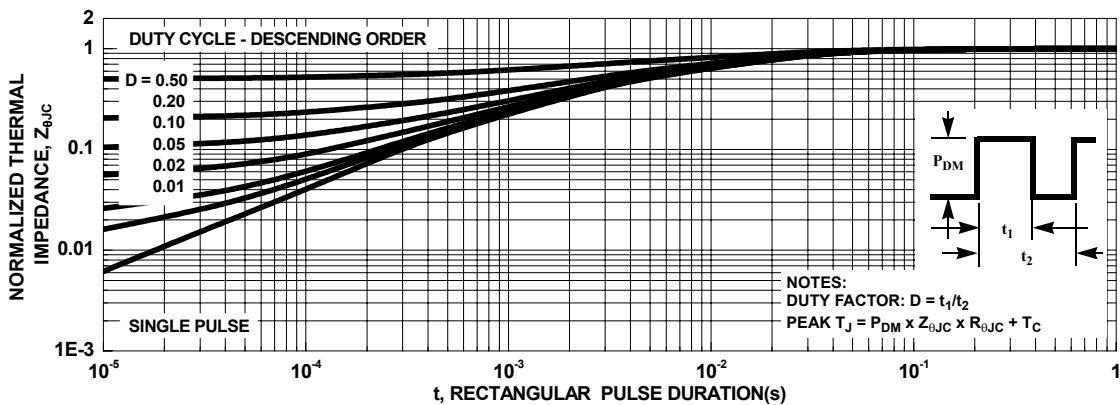


Figure 16. IGBT Normalized Transient Thermal Impedance, Junction to Case

Test Circuit and Waveforms

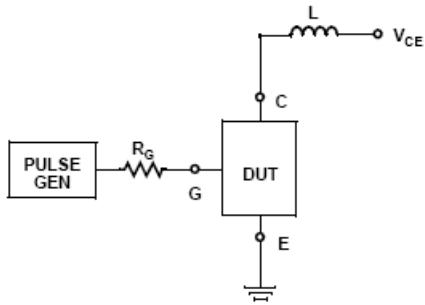


Figure 17. Inductive Switching Test Circuit

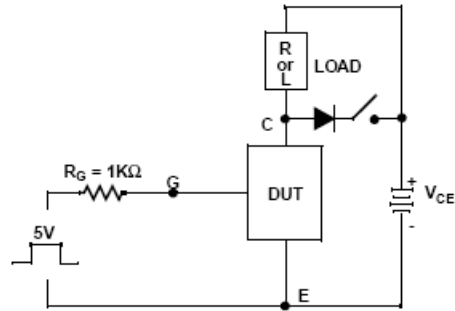


Figure 18. t_{ON} and t_{OFF} Switching Test Circuit

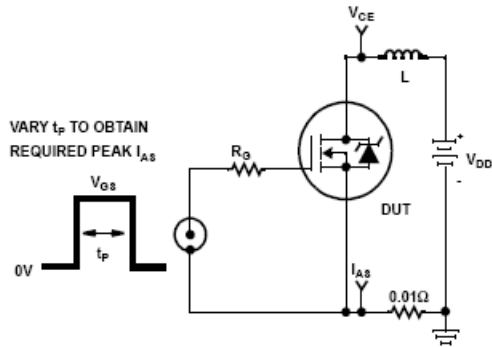


Figure 19. Energy Test Circuit

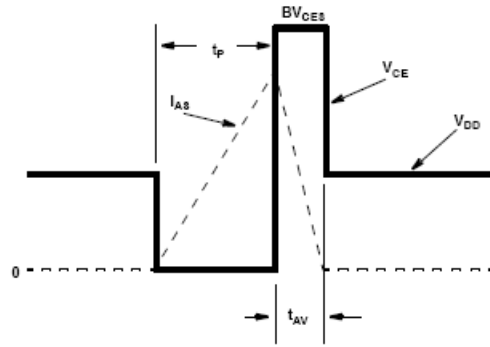
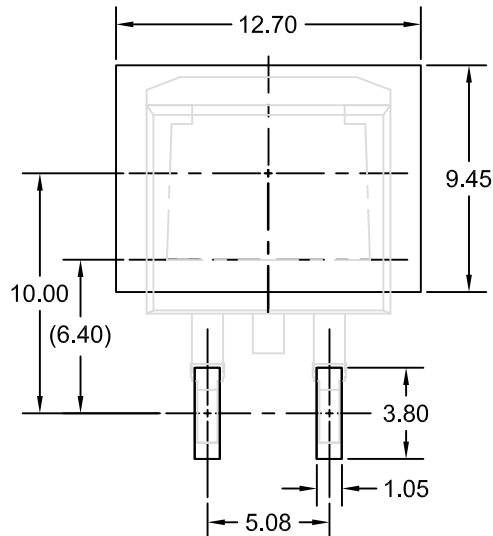
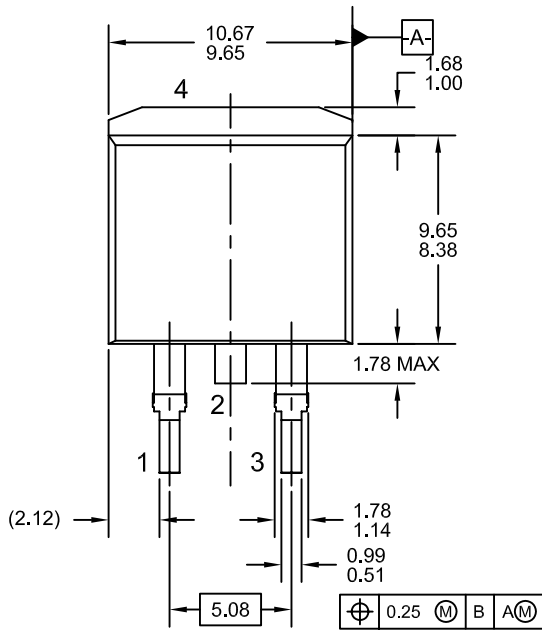
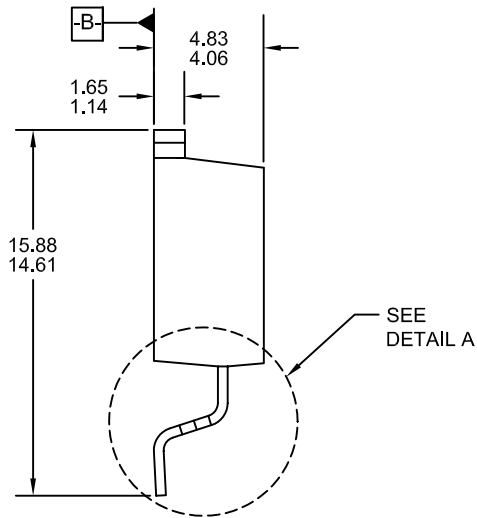
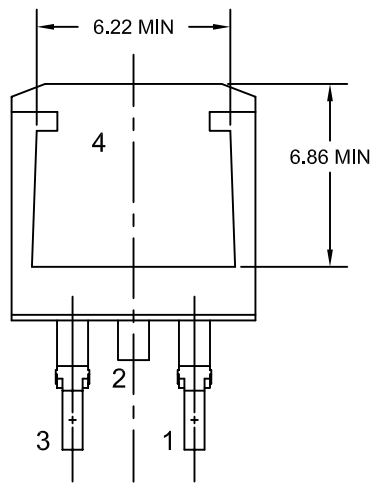


Figure 20. Energy Waveforms

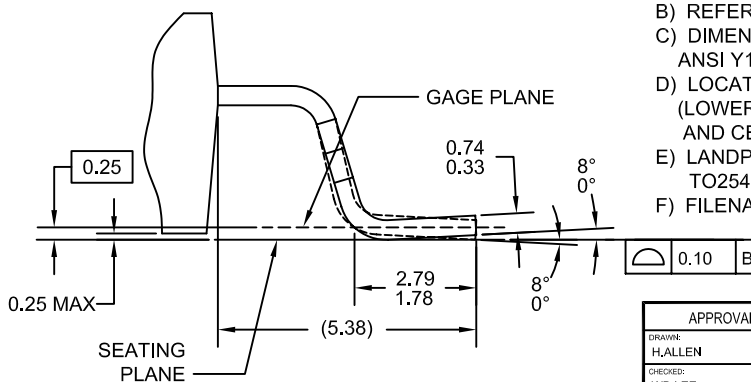
REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APPD
A	RELEASE TO DOCUMENT CONTROL	CB/085/99	08NOV1999	MRG
B	CHG HEATSNK DIM FR 1.25 TO 1.50; INQ DIM FR 1.25 TO 1.50; LD OUT FR 1.25 TO 1.50; ADD DIM 1.25; CHG THK FR 1.25 TO 1.50; CHG THK FR 1.25 TO 1.50; CHG FOOT LTH FR 1.25 TO 1.50; ADD DETAIL A; CHG LD THCK FR 1.25 TO 1.50; CHG FOOT LTH FR 1.25 TO 1.50; ADD DIM 1.50; CHG LAND PATTERN DIM FR 2.50 TO 3.00 MIN; FR FOOT TO 3.00 MIN; FR ADD TO 4.00 MIN; FR 1.25 TO 1.50 MIN; DEL NOTE C; D; AND ARRANGE; ADD NOTE E.	CB/044/00	28FEB2000	MRG
C	CHG ORDERED FR 1.25 TO 1.50; MAX LD THK FR 1.25 TO 1.50; INQ THCK FR 1.25 TO 1.50; HEAT SNK THCK FR 1.25 TO 1.50; LD THCK FR 1.25 TO 1.50; FOOT LANDING FR 1.25 TO 1.50; FOOT ANGLE FR 3 TO 5 DEG; PROFILE DIM FR 1.5 TO MAX TO 1.50; MAX SINK HEAT SNK W/FR BUSH TO 1.50 MIN; LEN FR 1.25 TO 1.50 MIN; REMOVE EJECTOR PIN MARK; ADD NOTE E.	CB/254/04	7OCT2004	RCM
D	REMOVE NOTE B; ADD NOTE E	CB/043/05	30MAR2005	MRG
E	REMOVED SITE INFO AND ECN COLUMN. ADDED NOTE F. TITLE CHANGED	06AUG2007		H.ALLEN
F	UPDATED HEATSNK PER IPC STANDARD. NOTE E IPC REFERENCE. FONT TO ARIAL. UPDATED DRAWING TITLE TO REFLECT JEDEC STANDARD.		02 MAY 09	H.ALLEN



LAND PATTERN RECOMMENDATION
UNLESS NOTED, ALL DIMS TYPICAL



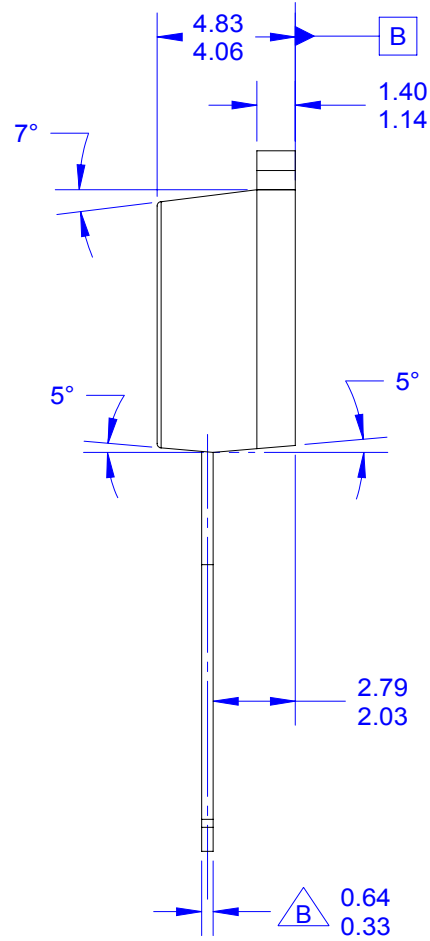
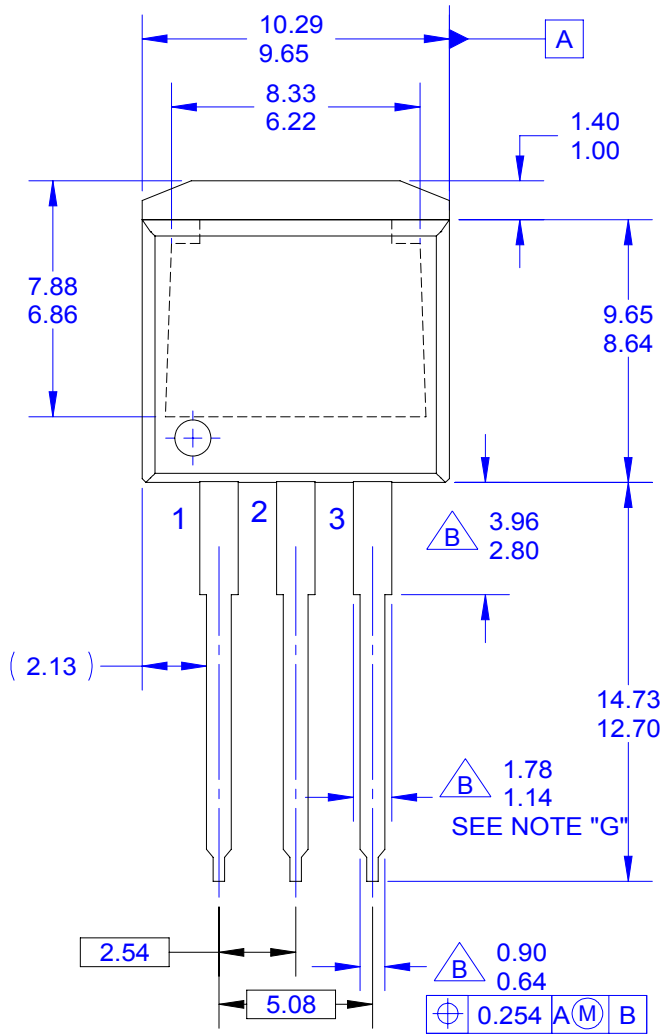
- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
 - B) REFERENCE JEDEC, TO-263, VARIATION AB.
 - C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5M - 1994.
 - D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
 - E) LANDPATTERN RECOMMENDATION PER IPC TO254P1524X482-3N
 - F) FILENAME: TO263A02REV6



DETAIL A, ROTATED 90°
SCALE: 2X

APPROVALS		DATE		2LD, JEDEC TO-263, VARIATION AB, SURFACE MOUNT
DRAWN:	H.ALLEN	2 MAY 09		
CHECKED:	WB LEE	2 MAY 09		
APPROVED:				
			SCALE: 1:1	SIZE: NA
			DRAWING NUMBER: MKT-TO263A02	REV: 6
			FORMERLY: N/A	SHEET: 1 OF 1

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NOTES:






- A. EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.
- B. DOES NOT COMPLY JEDEC STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
- F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)
- G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.
- H. DRAWING FILE NAME: TO262A03REV5

APPROVALS		DATE					
DRAWN: BOBOY MALDO		11FEB2010					
CHECKED: KH LEE				TO262 3LD JEDEC VARIATION AA			
APPROVED: BY HUANG							
APPROVED: HOWARD ALLEN							
PROJECTION				SCALE	SIZE	DRAWING NUMBER	REV
				1:1	N/A	MKT-TO262A03	5
				FORMERLY: N/A		SHEET: 1 OF 1	



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Definition of Terms

Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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