4042B
QUAD D LATCH

DESCRIPTION – The 4042B is a 4-Bit Latch with four Data Inputs (D_0-D_3), four buffered Latch Outputs (Q_0-Q_3), four buffered Complementary Latch Outputs ($\overline{Q}_0$-$\overline{Q}_3$) and two Common Enable Inputs (E_0 and E_1). Information on the Data Inputs (D_0-D_3) is transferred to the Outputs (Q_0-Q_3) while both Enable Inputs (E_0, E_1) are in the same state, either HIGH or LOW. The Outputs (Q_0-Q_3) follow the Data Inputs (D_0-D_3) as long as both Enable Inputs (E_0, E_1) remain in the same state. When the two Enable Inputs (E_0, E_1) are different, the Data Inputs (D_0-D_3) do not affect the Outputs (Q_0-Q_3) and the information in the latch is stored. The $\overline{Q}_0$–$\overline{Q}_3$ Outputs are always the complement of the Q_0-Q_3 Outputs. The Exclusive-OR input structure allows the choice of either polarity for the Enable Input. With one Enable Input HIGH, the other Enable Input is active HIGH; with one Enable Input LOW, the other Enable Input is active LOW.

The last moment prior to the trailing end of the enable condition that the Latch Outputs can still be affected by the inputs is specified as a set-up time. A negative set-up time, as typically exhibited by this device, means that the latches respond to input changes after the end of the enable condition. Following established industry practice, a hold time is specified, defining the time after the end of the enable condition, that the inputs must be held stable, so that they do not affect the state of the latches. It follows from this definition, that the hold time is identical with the negative set-up time. Set-up and hold times have a tolerance, due to manufacturing process variations, temperature and supply voltage changes. For predictable operation the data input levels must be held stable over the full spread of this timing window starting with the earliest set-up time (largest positive or smallest negative value) to the latest hold time.

- **ACTIVE HIGH OR ACTIVE LOW ENABLE**
- **TRUE AND COMPLEMENTARY OUTPUTS (Q & $\overline{Q}$)**

PIN NAMES

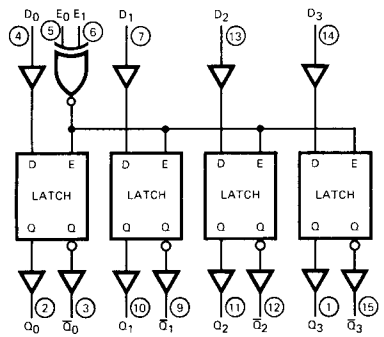
D_0-D_3	Data Inputs
E_0, E_1	Enable Inputs
Q_0-Q_3	Parallel Latch Outputs
$\overline{Q}_0$-$\overline{Q}_3$	Complementary Parallel Latch Outputs

TRUTH TABLE

E_0	E_1	LATCH CONDITION
L	L	Enabled
L	H	Not Enabled
H	L	Not Enabled
H	H	Enabled

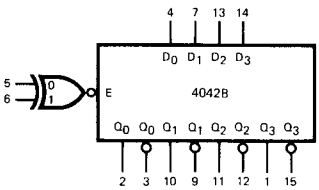
L = LOW Level
H = HIGH Level

LOGIC DIAGRAM



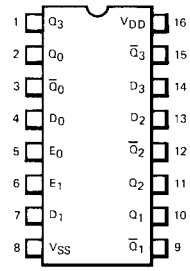
V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

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DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20 150			40 300			80 600	μA	MIN, 25°C MAX	All inputs at 0 V or V_{DD}
		XM			5 150			10 300			20 600	μA	MIN, 25°C MAX	

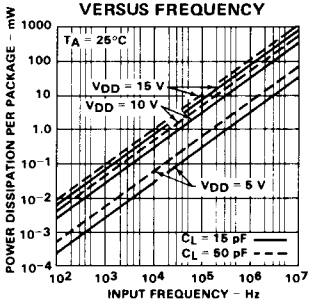
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		101	200		45	90		33	72	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PHL}	Data to Output		99	200		44	88		33	70	ns	
t_{PLH}	Propagation Delay,		156	310		66	132		47	106	ns	
t_{PHL}	Enable to Output		137	275		58	116		41	93	ns	
t_{TLH}	Output Transition Time		65	135		31	70		25	45	ns	
t_{THL}			60	135		26	70		20	45	ns	
t_s	Set-Up Time, D_n to E_0 or E_1	10	-12		10	-6		8	-4		ns	
t_h	Hold Time, D_n to E_0 or E_1	50	25		25	13		20	7		ns	
$t_w E_n$	Minimum Enable Pulse Width	80	40		32	16		26	12		ns	

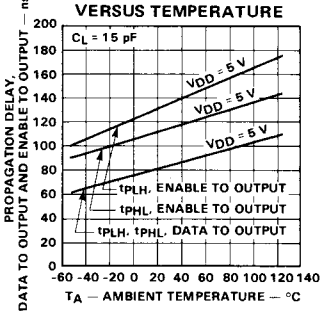
NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

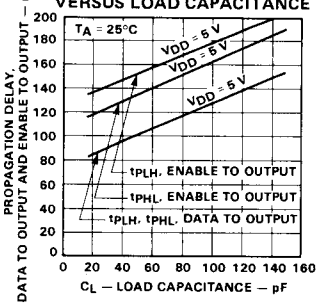
TYPICAL POWER DISSIPATION VERSUS FREQUENCY



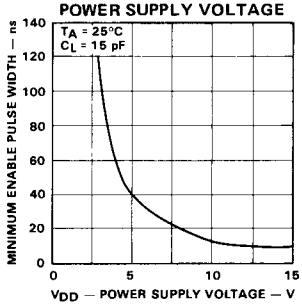
PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



MINIMUM ENABLE PULSE WIDTH VERSUS POWER SUPPLY VOLTAGE



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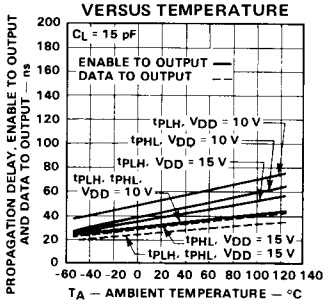
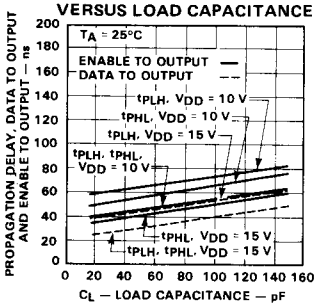


PROPAGATION DELAY VERSUS LOAD CAPACITANCE



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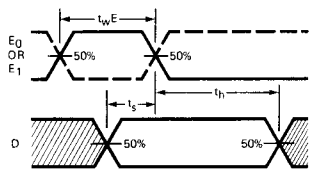
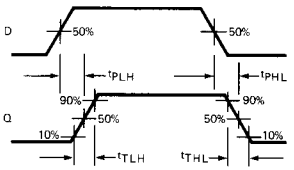
SWITCHING WAVEFORMS

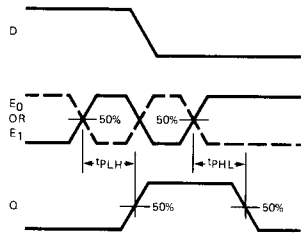


SET-UP AND HOLD TIMES, MINIMUM ENABLE PULSE WIDTH

NOTE:
Either E_0 or E_1 is held HIGH or LOW while the other Enable Input is pulsed as per the Truth Table. t_s and t_h are shown as positive values but may be specified as negative values.



PROPAGATION DELAY DATA TO OUTPUT AND TRANSITION TIMES, WITH LATCH ENABLED



PROPAGATION DELAY ENABLE TO OUTPUT

NOTE:
Either E_0 or E_1 is held HIGH or LOW while the other Enable Input is pulsed as per the Truth Table.