HM-6551/883

256 x 4 CMOS RAM

FN2988
Rev.2.00
July 2003

The HM-6551/883 is a 256 x 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation. On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6551/883 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Ordering Information

PACKAGE	TEMP. RANGE	220ns	300ns	PKG. DWG. #
CERDIP	-55°C to +125°C	HM1-6551B/883	HM1-6551/883	F22.4

Pin Descriptions

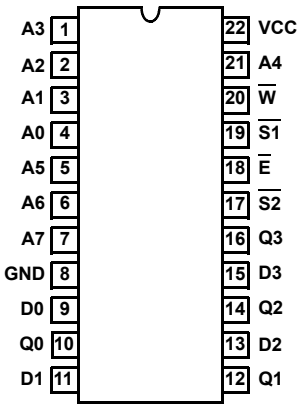
PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
D	Data Input
Q	Data Output

Features

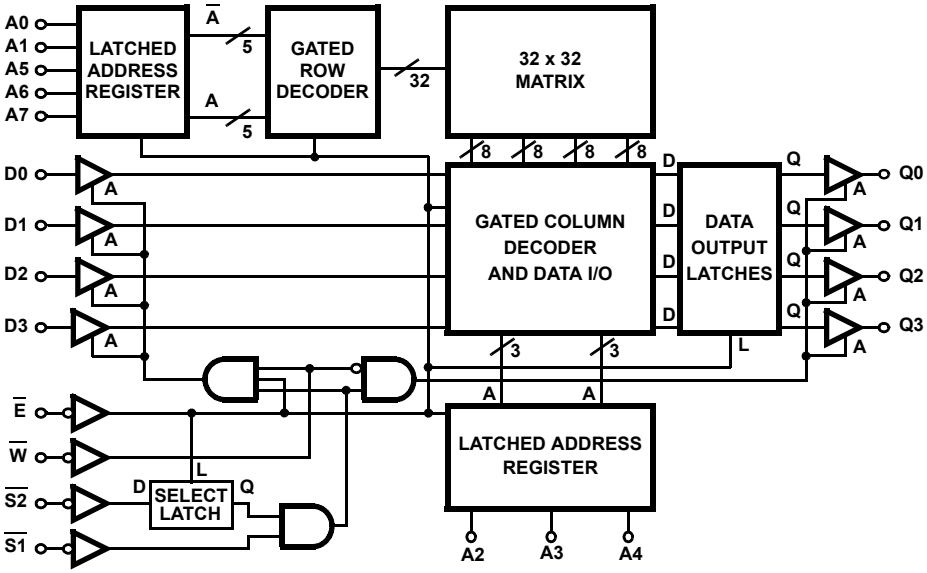
- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Power Standby . . . . . 50µW Max
- Low Power Operation. . . . . .20mW/MHz Max
- Fast Access Time. . . . . 220ns Max
- Data Retention . . . . . .at 2.0V Min
- TTL Compatible Input/Output
- High Output Drive - 1 TTL Load
- Internal Latched Chip Select
- High Noise Immunity
- On-Chip Address Register
- Latched Outputs
- Three-State Output

Pinout

HM-6551/883 (CERDIP)
TOP VIEW



Functional Diagram



NOTES:

1. Select Latch: L Low → Q = D and Q latches on rising edge of L.
2. Address Latches And Gated Decoders: Latch on falling edge of $\overline{E}$ and gate on falling edge of $\overline{E}$.
3. All lines positive logic-active high.
4. Three-State Buffers: A high → output active.
5. Data Latches: L High → Q = D and Q latches on falling edge of L.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to VCC +0.3V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C
Input Low Voltage . . . . . 0V to +0.8V
nput High Voltage . . . . . .VCC -2.0V to VCC
Input Rise and Fall Time . . . . . 40ns Max.

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CERDIP Package	60°C/W	15°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 1930 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

TABLE 1. HM-6551/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V IOL = 1.6mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V IOH = -0.4mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	+1.0	µA
Output Leakage Current	IOZ	VCC = 5.5 V, VO = GND or VCC	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC IO = 0mA, VI = VCC or GND	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	10	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 2) $\overline{E}$ = 1MHz, IO = 0mA VI = VCC or GND	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	4	mA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA VI = VCC or GND	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	10	µA

NOTES:

1. All voltages referenced to device GND.
2. Typical derating 1.5mA/MHz increase in ICCOP.

TABLE 2. HM-6551/883 A.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL		(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS				UNITS
						HM-6551B/883		HM-6551/883		
						MIN	MAX	MIN	MAX	
Chip Enable Access Time	(1)	TELQV	VCC = 4.5 and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	220	-	300	ns
Address Access Time	(2)	TAVQV	VCC = 4.5 and 5.5V, Note 3	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	220	-	300	ns
Chip Select 1 Output Enable Time	(3)	TS1LQX	VCC = 4.5 and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	5	-	5	-	ns
Write Enable Output Disable Time	(4)	TWLQZ	VCC = 4.5 and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	130	-	150	ns
Chip Select 1 Output Disable Time	(5)	TS1HQZ	VCC = 4.5 and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	130	-	150	ns
Chip Enable Pulse Negative Width	(6)	TELEH	VCC = 4.5 and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	220	-	300	-	ns
Chip Enable Pulse Positive Width	(7)	TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	100	-	100	-	ns
Address Setup Time	(8)	TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	0	-	0	-	ns
Chip Select 2 Setup Time	(9)	TS2LEL	VCC = 4.5 and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	0	-	0	-	ns
Address Hold Time	(10)	TELAX	VCC = 4.5 and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	40	-	50	-	ns
Chip Select 2 Hold Time	(11)	TELS2X	VCC = 4.5 and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	40	-	50	-	ns
Data Setup Time	(12)	TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	100	-	150	-	ns
Data Hold Time	(13)	TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	0	-	0	-	ns
Chip Select 1 Write Pulse Setup Time	(14)	TWLS1H	VCC = 4.5 and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	120	-	180	-	ns
Chip Enable Write Pulse Setup Time	(15)	TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	120	-	180	-	ns
Chip Select 1 Write Pulse Hold Time	(16)	TS1LWH	VCC = 4.5 and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	120	-	180	-	ns
Chip Enable Write Pulse Hold Time	(17)	TELWH	VCC = 4.5 and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	120	-	180	-	ns
Write Enable Pulse Width	(18)	TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	120	-	180	-	ns
Read or Write Cycle Time	(19)	TELEL	VCC = 4.5 and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	320	-	400	-	ns

NOTES:

1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 1.6mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. TAVQV = TELQV + TAVEL.

TABLE 3. HM-6551B/883 AND HM-6551/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	T_A = +25°C	-	10	pF
Output Capacitance	CO	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	T_A = +25°C	-	12	pF

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Timing Waveforms

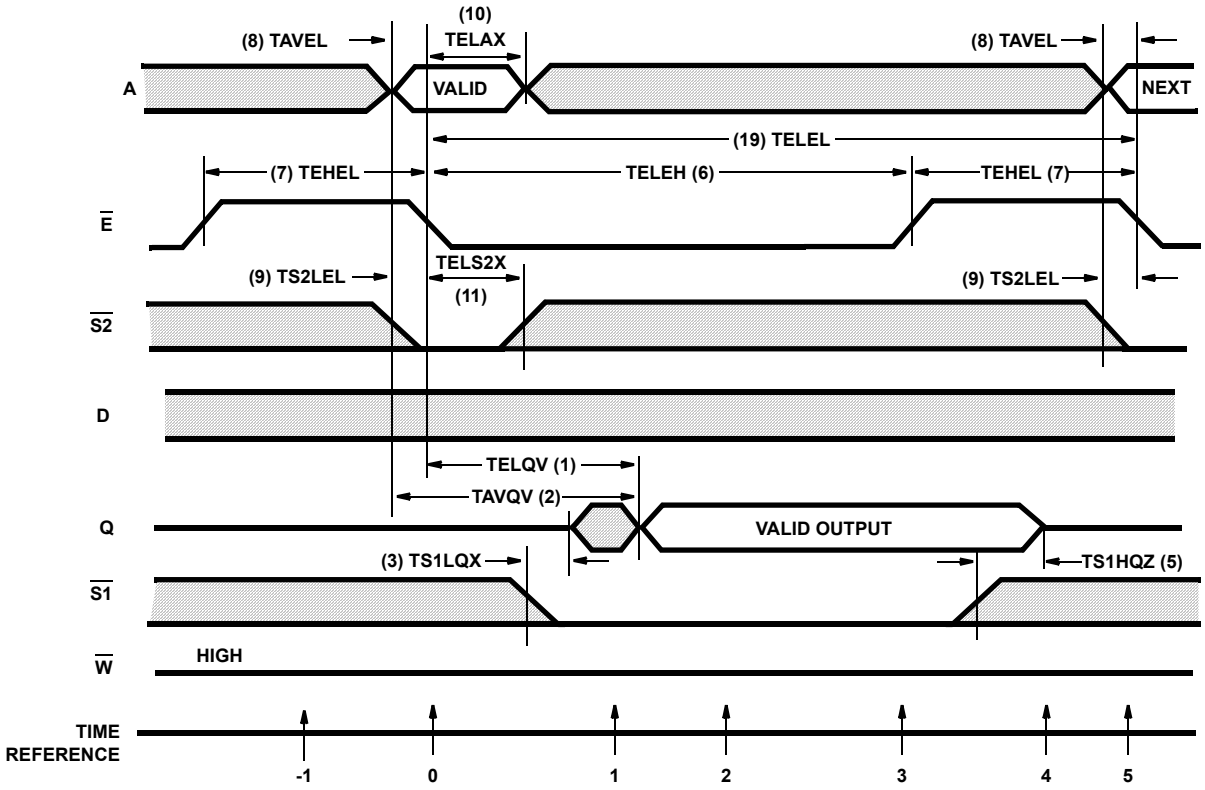


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS						OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{S2}$	$\overline{W}$	A	D	Q	
-1	H	H	X	X	X	X	Z	Memory Disabled
0	↘	X	L	H	V	X	Z	Addresses and $\overline{S2}$ are Latched, Cycle Begins
1	L	L	X	H	X	X	X	Output Enabled but Undefined
2	L	L	X	H	X	X	V	Data Output Valid
3	↗	L	X	H	X	X	V	Outputs Latched, Valid Data, $\overline{S2}$ Unlatches
4	H	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	X	L	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The HM-6551/883 Read Cycle is initiated by the falling edge of $\overline{E}$. This signal latches the input address word and $\overline{S2}$ into on-chip registers providing the minimum setup and hold times are met. After the required hold time, these inputs may change state without affecting device operation. $\overline{S2}$ acts as a high order address and simplifies decoding. For the output to be read, $\overline{E}$, $\overline{S1}$ must be low and $\overline{W}$ must be high. $\overline{S2}$ must have been latched low on the falling edge of $\overline{E}$. The output data will be valid at access time (TELQV). The HM-6551/883 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains in that state until $\overline{E}$ falls. Also on the rising edge of $\overline{E}$, $\overline{S2}$ unlatches and controls the outputs along with $\overline{S1}$. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Timing Waveforms (Continued)

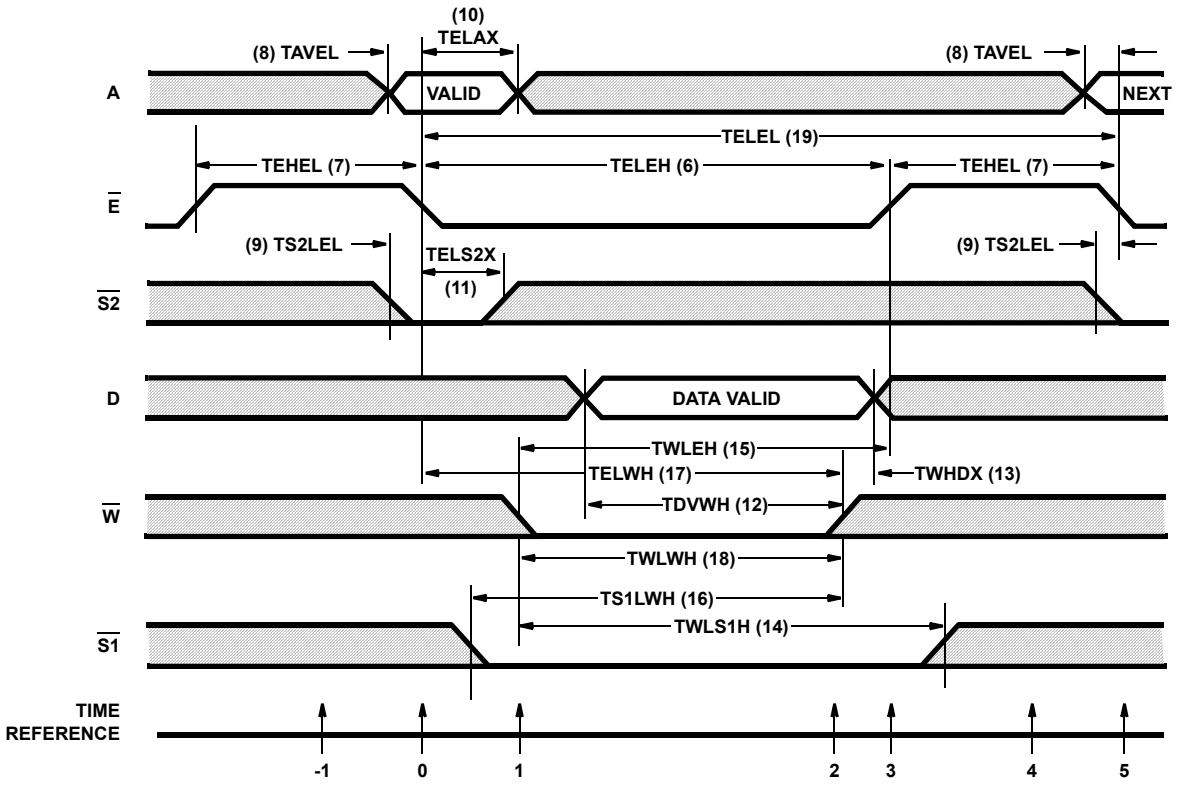


FIGURE 2. WRITE CYCLE

TRUTH TABLE

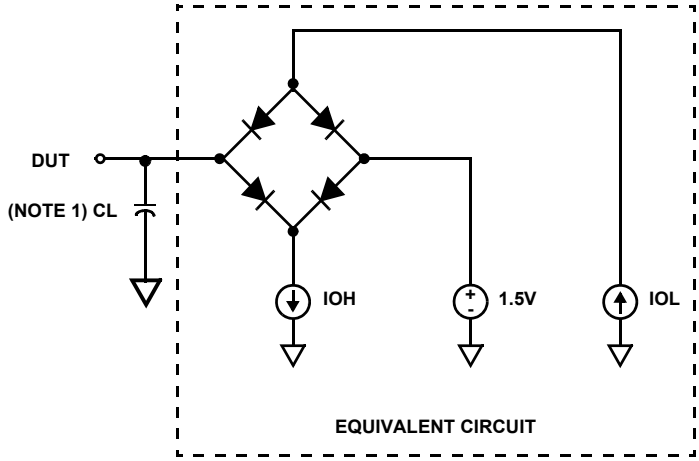
TIME REFERENCE	INPUTS						OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{S2}$	$\overline{W}$	A	D	Q	
-1	H	H	X	X	X	X	Z	Memory Disabled
0	↘	X	L	X	V	X	Z	Cycle Begins, Addresses and $\overline{S2}$ are Latched
1	L	L	X	↘	X	X	Z	Write Period Begins
2	L	L	X	↗	X	V	Z	Data In is Written
3	↗	X	X	H	X	X	Z	Write is Completed
4	H	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	X	L	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

In the Write Cycle the falling edge of $\overline{E}$ latches the addresses and $\overline{S2}$ into on-chip registers. $\overline{S2}$ must be latched in the low state to enable the device. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$ being low and $\overline{S2}$ being latched simultaneously. The $\overline{W}$ line may go low at any time during the cycle providing that the write pulse setup times (TWLEH and TWLS1H) are met. The write portion of the cycle is terminated on the first rising edge of either $\overline{E}$, $\overline{W}$, or $\overline{S1}$.

If a series of consecutive write cycles are to be executed, the $\overline{W}$ line may be held low until all desired locations have been written. If this method is used, data setup and hold times must be referenced to the first rising edge of $\overline{E}$ or $\overline{S1}$. By positioning the write pulse at different times within the $\overline{E}$ and $\overline{S1}$ low time (TELEH), various types of write cycles may be performed. If the $\overline{S1}$ low time (TS1LS1H) is greater than the $\overline{W}$ pulse, plus an output enable time (TS1LQX), a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The HM-6551/883 may be used on a common I/O bus structure by tying the input and output pins together. The multiplexing is accomplished internally by the $\overline{W}$ line. In the write cycle, when $\overline{W}$ goes low, the output buffers are forced to a high impedance state. One output disable time delay (TWLQZ) must be allowed before applying input data to the bus.

Test Load Circuit

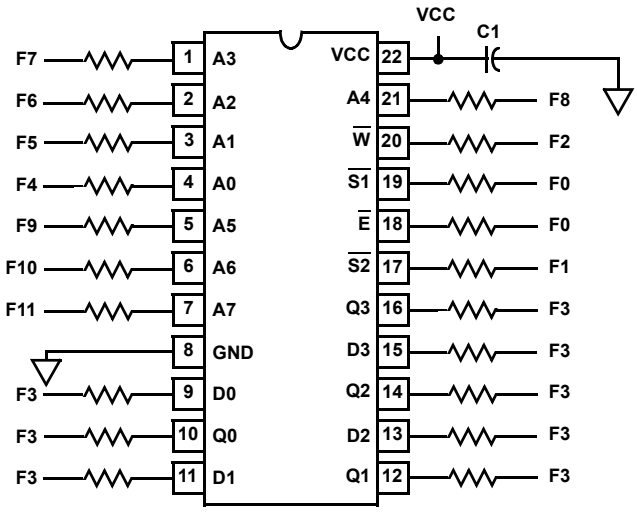


NOTE:

1. Test head capacitance includes stray and jig capacitance.

Burn-In Circuit

HM-6551/883
CERDIP



NOTES:
All resistors 47kΩ ±5%.
F0 = 100kHz ±10%.
F1 = F0 ÷ 2, F2 = F1 ÷ 2, F3 = F2 ÷ 2 . . . F12 = F11 ÷ 2.
VCC = 5.5V ±0.5V.
VIH = 4.5V ±10%.
VIL = -0.2V to +0.4V.
C1 = 0.01µF Min.

Die Characteristics

DIE DIMENSIONS:
132 x 160 x 19 ±1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ±2kÅ

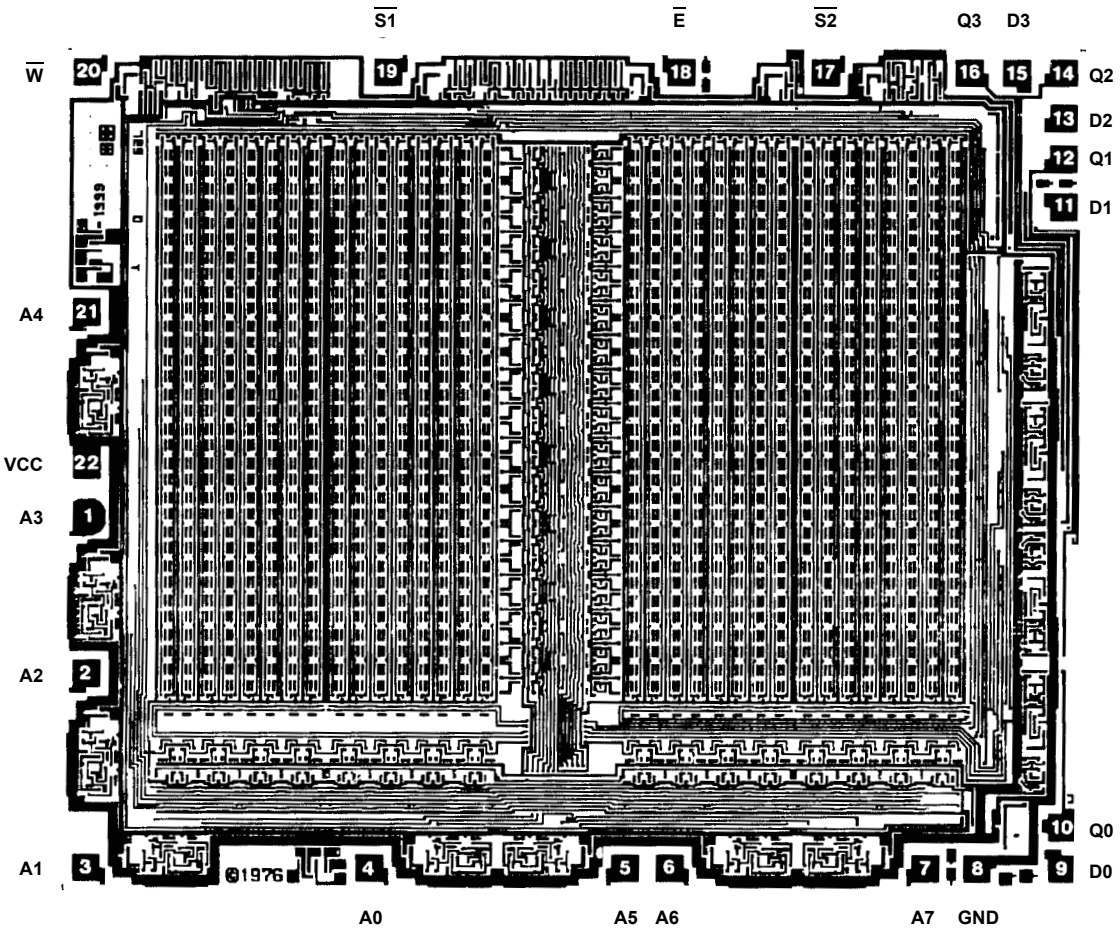
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
1.337×10^5 A/cm^2

LEAD TEMPERATURE (10s soldering):
≤300°C

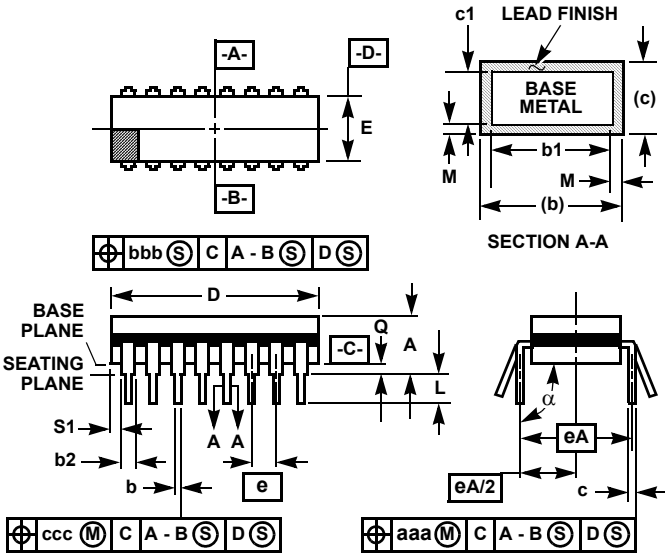
Metallization Mask Layout

HM-6551/883



NOTE: Pin numbers correspond to DIP Package only.

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F22.4 MIL-STD-1835 GDIP1-T22 (D-7, CONFIGURATION A)
22 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.111	-	28.22	5
E	0.350	0.410	8.89	10.41	5
e	0.100 BSC		2.54 BSC		-
eA	0.400 BSC		10.16 BSC		-
eA/2	0.200 BSC		5.08 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	22		22		8

Rev. 0 6/13/95