



27C512A

512K (64K x 8) CMOS EPROM

FEATURES

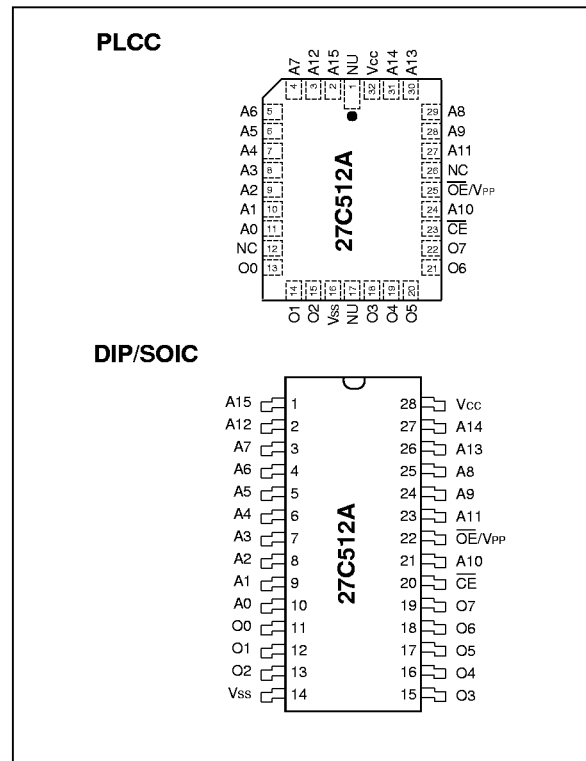
- High speed performance
- CMOS Technology for low power consumption
 - 25 mA Active current
 - 30 μ A Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- High speed express programming algorithm
- Organized 64K x 8: JEDEC standard pinouts
 - 28-pin Dual-in-line package
 - 32-pin PLCC Package
 - 28-pin SOIC package
 - Tape and reel
- Data Retention > 200 years
- Available for the following temperature ranges
 - Commercial: 0°C to +70°C
 - Industrial: -40°C to +85°C
 - Automotive: -40°C to +125°C

DESCRIPTION

The Microchip Technology Inc. 27C512A is a CMOS 512K bit electrically Programmable Read Only Memory (EPROM). The device is organized into 64K words by 8 bits (64K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 90 ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and high reliability are requirements.

A complete family of packages is offered to provide the most flexibility in applications. For surface mount applications, PLCC or SOIC packaging is available. Tape or reel packaging is also available for PLCC or SOIC packages.

PACKAGE TYPES



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

VCC and input voltages w.r.t. VSS -0.6V to +7.25V

VPP voltage w.r.t. VSS during programming -0.6V to +14V

Voltage on A9 w.r.t. VSS..... -0.6V to +13.5V

Output voltage w.r.t. VSS.....-0.6V to VCC +1.0V

Storage temperature -65°C to +150°C

Ambient temp. with power applied..... -65°C to +125°C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

| Name | Function |
|------------------------|---|
| A0-A15 | Address Inputs |
| \overline{CE} | Chip Enable |
| \overline{OE}/V_{PP} | Output Enable/Programming Voltage |
| O0 - O7 | Data Output |
| VCC | +5V Power Supply |
| VSS | Ground |
| NC | No Connection; No Internal Connection |
| NU | Not Used; No External Connection is Allowed |

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

| VCC = +5V ±10% Commercial: Tamb = 0°C to +70°C Industrial: Tamb = -40°C to +85°C Extended (Automotive): Tamb = -40°C to +125°C | | | | | | | |
|---|------------------|------------|------------------------|------|--------------------|-------|--|
| Parameter | Part* | Status | Symbol | Min | Max | Units | Conditions |
| Input Voltages | all | Logic "1" | V _{IH} | 2.0 | V _{CC} +1 | V | |
| | | Logic "0" | V _{IL} | -0.5 | 0.8 | V | |
| Input Leakage | all | | I _{LI} | -10 | 10 | µA | V _{IN} = 0 to V _{CC} |
| Output Voltages | all | Logic "1" | V _{OH} | 2.4 | | V | I _{OH} = -400 µA I _{OL} = 2.1 mA |
| | | Logic "0" | V _{OL} | | 0.45 | V | |
| Output Leakage | all | — | I _{LO} | -10 | 10 | µA | V _{OUT} = 0V to V _{CC} |
| Input Capacitance | all | — | C _{IN} | — | 6 | pF | V _{IN} = 0V; Tamb = 25°C; f = 1 MHz |
| Output Capacitance | all | — | C _{OUT} | — | 12 | pF | V _{OUT} = 0V; Tamb = 25°C; f = 1 MHz |
| Power Supply Current, Active | C I, E | TTL input | I _{CC} | — | 25 | mA | V _{CC} = 5.5V f = 1 MHz; $\overline{OE}/V_{PP} = \overline{CE} = V_{IL}$; I _{OUT} = 0 mA; V _{IL} = -0.1 to 0.8V; V _{IH} = 2.0 to V _{CC} ; Note 1 |
| | | TTL input | I _{CC} | — | 35 | mA | |
| Power Supply Current, Standby | C I, E all | TTL input | I _{CC(S)TLL} | — | 1 | mA | $\overline{CE} = V_{CC} \pm 0.2V$ |
| | | TTL input | I _{CC(S)TLL} | — | 2 | mA | |
| | | CMOS input | I _{CC(S)CMOS} | — | 30 | µA | |

* Parts: C=Commercial Temperature Range; I, E=Industrial and Extended Temperature Ranges

Note 1: Typical active current increases .75 mA per MHz up to operating frequency for all temperature ranges.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

| AC Testing Waveform: | | V _{IH} = 2.4V and V _{IL} = .45V; V _{OH} = 2.0V and V _{OL} = 0.8V | | | | | | | | | |
|--|------------------|--|-----|------------|-----|-----------|------------------------------------|-----------|-----|-------|---|
| Output Load: | | 1 TTL Load + 100 pF | | | | | | | | | |
| Input Rise and Fall Times: | | 10 ns | | | | | | | | | |
| Ambient Temperature: | | Commercial: | | | | | T _{amb} = 0°C to +70°C | | | | |
| | | Industrial: | | | | | T _{amb} = -40°C to +85°C | | | | |
| | | Extended (Automotive): | | | | | T _{amb} = -40°C to +125°C | | | | |
| Parameter | Sym | 27C512-90* | | 27C512-10* | | 27C512-12 | | 27C512-15 | | Units | Conditions |
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Address to Output Delay | t _{ACC} | — | 90 | — | 100 | — | 120 | — | 150 | ns | $\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$ |
| \overline{CE} to Output Delay | t _{CE} | — | 90 | — | 100 | — | 120 | — | 150 | ns | $\overline{OE}/V_{PP} = V_{IL}$ |
| \overline{OE} to Output Delay | t _{OE} | — | 40 | — | 40 | — | 50 | — | 60 | ns | $\overline{CE} = V_{IL}$ |
| \overline{OE} to Output High Impedance | t _{OFF} | 0 | 35 | 0 | 35 | 0 | 40 | 0 | 45 | ns | |
| Output Hold from Address, \overline{CE} or \overline{OE} / V _{PP} , whichever occurred first | t _{OH} | 0 | — | 0 | — | 0 | — | 0 | — | ns | |

*90/10 AC Testing Waveforms: V_{IH} = 3.0V and V_{IL} = 0V; V_{OH} = 1.5V and V_{OL} = 1.5V
Output Load: 1 TTL Load + 30 pF

FIGURE 1-1: READ WAVEFORMS

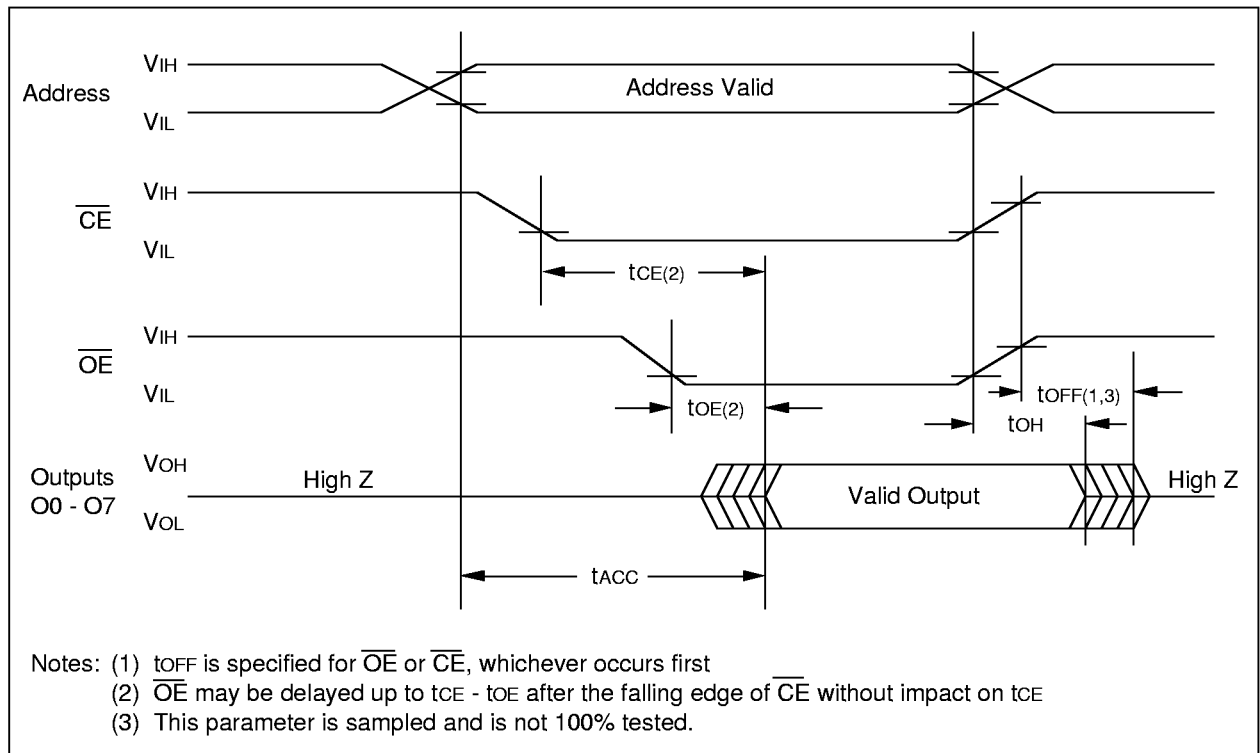


TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

| Ambient Temperature: $T_{amb} = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ $V_{CC} = 6.5\text{V} \pm 0.25\text{V}$, $\overline{\text{OE}}/V_{PP} = V_H = 13.0\text{V} \pm 0.25\text{V}$ | | | | | | |
|--|-----------|-----------|------|------------|---------------|---------------------------------|
| Parameter | Status | Symbol | Min. | Max. | Units | Conditions (See Note 1) |
| Input Voltages | Logic "1" | V_{IH} | 2.0 | $V_{CC}+1$ | V | |
| | Logic "0" | V_{IL} | -0.1 | 0.8 | V | |
| Input Leakage | — | I_{LI} | -10 | 10 | μA | $V_{IN} = 0\text{V to } V_{CC}$ |
| Output Voltages | Logic "1" | V_{OH} | 2.4 | | V | $I_{OH} = -400 \mu\text{A}$ |
| | Logic "0" | V_{OL} | — | 0.45 | V | $I_{OL} = 2.1 \text{ mA}$ |
| VCC Current, program & verify | — | I_{CC2} | — | 35 | mA | $\overline{\text{CE}} = V_{IL}$ |
| $\overline{\text{OE}}/V_{PP}$ Current, program | — | I_{PP2} | — | 25 | mA | |
| A9 Product Identification | — | V_{ID} | 11.5 | 12.5 | V | |

Note 1: V_{CC} must be applied simultaneously or before V_{PP} voltage on $\overline{\text{OE}}/V_{PP}$ and removed simultaneously or after the V_{PP} voltage on $\overline{\text{OE}}/V_{PP}$.

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

| for Program, Program Verify and Program Inhibit Modes | | AC Testing Waveform: $V_{IH}=2.4\text{V}$ and $V_{IL}=0.45\text{V}$; $V_{OH}=2.0\text{V}$; $V_{OL}=0.8\text{V}$ Ambient Temperature: $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ $V_{CC} = 6.5\text{V} \pm 0.25\text{V}$, $\overline{\text{OE}}/V_{PP} = V_H = 13.0\text{V} \pm 0.25\text{V}$ | | | | |
|--|--------|---|------|---------------|---------------------------|--|
| Parameter | Symbol | Min. | Max. | Units | Remarks | |
| Address Set-Up Time | tAS | 2 | — | μs | | |
| Data Set-Up Time | tDS | 2 | — | μs | | |
| Data Hold Time | tDH | 2 | — | μs | | |
| Address Hold Time | tAH | 0 | — | μs | | |
| Float Delay (2) | tDF | 0 | 130 | ns | | |
| VCC Set-Up Time | tVCS | 2 | — | μs | | |
| Program Pulse Width (1) | tPW | 95 | 105 | μs | 100 μs typical | |
| $\overline{\text{CE}}$ Set-Up Time | tCES | 2 | — | μs | | |
| $\overline{\text{OE}}$ Set-Up Time | tOES | 2 | — | μs | | |
| $\overline{\text{OE}}$ Hold Time | tOEH | 2 | — | μs | | |
| $\overline{\text{OE}}$ Recovery Time | tOR | 2 | — | μs | | |
| $\overline{\text{OE}}/V_{PP}$ Rise Time During Programming | tPRT | 50 | — | ns | | |

Note 1: For express algorithm, initial programming width tolerance is 100 $\mu\text{s} \pm 5\%$.

2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS (1)

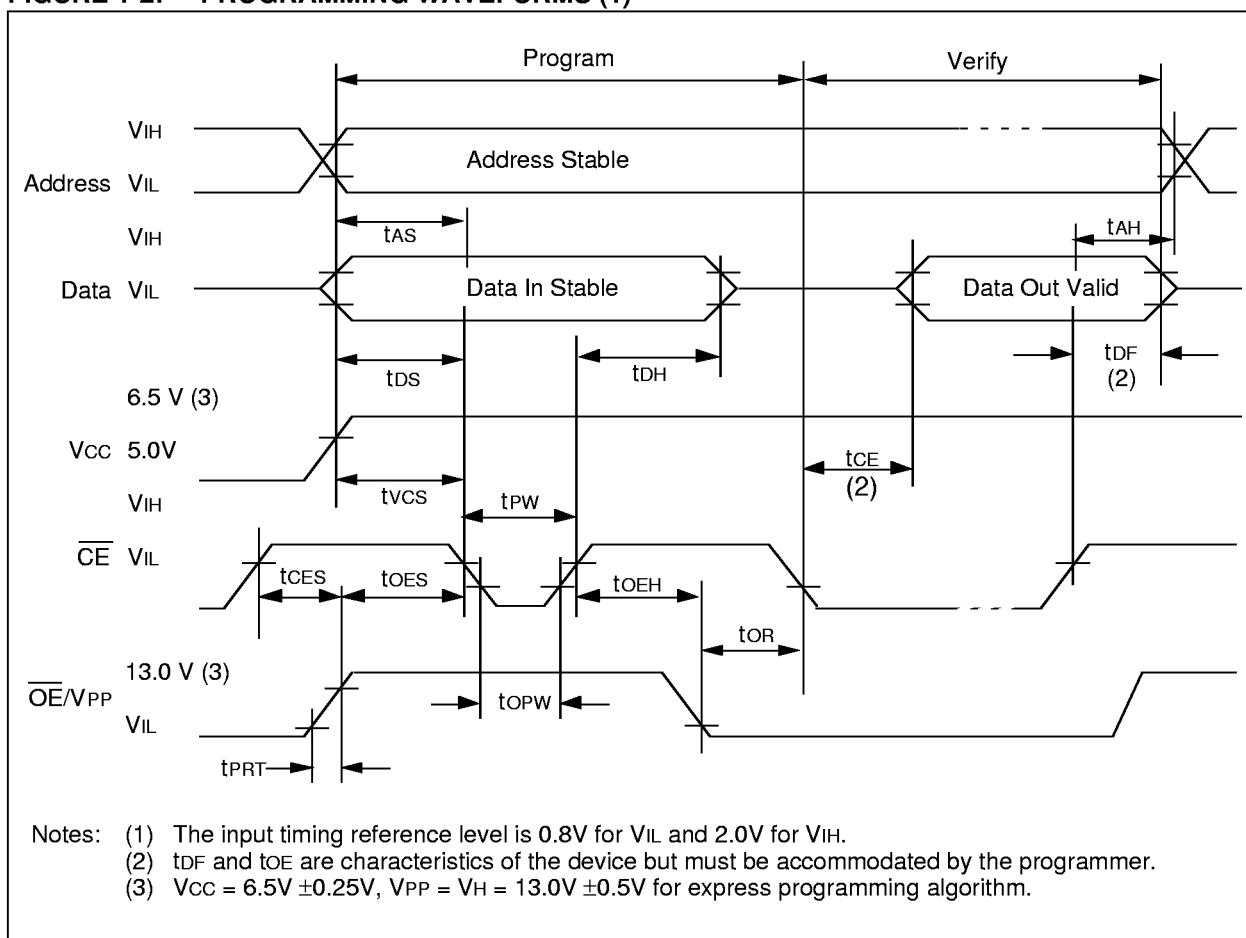


TABLE 1-6: MODES

| Operation Mode | CE | OE/VPP | A9 | O0 - O7 |
|-----------------|-----|--------|----|---------------|
| Read | VIL | VIL | X | DOUT |
| Program | VIL | VH | X | DIN |
| Program Verify | VIL | VIL | X | DOUT |
| Program Inhibit | VIH | VH | X | High Z |
| Standby | VIH | X | X | High Z |
| Output Disable | VIL | VIH | X | High Z |
| Identity | VIL | VIL | VH | Identity Code |

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

- the CE pin is low to power up (enable) the chip
- the OE/VPP pin is low to gate the data to the output pins

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from CE to output (tCE). Data is transferred to the output after a delay (tOE) from the falling edge of OE/VPP.

1.3 Standby Mode

The standby mode is entered when the \overline{CE} pin is high, and the program mode is not identified.

When this conditions are met, the supply current will drop from 25 mA to 30 μ A.

1.4 Output Enable \overline{OE}/VPP

This multifunction pin eliminates bus connection in multiple bus microprocessor systems and the outputs go to high impedance when:

- the \overline{OE}/VPP pin is high (V_{IH}).

When a V_H input is applied to this pin, it supplies the programming voltage (V_{PP}) to the device.

1.5 Erase Mode (UV Windowed Versions)

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1's" state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/ cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000 mW/cm^2 for approximately 40 minutes.

1.6 Programming Mode

The Express algorithm must be used for best results. It has been developed to improve programming yields and throughput times in a production environment. Up to 10 100-microsecond pulses are applied until the byte is verified. A flowchart of the Express algorithm is shown in Figure 1-3.

Programming takes place when:

- V_{CC} is brought to the proper voltage,
- \overline{OE}/VPP is brought to the proper V_H level, and
- \overline{CE} line is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0 - A15 and the data to be programmed is presented to pins O0 - O7. When data and address are stable, a low going pulse on the \overline{CE} line programs that location.

1.7 Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

- V_{CC} is at the proper level,
- the \overline{OE}/VPP pin is low, and
- the \overline{CE} line is low.

1.8 Inhibit

When programming multiple devices in parallel with different data, only \overline{CE} needs to be under separate control to each device. By pulsing the \overline{CE} line low on a particular device, that device will be programmed; all other devices with \overline{CE} held high will not be programmed with the data (although address and data will be available on their input pins).

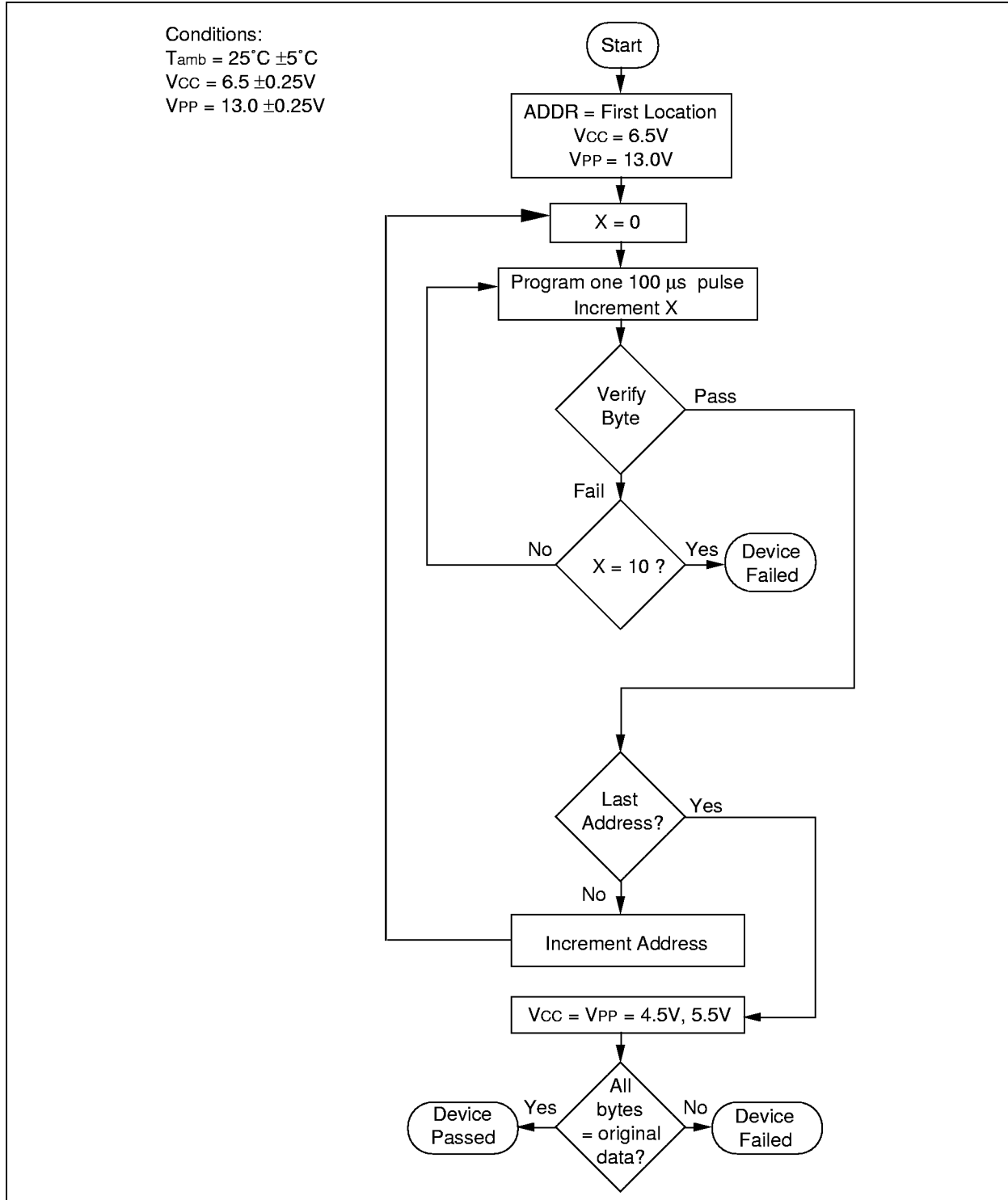
1.9 Identity Mode

In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc. and the device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The \overline{CE} and \overline{OE}/VPP lines must be at V_{IL} . A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

| Pin \rightarrow | Input | Output | | | | | | | | |
|--------------------------|----------|--------|---|---|---|---|---|---|---|-------------|
| Identity \downarrow | A0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | H e x |
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Manufacturer | V_{IL} | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 29 |
| Device Type* | V_{IH} | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0D |

* Code subject to change

FIGURE 1-3: PROGRAMMING EXPRESS ALGORITHM



27C512A

NOTES:

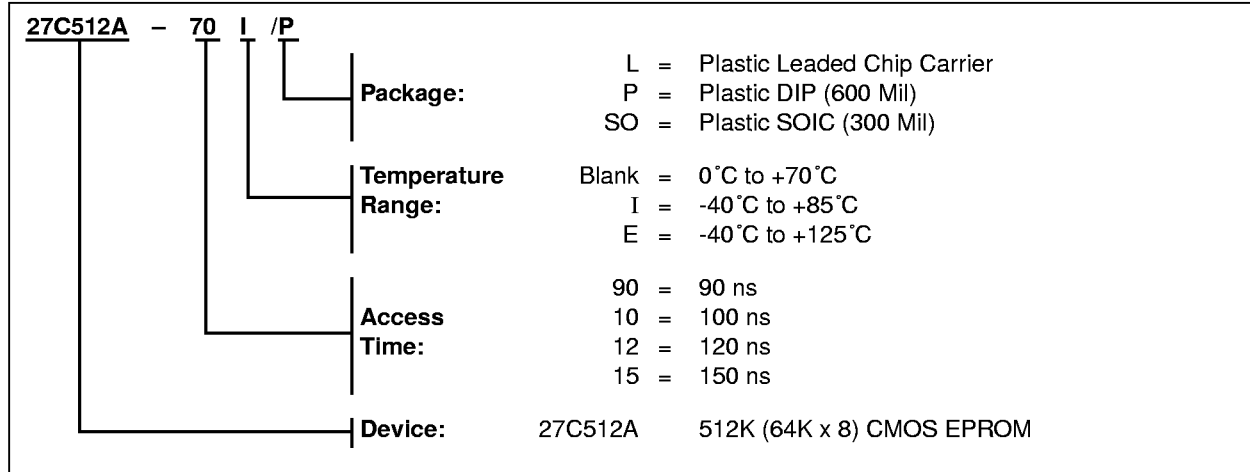
NOTES:

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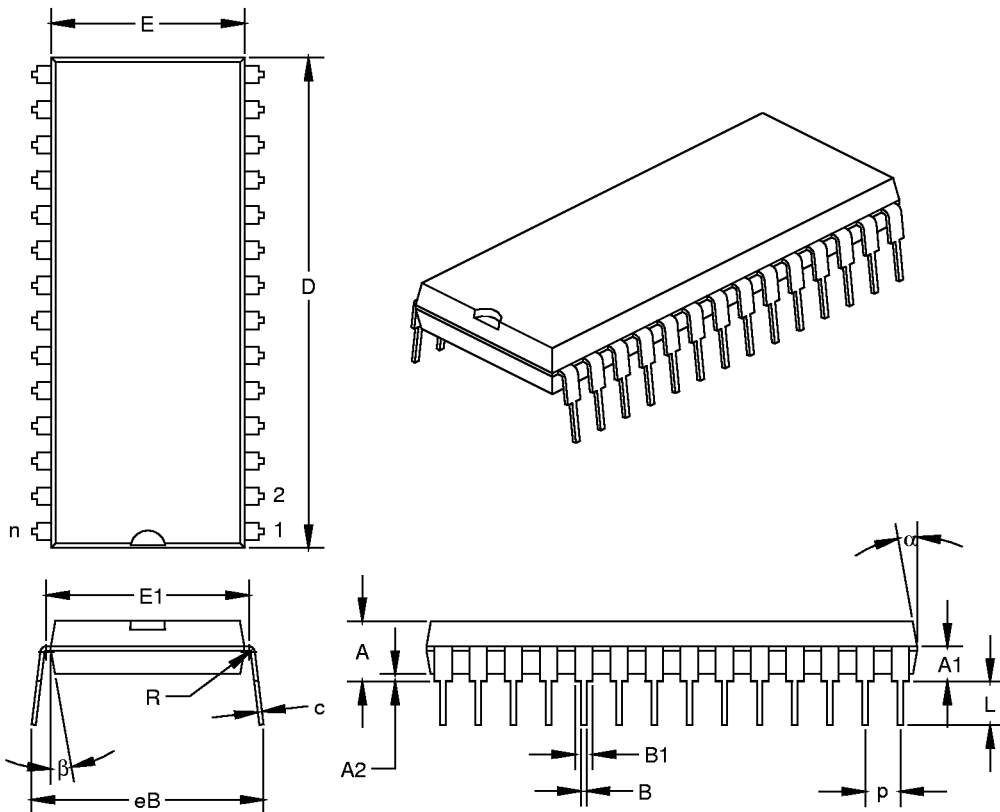
27C512A Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use listed part numbers, and refer to factory or listed sales offices.



Packaging Diagrams and Parameters

Package Type: K04-079 28-Lead Plastic Dual In-line (P) – 600 mil



| Units | | INCHES* | | | MILLIMETERS | | |
|------------------------------|-----------------|---------|-------|-------|-------------|-------|-------|
| | | MIN | NOM | MAX | MIN | NOM | MAX |
| Dimension Limits | | | | | | | |
| PCB Row Spacing | | | 0.600 | | | 15.24 | |
| Number of Pins | n | | 28 | | | 28 | |
| Pitch | p | | 0.100 | | | 2.54 | |
| Lower Lead Width | B | 0.014 | 0.016 | 0.018 | 0.36 | 0.41 | 0.46 |
| Upper Lead Width | B1 [†] | 0.040 | 0.050 | 0.060 | 1.02 | 1.27 | 1.52 |
| Shoulder Radius | R | 0.000 | 0.005 | 0.010 | 0.00 | 0.13 | 0.25 |
| Lead Thickness | c | 0.008 | 0.012 | 0.015 | 0.20 | 0.29 | 0.38 |
| Top to Seating Plane | A | 0.160 | 0.173 | 0.185 | 4.06 | 4.38 | 4.70 |
| Top of Lead to Seating Plane | A1 | 0.081 | 0.101 | 0.121 | 2.04 | 2.55 | 3.06 |
| Base to Seating Plane | A2 | 0.015 | 0.023 | 0.030 | 0.38 | 0.57 | 0.76 |
| Tip to Seating Plane | L | 0.115 | 0.125 | 0.135 | 2.92 | 3.18 | 3.43 |
| Package Length | D [‡] | 1.380 | 1.395 | 1.465 | 35.05 | 35.43 | 37.20 |
| Molded Package Width | E [‡] | 0.505 | 0.550 | 0.555 | 12.80 | 13.97 | 14.10 |
| Radius to Radius Width | E1 | 0.567 | 0.577 | 0.587 | 14.40 | 14.66 | 14.91 |
| Overall Row Spacing | eB | 0.640 | 0.660 | 0.680 | 16.26 | 16.76 | 17.27 |
| Mold Draft Angle Top | α | 5 | 10 | 15 | 5 | 10 | 15 |
| Mold Draft Angle Bottom | β | 5 | 10 | 15 | 5 | 10 | 15 |

* Controlling Parameter.

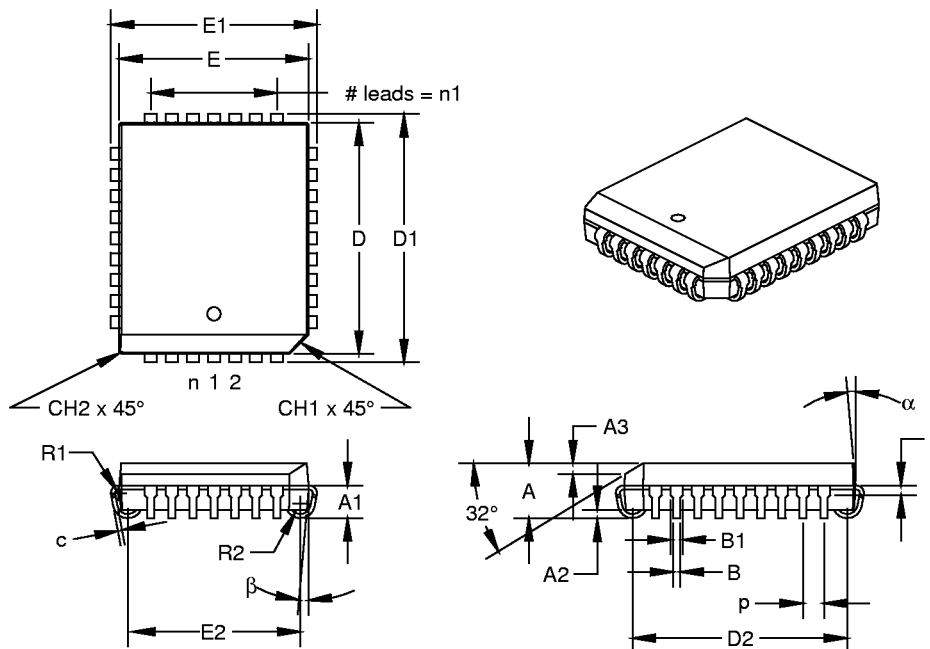
[†] Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

[‡] Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-011 AB

Packaging Diagrams and Parameters

Package Type: K04-023 32-Lead Plastic Leaded Chip Carrier (L) – Rectangle



| Units | | INCHES* | | | MILLIMETERS | | |
|-------------------------|-----------------|---------|-------|-------|-------------|-------|-------|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 32 | | | 32 | |
| Pitch | p | | 0.050 | | | 1.27 | |
| Overall Pack. Height | A | 0.127 | 0.131 | 0.135 | 3.23 | 3.33 | 3.43 |
| Shoulder Height | A1 | 0.060 | 0.078 | 0.095 | 1.52 | 1.97 | 2.41 |
| Standoff | A2 | 0.015 | 0.020 | 0.025 | 0.38 | 0.51 | 0.64 |
| Side 1 Chamfer Dim. | A3 | 0.021 | 0.026 | 0.031 | 0.53 | 0.66 | 0.79 |
| Corner Chamfer (1) | CH1 | 0.035 | 0.045 | 0.055 | 0.89 | 1.14 | 1.40 |
| Corner Chamfer (other) | CH2 | 0.000 | 0.005 | 0.010 | 0.00 | 0.13 | 0.25 |
| Overall Pack. Width | E1 | 0.485 | 0.490 | 0.495 | 12.32 | 12.45 | 12.57 |
| Overall Pack. Length | D1 | 0.585 | 0.590 | 0.595 | 14.86 | 14.99 | 15.11 |
| Molded Pack. Width | E [‡] | 0.447 | 0.450 | 0.453 | 11.35 | 11.43 | 11.51 |
| Molded Pack. Length | D [‡] | 0.547 | 0.550 | 0.553 | 13.89 | 13.97 | 14.05 |
| Footprint Width | E2 | 0.380 | 0.410 | 0.440 | 9.65 | 10.41 | 11.18 |
| Footprint Length | D2 | 0.480 | 0.510 | 0.540 | 12.19 | 12.95 | 13.72 |
| Pins along Width | n1 | | 7 | | | 7 | |
| Lead Thickness | c | 0.008 | 0.010 | 0.012 | 0.20 | 0.25 | 0.30 |
| Upper Lead Width | B1 [†] | 0.026 | 0.029 | 0.032 | 0.66 | 0.74 | 0.81 |
| Lower Lead Width | B | 0.013 | 0.017 | 0.021 | 0.33 | 0.43 | 0.53 |
| Upper Lead Length | L | 0.010 | 0.020 | 0.030 | 0.25 | 0.51 | 0.76 |
| Shoulder Inside Radius | R1 | 0.003 | 0.008 | 0.013 | 0.08 | 0.20 | 0.33 |
| J-Bend Inside Radius | R2 | 0.020 | 0.025 | 0.030 | 0.51 | 0.64 | 0.76 |
| Mold Draft Angle Top | α | 0 | 5 | 10 | 0 | 5 | 10 |
| Mold Draft Angle Bottom | β | 0 | 5 | 10 | 0 | 5 | 10 |

* Controlling Parameter.

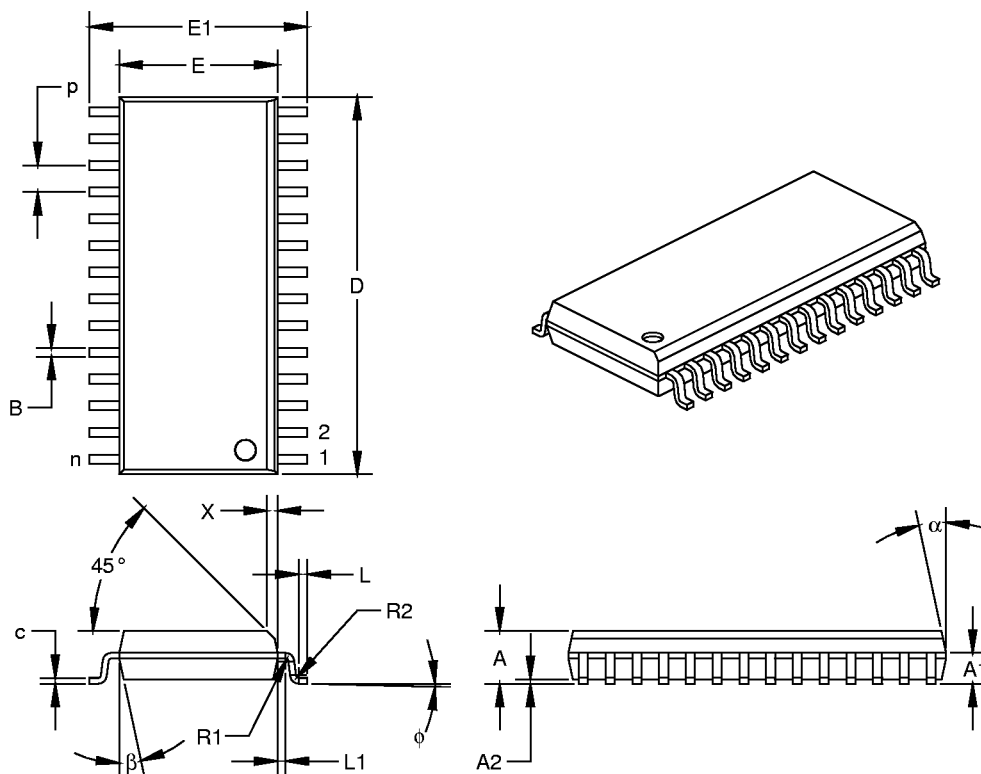
† Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-016 AE

Packaging Diagrams and Parameters

Package Type: K04-052 28-Lead Plastic Small Outline (SO) – Wide, 300 mil



| Units | | INCHES* | | | MILLIMETERS | | |
|-------------------------|----------------|---------|-------|-------|-------------|-------|-------|
| | | MIN | NOM | MAX | MIN | NOM | MAX |
| Pitch | p | | 0.050 | | | 1.27 | |
| Number of Pins | n | | 28 | | | 28 | |
| Overall Pack. Height | A | 0.093 | 0.099 | 0.104 | 2.36 | 2.50 | 2.64 |
| Shoulder Height | A1 | 0.048 | 0.058 | 0.068 | 1.22 | 1.47 | 1.73 |
| Standoff | A2 | 0.004 | 0.008 | 0.011 | 0.10 | 0.19 | 0.28 |
| Molded Package Length | D [‡] | 0.700 | 0.706 | 0.712 | 17.78 | 17.93 | 18.08 |
| Molded Package Width | E [‡] | 0.292 | 0.296 | 0.299 | 7.42 | 7.51 | 7.59 |
| Outside Dimension | E1 | 0.394 | 0.407 | 0.419 | 10.01 | 10.33 | 10.64 |
| Chamfer Distance | X | 0.010 | 0.020 | 0.029 | 0.25 | 0.50 | 0.74 |
| Shoulder Radius | R1 | 0.005 | 0.005 | 0.010 | 0.13 | 0.13 | 0.25 |
| Gull Wing Radius | R2 | 0.005 | 0.005 | 0.010 | 0.13 | 0.13 | 0.25 |
| Foot Length | L | 0.011 | 0.016 | 0.021 | 0.28 | 0.41 | 0.53 |
| Foot Angle | φ | 0 | 4 | 8 | 0 | 4 | 8 |
| Radius Centerline | L1 | 0.010 | 0.015 | 0.020 | 0.25 | 0.38 | 0.51 |
| Lead Thickness | c | 0.009 | 0.011 | 0.012 | 0.23 | 0.27 | 0.30 |
| Lower Lead Width | B [†] | 0.014 | 0.017 | 0.019 | 0.36 | 0.42 | 0.48 |
| Mold Draft Angle Top | α | 0 | 12 | 15 | 0 | 12 | 15 |
| Mold Draft Angle Bottom | β | 0 | 12 | 15 | 0 | 12 | 15 |

* Controlling Parameter.

† Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡ Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

JEDEC equivalent: MS-013 AE