

# ±15kV ESD-Protected, Low-Voltage, SPDT/SPST, CMOS Analog Switches

## General Description

The MAX4561/MAX4568/MAX4569 are low-voltage, ESD-protected analog switches. The normally open (NO) and normally closed (NC) inputs are protected against ±15kV electrostatic discharge (ESD) without latchup or damage, and the COM input is protected against 2.5kV ESD.

These switches operate from a single +1.8V to +12V supply. The 70Ω at 5V (120Ω at 3V) on-resistance is matched between channels to 2Ω max, and is flat (4Ω max) over the specified signal range. The switches can handle Rail-to-Rail® analog signals. Off-leakage current is only 0.5nA at +25°C and 5nA at +85°C. The digital input has +0.8V to +2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a single +5V supply. The MAX4561 is a single-pole/double-throw (SPDT) switch. The MAX4568 NO and MAX4569 NC are single-pole/single-throw (SPST) switches.

The MAX4561 is available in a 6-pin SOT23 package, and the MAX4568/MAX4569 are available in 5-pin SOT23 packages.

## Applications

High-ESD Environments  
 Battery-Powered Systems  
 Audio and Video Signal Routing  
 Low-Voltage Data-Acquisition Systems  
 Sample-and-Hold Circuits  
 Communications Circuits

*Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.*

## Features

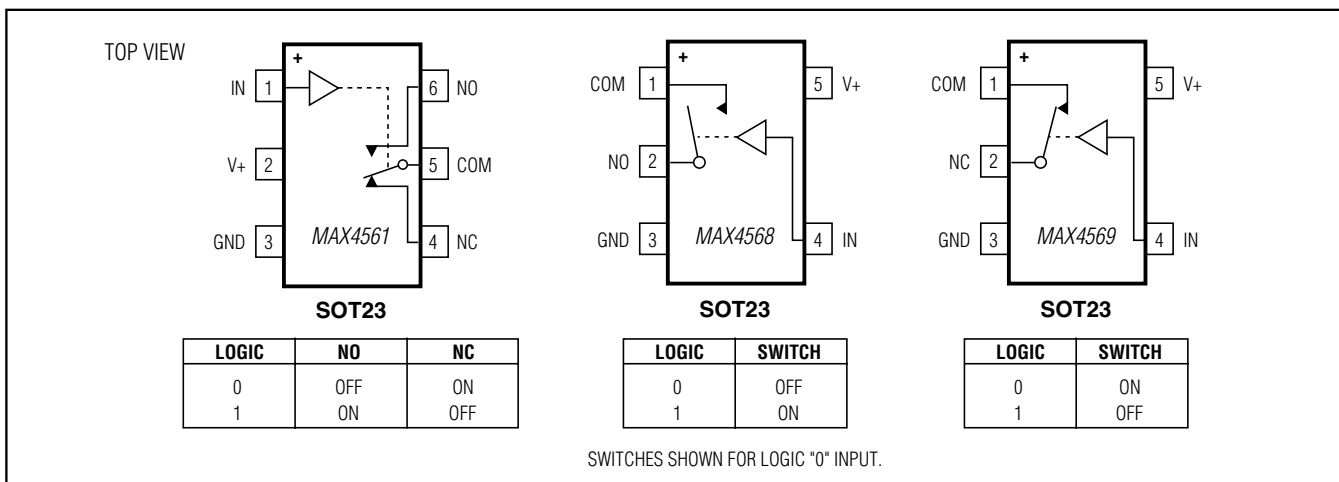
- ◆ ESD-Protected NO, NC
  - ±15kV—Human Body Model
  - ±15kV—IEC 1000-4-2, Air-Gap Discharge
  - ±8kV—IEC 1000-4-2, Contact Discharge
- ◆ Guaranteed On-Resistance
  - 70Ω +5V Supply
  - 120Ω with Single +3V Supply
- ◆ On-Resistance Match Between Channels (2Ω max)
- ◆ Low On-Resistance Flatness: 4Ω max
- ◆ Guaranteed Low Leakage Currents
  - 0.5nA Off-Leakage (at T<sub>A</sub> = +25°C)
  - 0.5nA On-Leakage (at T<sub>A</sub> = +25°C)
- ◆ Guaranteed Break-Before-Make at 5ns (MAX4561 only)
- ◆ Rail-to-Rail Signal Handling Capability
- ◆ TTL/CMOS-Logic Compatible with +5V Supplies
- ◆ Industry Standard Pin-Outs
  - MAX4561 Pin Compatible with MAX4544
  - MAX4568/MAX4569 Pin Compatible with MAX4514/MAX4515

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4561EUT+T	-40°C to +85°C	6 SOT23	AAIE
MAX4568EUK+T	-40°C to +85°C	5 SOT23	ADOE
MAX4569EUK+T	-40°C to +85°C	5 SOT23	ADOF

+ Denotes a lead(Pb)-free/RoHS-compliant package.  
 T = Tape and reel.

## Pin Configurations/Functional Diagrams/Truth Tables



# ±15kV ESD-Protected, Low-Voltage, SPDT/SPST, CMOS Analog Switches

## ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3 to +13V  
 IN, COM, NO, NC to GND (Note 1) .....-0.3V to (V+ + 0.3V)  
 Continuous Current (any terminal).....±10mA  
 Peak Current  
 (NO, NC, COM; pulsed at 1ms 10% duty cycle).....±30mA  
 ESD Protection per Method IEC 1000-4-2 (NO, NC)  
 Air-Gap Discharge .....±15kV  
 Contact Discharge .....±8kV  
 ESD Protection per Method 3015.7  
 V+, GND, IN, COM.....±2.5kV

NO, NC.....±15kV  
 Continuous Power Dissipation (T<sub>A</sub> = +70°C)  
 5-Pin SOT23 (derate 3.1mW/°C above +70°C) .....247mW  
 6-Pin SOT23 (derate 8.7mW/°C above +70°C).....696mW  
 Operating Temperature Range .....-40°C to +85°C  
 Storage Temperature Range .....-65°C to +150°C  
 Lead Temperature (soldering, 10s) .....+300°C  
 Soldering Temperature (reflow) .....+260°C

**Note 1:** Signals on NO, NC, COM, or IN exceeding V+ or GND are clamped by internal diodes. Limit forward current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.5V to +5.5V, V<sub>IH</sub> = +2.4V, V<sub>IL</sub> = +0.8V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise specified. Typical values are at T<sub>A</sub> = +25°C.)  
 (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>ANALOG SWITCH</b>							
Input Voltage Range	V <sub>COM</sub> , V <sub>NO</sub> , V <sub>NC</sub>		0		V+	V	
On-Resistance	R <sub>ON</sub>	V+ = 4.5V, I <sub>COM</sub> = 1mA; V <sub>NO</sub> or V <sub>NC</sub> = 1V, 3.5V	T <sub>A</sub> = +25°C		45	70	Ω
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			75	
On-Resistance Match Between Channels (Note 4)	ΔR <sub>ON</sub>	V+ = 4.5V, I <sub>COM</sub> = 1mA; V <sub>NO</sub> or V <sub>NC</sub> = 1V, 3.5V	T <sub>A</sub> = +25°C		0.5	2	Ω
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			3	
On-Resistance Flatness (Note 5)	R <sub>FLAT(ON)</sub>	V+ = 4.5V, I <sub>COM</sub> = 1mA; V <sub>NO</sub> or V <sub>NC</sub> = 1V, 2.25V, 3.5V	T <sub>A</sub> = +25°C		2	4	Ω
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			5	
Off-Leakage Current (NO or NC)	I <sub>NO(OFF)</sub> , I <sub>NC(OFF)</sub>	V+ = 5.5V, V <sub>COM</sub> = 1V, 4.5V; V <sub>NO</sub> or V <sub>NC</sub> = 4.5V, 1V	T <sub>A</sub> = +25°C		-0.5	0.01	nA
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>		-5	5	
COM Off-Leakage Current (MAX4568/MAX4569 only)	I <sub>COM(OFF)</sub>	V+ = 5.5V, V <sub>COM</sub> = 1V, 4.5V; V <sub>NO</sub> or V <sub>NC</sub> = 4.5V, 1V	T <sub>A</sub> = +25°C		-0.5	0.01	nA
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>		-5	5	
COM On-Leakage Current	I <sub>COM(ON)</sub>	V+ = 5.5V, V <sub>COM</sub> = 1V, 4.5V; V <sub>NO</sub> or V <sub>NC</sub> = 1V, 4.5V or unconnected	T <sub>A</sub> = +25°C		-1	1	nA
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>		-10	10	
<b>LOGIC INPUT</b>							
Input Logic High	V <sub>IH</sub>		2.4			V	
Input Logic Low	V <sub>IL</sub>				0.8	V	
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = 0 or V+	-1		1	μA	

# **$\pm 15\text{kV}$ ESD-Protected, Low-Voltage, SPDT/SPST, CMOS Analog Switches**

## **ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)**

( $V_+$  = +4.5V to +5.5V,  $V_{IH}$  = +2.4V,  $V_{IL}$  = +0.8V,  $T_A$  =  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise specified. Typical values are at  $T_A$  = +25°C.)  
(Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>SWITCH DYNAMIC CHARACTERISTICS</b>							
Turn-On Time	$t_{ON}$	$V_{NO}, V_{NC} = 3V, R_L = 300\Omega, C_L = 35\text{pF}$ ; Figure 1	$T_A = +25^\circ\text{C}$		90	150	ns
			$T_A = T_{MIN}$ to $T_{MAX}$			180	
Turn-Off Time	$t_{OFF}$	$V_{NO}, V_{NC} = 3V, R_L = 300\Omega, C_L = 35\text{pF}$ ; Figure 1	$T_A = +25^\circ\text{C}$		40	80	ns
			$T_A = T_{MIN}$ to $T_{MAX}$			100	
Break-Before-Make Delay (MAX4561 only)	$t_{BBM}$	$V_{NO}, V_{NC} = 3V, R_L = 300\Omega, C_L = 35\text{pF}$ ; Figure 2		5	50	ns	
Charge Injection	Q	$V_{GEN} = 2V, C_L = 1.0\text{nF}, R_{GEN} = 0$ ; Figure 3	$T_A = +25^\circ\text{C}$	MAX4561	17	pC	
				MAX4568/9	6		
NO or NC Off Capacitance	$C_{OFF}$	$V_{NO} = V_{NC} = \text{GND}, f = 1\text{MHz}$ ; Figure 4	$T_A = +25^\circ\text{C}$		20	pF	
COM Off-Capacitance (MAX4568/MAX4569 only)	$C_{COM}$	$V_{COM} = \text{GND}, f = 1\text{MHz}$ ; Figure 4	$T_A = +25^\circ\text{C}$		12	pF	
COM On-Capacitance	$C_{COM}$	$V_{COM} = V_{NO}, V_{NC} = \text{GND}, f = 1\text{MHz}$ ; Figure 4	$T_A = +25^\circ\text{C}$	MAX4561	31	pF	
				MAX4568/9	20		
Off-Isolation (Note 6)	$V_{ISO}$	$V_{NO} = V_{NC} = 1V_{RMS}, R_L = 50\Omega, C_L = 5\text{pF}, f = 1\text{MHz}$ ; Figure 5	$T_A = +25^\circ\text{C}$		-75	dB	
Total Harmonic Distortion	THD	$R_L = 600\Omega, 5V_{p-p}, f = 20\text{Hz}$ to $20\text{kHz}$	$T_A = +25^\circ\text{C}$		0.01	%	
ESD SCR Holding Current	$I_H$		$T_A = +25^\circ\text{C}$		110	mA	
			$T_A = +85^\circ\text{C}$		70		
<b>POWER SUPPLY</b>							
Power-Supply Range	$V_+$		1.8		12	V	
Positive Supply Current	$I_+$	$V_+ = 5.5V, V_{IN} = 0$ or $V_+$	$T_A = +25^\circ\text{C}$		0.05	1	$\mu\text{A}$
			$T_A = T_{MIN}$ to $T_{MAX}$			10	

**MAX4561/MAX4568/MAX4569**

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## ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.6V, V<sub>IH</sub> = +2.0V, V<sub>IL</sub> = +0.6V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise specified. Typical values are at T<sub>A</sub> = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>ANALOG SWITCH</b>						
On-Resistance	R <sub>ON</sub>	I <sub>COM</sub> = 1mA, V <sub>NO</sub> or V <sub>NC</sub> = 1.5V, V+ = 2.7V	T <sub>A</sub> = +25°C	75	120	Ω
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>		150	
<b>LOGIC INPUT</b>						
Input Logic High	V <sub>IH</sub>		2.0			V
Input Logic Low	V <sub>IL</sub>				0.6	V
<b>SWITCH DYNAMIC CHARACTERISTICS</b>						
Turn-On Time	t <sub>ON</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 1.5V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Figure 1	T <sub>A</sub> = +25°C	150	250	ns
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>		300	
Turn-Off Time	t <sub>OFF</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 1.5V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Figure 1	T <sub>A</sub> = +25°C	60	100	ns
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>		150	
Break-Before-Make Delay (MAX4561 only)	T <sub>BBM</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 3V, R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35pF, Figure 2	T <sub>A</sub> = +25°C	1.5	80	ns

**Note 2:** The algebraic convention, where the most negative value is a minimum and the most positive value is a maximum, is used in this data sheet.

**Note 3:** Parameters are 100% tested at +25°C and guaranteed by correlation at the full rated temperature.

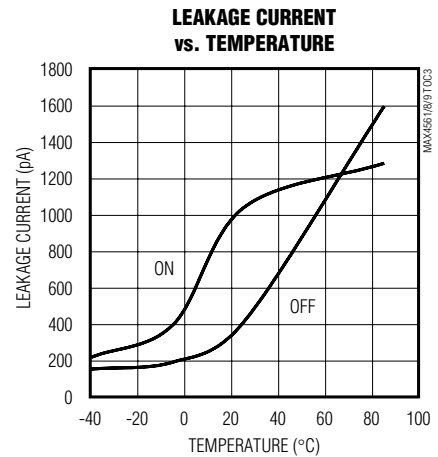
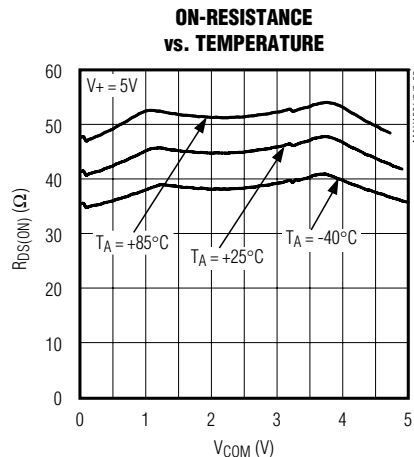
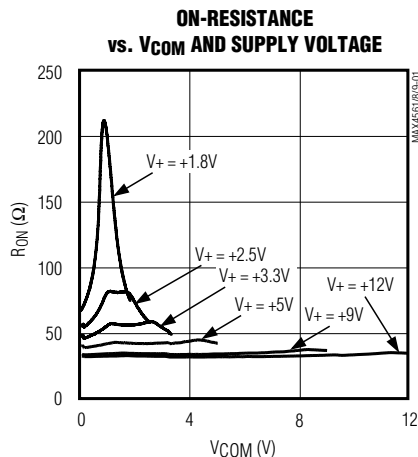
**Note 4:** ΔR<sub>ON</sub> = R<sub>ON</sub>(MAX) - R<sub>ON</sub>(MIN).

**Note 5:** Flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured over the specified analog signal ranges.

**Note 6:** Off-Isolation = 20log<sub>10</sub>(V<sub>COM</sub>/V<sub>NO</sub>), V<sub>COM</sub> = output, V<sub>NO</sub> = input to off switch.

## Typical Operating Characteristics

(T<sub>A</sub> = +25°C, unless otherwise noted.)



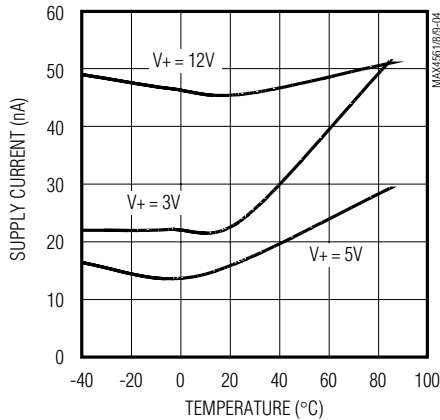
# ±15kV ESD-Protected, Low-Voltage, SPDT/SPST, CMOS Analog Switches

## Typical Operating Characteristics (continued)

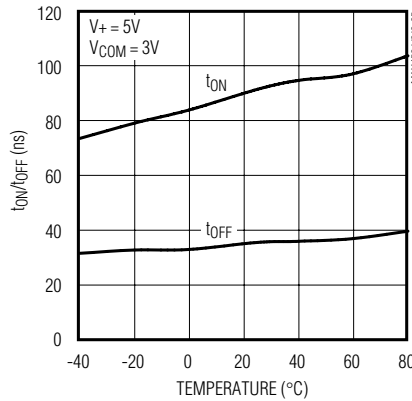
( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

MAX4561/MAX4568/MAX4569

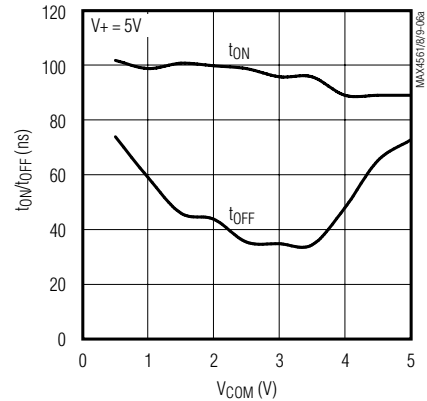
**SUPPLY CURRENT vs. TEMPERATURE AND SUPPLY VOLTAGE**



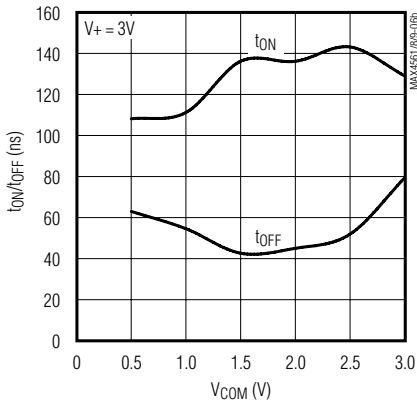
**TURN-ON/TURN-OFF TIME vs. TEMPERATURE**



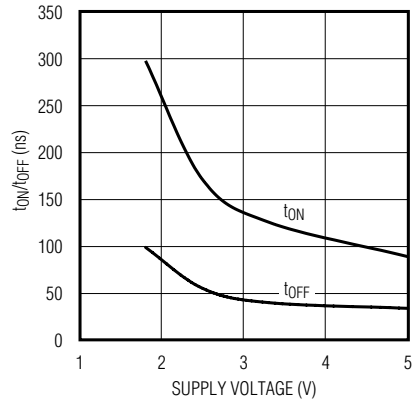
**TURN-ON/TURN-OFF TIME vs. VCOM**



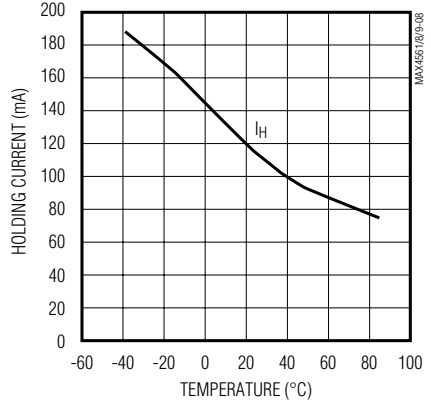
**TURN-ON/TURN-OFF TIME vs. VCOM**



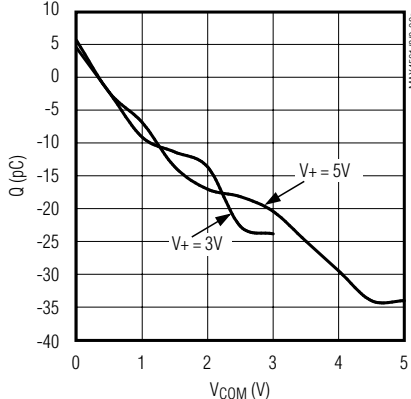
**TURN-ON/TURN-OFF TIME vs. SUPPLY VOLTAGE**



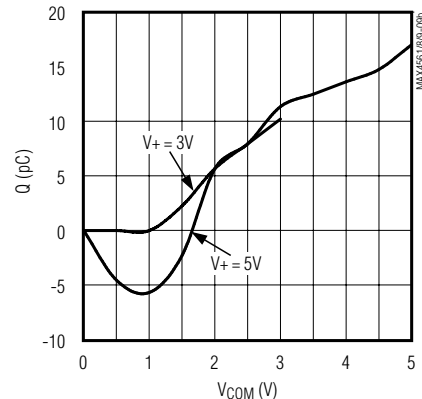
**SCR HOLDING CURRENT vs. TEMPERATURE**



**MAX4561 CHARGE INJECTION vs. VCOM**



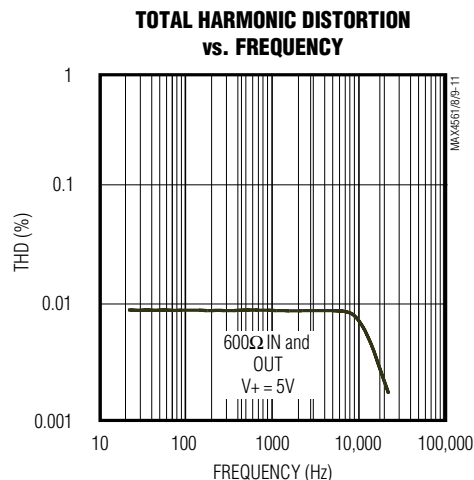
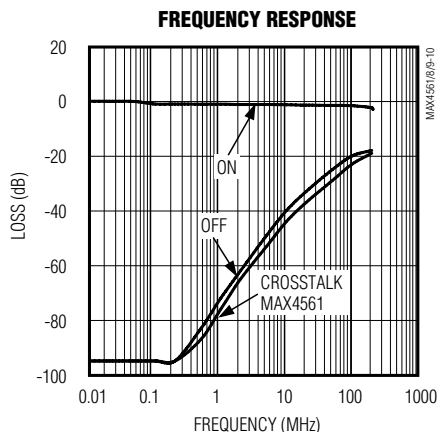
**MAX4568/MAX4569 CHARGE INJECTION vs. VCOM**



# ±15kV ESD-Protected, Low-Voltage, SPDT/SPST, CMOS Analog Switches

## Typical Operating Characteristics (continued)

(T<sub>A</sub> = +25°C, unless otherwise noted.)



## Pin Description

PIN			NAME	FUNCTION
MAX4561	MAX4568	MAX4569		
1	4	4	IN	Logic Control Input
2	5	5	V+	Positive Supply Voltage
3	3	3	GND	Ground
4	–	2	NC	Analog Switch Normally Closed Terminal
5	1	1	COM	Analog Switch Common Terminal
6	2	–	NO	Analog Switch Normally Open Terminal

### Applications Information

Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all CMOS devices. Always sequence V+ on first, followed by the logic inputs, NO/NC, or COM.

### Operating Considerations for High-Voltage Supply

The MAX4561/MAX4568/MAX4569 are capable of +12V single-supply operation with some precautions. The absolute maximum rating for V+ is +13V (referenced to GND). When operating near this region, bypass V+ with a 0.1μF min capacitor to ground as close to the device as possible.

# ±15kV ESD-Protected, Low-Voltage, SPDT/SPST, CMOS Analog Switches

## ±15kV ESD Protection

The MAX4561/MAX4568/MAX4569 are ±15kV ESD-protected at the NC/NO terminals in accordance with IEC1000-4-2. To accomplish this, bidirectional SCRs are included on-chip between these terminals. When the voltages at these terminals go Beyond-the-Rails™, the corresponding SCR turns on in a few nanoseconds and bypasses the surge safely to ground. This method is superior to using diode clamps to the supplies because unless the supplies are very carefully decoupled through low-ESR capacitors, the ESD current through the diode clamp could cause a significant spike in the supplies. This may damage or compromise the reliability of any other chip powered by those same supplies.

There are diodes from NC/NO to the supplies in addition to the SCRs. A resistance in series with each of these diodes limits the current into the supplies during an ESD strike. The diodes protect these terminals from overvoltages that are not a result of ESD strikes. These diodes also protect the device from improper power-supply sequencing.

Once the SCR turns on because of an ESD strike, it remains on until the current through it falls below its “holding current.” The holding current is typically 110mA in the positive direction (current flowing into the NC/NO terminal) at room temperature (see SCR Holding Current vs. Temperature in the *Typical Operating Characteristics*). Design the system so that any sources connected to NC/NO are current-limited to a value below the holding current to ensure the SCR turns off when the ESD event is finished and normal operation resumes. Also, remember that the holding current varies significantly with temperature. The worst case is at +85°C when the holding currents drop to 70mA. Since this is a typical number to guarantee turn-off of the SCRs under all conditions, the sources connected to these terminals should be current-limited to no more than half this value. When the SCR is latched, the voltage across it is approximately 3V. The supply voltages do not affect the holding current appreciably. The sources connected to the COM side of the switches need not be current limited since the switches turn off internally when the corresponding SCR(s) latch.

Even though most of the ESD current flows to GND through the SCRs, a small portion of it goes into V+. Therefore, it is a good idea to bypass the V+ with 0.1µF capacitors directly to the ground plane.

ESD protection can be tested in various ways. Inputs are characterized for protection to the following:

*Beyond-the-Rails is a trademark of Maxim Integrated Products.*

- ±15kV using the Human Body Model
- ±8kV using the Contact Discharge method specified in IEC 1000-4-2 (formerly IEC 801-2)
- ±15kV using the Air-Gap Discharge method specified in IEC 1000-4-2 (formerly IEC 801-2)

## ESD Test Conditions

Contact Maxim Integrated Products for a reliability report that documents test setup, methodology, and results.

## Human Body Model

Figure 6 shows the Human Body Model, and Figure 7 shows the waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which can be discharged into the test device through a 1.5kΩ resistor.

## IEC 1000-4-2

The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX4561 enables the design of equipment that meets Level 4 (the highest level) of IEC 1000-4-2, without additional ESD protection components.

The major difference between tests done using the Human Body Model and IEC 1000-4-2 is higher peak current in IEC 1000-4-2. Because series resistance is lower in the IEC 1000-4-2 ESD test model (Figure 8), the ESD withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 9 shows the current waveform for the ±8kV IEC 1000-4-2 Level 4 ESD Contact Discharge test.

The Air-Gap test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

## Chip Information

PROCESS: CMOS





# ±15kV ESD-Protected, Low-Voltage, SPDT/SPST, CMOS Analog Switches

## Test Circuits/Timing Diagrams (continued)

MAX4561/MAX4568/MAX4569

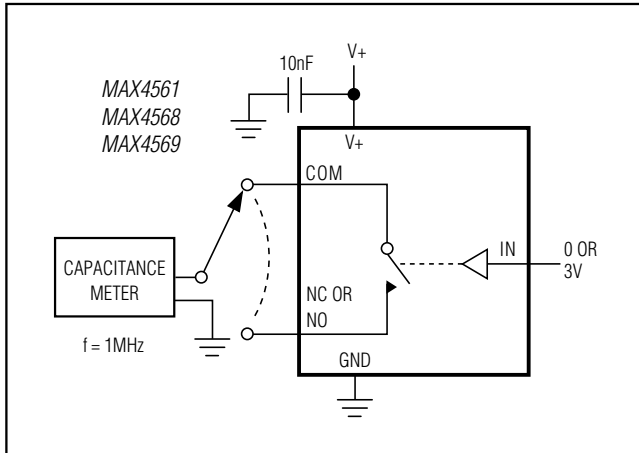


Figure 4. Channel On/Off-Capacitance

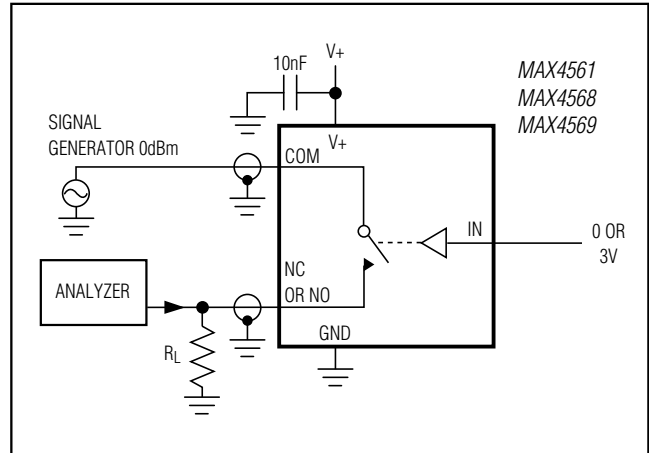


Figure 5. Off-Isolation/On-Channel

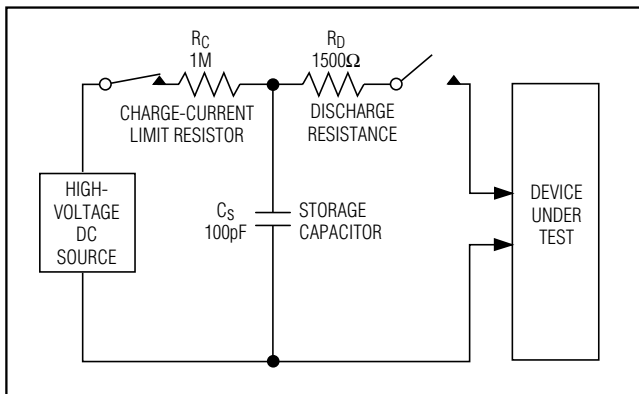


Figure 6. Human Body ESD Test Model

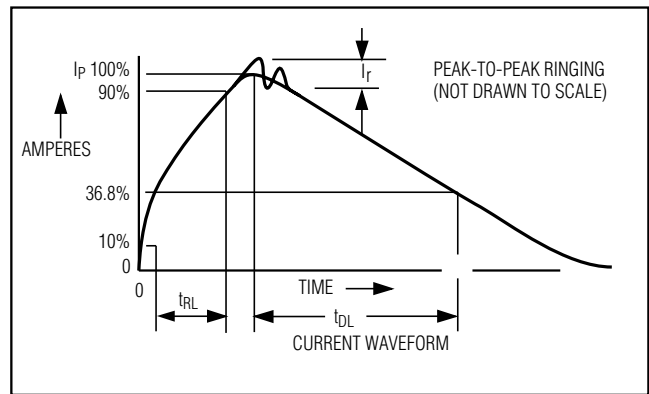


Figure 7. Human Body Model Current Waveform

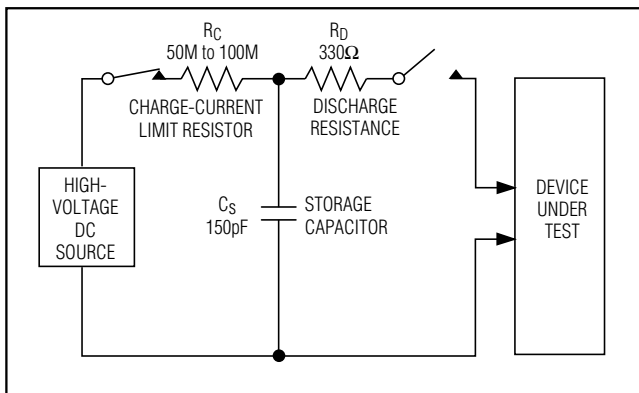


Figure 8. IEC 1000-4-2 ESD Test Model

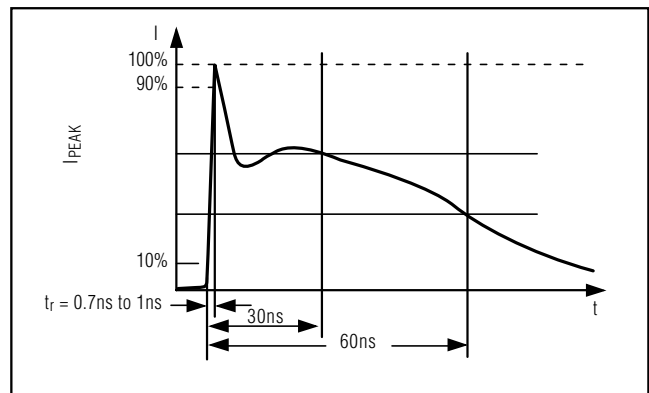


Figure 9. IEC 1000-4-2 ESD Generator Current Waveform

# **±15kV ESD-Protected, Low-Voltage, SPDT/SPST, CMOS Analog Switches**

## **Package Information**

For the latest package outline information and land patterns (footprints), go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

<b>PACKAGE TYPE</b>	<b>PACKAGE CODE</b>	<b>OUTLINE NO.</b>	<b>LAND PATTERN NO.</b>
5 SOT23	U5+2	<a href="#">21-0057</a>	<a href="#">90-0174</a>
6 SOT23	U6SN+1	<a href="#">21-0058</a>	<a href="#">90-0175</a>

# **±15kV ESD-Protected, Low-Voltage, SPDT/SPST, CMOS Analog Switches**

## **Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/00	Initial release	—
1	7/12	Added RoHS packaging option to data sheet	1, 2, 10

**MAX4561/MAX4568/MAX4569**

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