Digital Supervisor

D44TL1A0

for use with VI Chip® BCM Bus Converter Module

Features & Benefits

- PMBus® compatible host interface for enhanced monitoring and control of ChiP BCM Bus Converter Modules
- Interfaces with up to four BCMs through dedicated UART interfaces via Vicor Digital Isolators I13TL1A0 enabling secondary referenced BCM control and telemetry
- OVP, OCP, OTP protection and monitoring
- 10mm x 10mm Land Grid Array (LGA) package

Typical Applications

- 380V_{DC} Power Distribution
- High End Computing Systems
- Automated Test Equipment
- Industrial Systems
- High Density Power Supplies
- Communications Systems
- Transportation

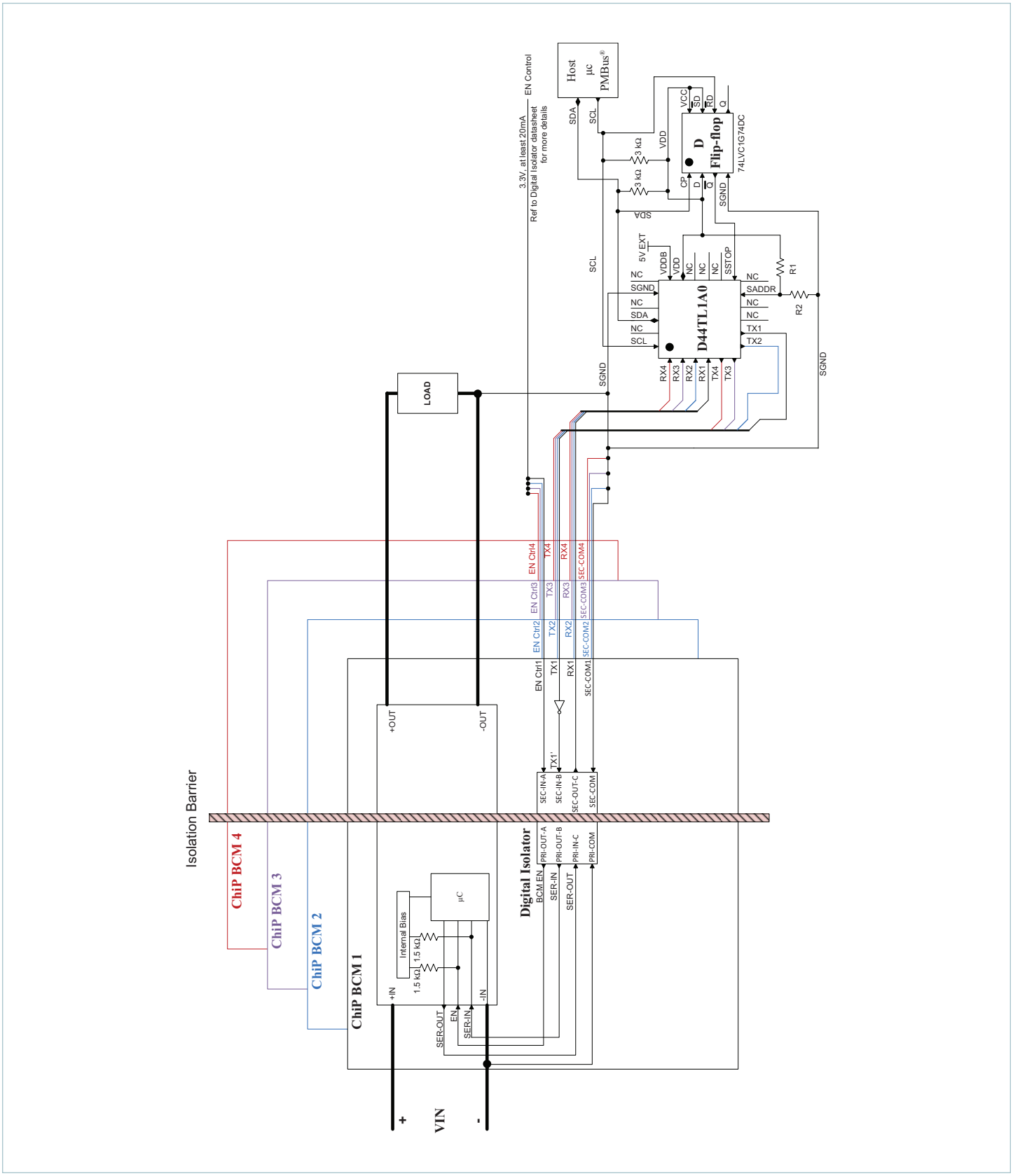
Product Description

The D44TL1A0 is a digital power system supervisor which provides a communication interface between a host processor and up to four ChiP BCM Bus Converter Modules. The Supervisor communicates with a system controller via a PMBus compatible interface. Acting as a communication bridge, the Supervisor communicates with up to four BCM Bus Converter Modules over isolated UART interfaces. Through the D44TL1A0, the host processor can configure, set protection limits, and monitor each BCM.

Standard Models

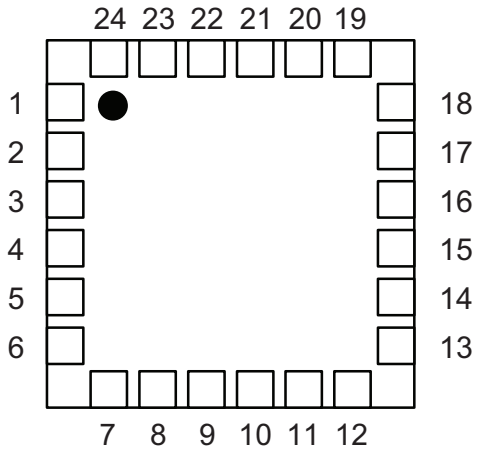
Part Number	Package Type	Temperature
D44TL1A0	LGA (10 x 10mm)	T-Grade (-40°C to 125°C)

Typical Application



Pin Configuration

Top View



10mm x 10mm Land Grid Array (LGA) package

Designator	Signal Name
1	RX4
2	RX3
3	RX2
4	RX1
5	TX4
6	TX3
7	TX2
8	TX1
9	NC
10	NC
11	SADDR
12	NC
13	SSTOP
14	NC
15	NC
16	NC
17	VDD
18	VDDB
19	NC
20	SGND
21	NC
22	SDA
23	NC
24	SCL

Pin Description

PIN Number	Signal Name	PIN Type	Function
1	RX4	INPUT	UART Receiver. Receive data from BCM_4
2	RX3	INPUT	UART Receiver. Receive data from BCM_3
3	RX2	INPUT	UART Receiver. Receive data from BCM_2
4	RX1	INPUT	UART Receiver. Receive data from BCM_1
5	TX4	OUTPUT	UART Transmitter. Send data to BCM_4
6	TX3	OUTPUT	UART Transmitter. Send data to BCM_3
7	TX2	OUTPUT	UART Transmitter. Send data to BCM_2
8	TX1	OUTPUT	UART Transmitter. Send data to BCM_1
11	SADDR	INPUT	I^2C address assignment
13	SSTOP	INPUT	I^2C REPEATED START decoded input Driven by Q-bar output of external D-Flip-flop
17	VDD	POWER	Regulated supply input + 3.3V nominal, used to power internal sub-circuitry Regulated supply output, + 3.3V nominal when Digital Supervisor is powered by VDDB
18	VDDB	POWER	Unregulated supply input
20	SGND	POWER	Signal ground
22	SDA	INPUT / OUTPUT	I^2C Data, PMBus® Compatible
24	SCL	INPUT	I^2C Clock, PMBus Compatible
9	NO CONNECT		
10			
12			
14			
15			
16			
19			
21			
23			

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
VDD		-0.3	4.6	V
I_{VDD}			0.15	A
VDDB		-0.3	17.6	V
RX4, RX3, RX2, RX1		-0.3	4.6	V
TX4, TX3, TX2, TX1		-0.3	V_{VDD_IN} + 0.5	V
SADDR, SSTOP		-0.3	3.6	V
SCL, SDA		-0.3	5.5	V

Signal Characteristics

Specifications apply over the rated supply range (VDD or VDDB), unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

VDD Pin

- Regulated supply power input to the module, required when VDDB is not used to supply power to the device.
- Regulated output 3.3V nominal output when supervisor is powered by VDDB.
- Intended to be used as low current supply for ancillary circuits.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
POWER INPUT	Regular Operation	VDD Voltage input	V_{VDD_IN}		**3.0**	3.3	**3.6**	V
		VDD Current consumption	I_{VDD_IN}				**50**	mA
	Startup	Inrush Current Peak	I_{VDD_INR}	V_{VDD_IN} Slew Rate = 1V/µs		2.5		A
		Turn on time	t_{VDD_ON}	From $V_{VDD\_IN\_MIN}$ to PMBus® active		1.5		ms
POWER OUTPUT	Regular Operation	VDD Voltage output	V_{VDD_OUT}		**3.23**	3.30	**3.37**	V
		VDD source Current	I_{VDD_OUT}				**50**	mA
	Transition	VDD Capacitance (External)	C_{VDD_EXT}				1	µF

VDDB Pin

- Unregulated supply power input, required when VDD is not used as supply.
- This pin is a no connect pin if VDD pin is used to power the device.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
POWER INPUT	Regular Operation	VDDB Voltage	V_{VDDB}		**3.6**		**16**	V
		VDDB Current consumption	I_{VDDB}				**50**	mA
	Startup	Inrush Current Peak	I_{VDDB_INR}	V_{VDDB} Slew Rate = 1V/µs		3.5		A
		Turn on time	t_{VDDB_ON}	From V_{VDDB_MIN} to PMBus active		1.5		ms

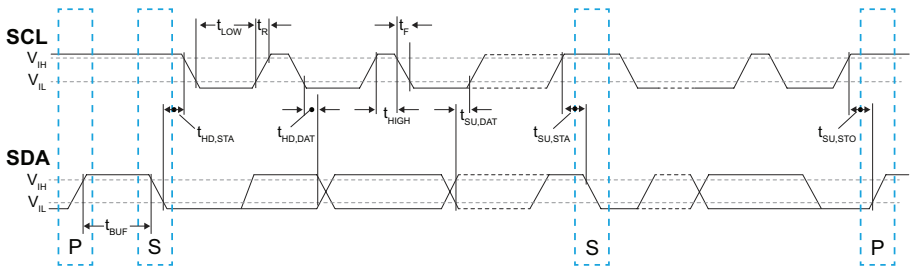
SGND Pin

- Power supply return pin, and reference for all Digital Supervisor signal Input / Output.

Signal Characteristics (Cont.)

Specifications apply over the rated supply range (VDD or VDDB), unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Serial Clock input (SCL) AND Serial Data (SDA) Pins								
• High−power SMBus specification and SMBus physical layer compatible. Note that optional SMBALERT# is signal not supported. • PMBus® command compatible. • The Digital Supervisor requires the use of a flip−flop to drive SSTOP. See system diagram section for more details.								
SIGNAL TYPE	**STATE**	**ATTRIBUTE**	**SYMBOL**	**CONDITIONS / NOTES**	**MIN**	**TYP**	**MAX**	**UNIT**
DIGITAL INPUT/OUTPUT	Regular Operation	**Electrical Parameters**						
		Input Voltage Threshold	V_{IH}	V_{VDD_IN} = 3.3V	2.3			V
			V_{IL}	V_{VDD_IN} = 3.3V			1	V
		Output Voltage Threshold	V_{OH}	V_{VDD_IN} = 3.3V	2.8			V
			V_{OL}	V_{VDD_IN} = 3.3V			0.5	V
		Leakage current	$I_{LEAK-PIN}$	Unpowered device	-10		10	µA
		Signal Sink Current	I_{LOAD}	V_{OL} = 0.4V	4			mA
		Signal Capacitive Load	C_I	Total capacitive load of one device pin			10	pF
		Signal Noise Immunity	V_{NOISE_PP}	10MHz to 100MHz	300			mV
		Timing Parameters						
		Operating Frequency	F_{SMB}	Idle state = 0Hz	10		400	KHz
		Free time between Stop and Start Condition	t_{BUF}		1.3			µs
		Hold time after Start or Repeated Start condition	$t_{HD:STA}$	First clock is generated after this hold time	0.6			µs
		Repeat Start Condition Setup time	$t_{SU:STA}$		0.6			µs
		Stop Condition setup time	$t_{SU:STO}$		0.6			µs
		Data Hold time	$t_{HD:DAT}$		300			ns
		Data Setup time	$t_{SU:DAT}$		100			ns
		Clock low time out	$t_{TIMEOUT}$		25		35	ms
		Clock low period	t_{LOW}		1.3			µs
		Clock high period	t_{HIGH}		0.6		50	µs
		Cumulative clock low extend time	$t_{LOW:SEXT}$				25	ms
		Clock or Data Fall time	t_F	Measured from (V_{IL_MAX} - 0.15) to (V_{IH_MIN} + 0.15)	20		300	ns
		Clock or Data Rise time	t_R	0.9 • $V_{VDD\_IN\_MAX}$ to (V_{IL_MAX} - 0.15)	20		300	ns



Signal Characteristics (Cont.)

Specifications apply over the rated supply range (VDD or VDDB), unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

UART TX / RX Pins

- Universal Asynchronous Receiver/Transmitter (UART) pins.
- Provide intra–system communication to a ChiP Bus Converter Module (BCM).
- The Digital Supervisor requires a Digital Isolator I13TL1A0 in order to communicate to a BCM using the UART pins.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
GENERAL I/O	Regular Operation	Baud Rate	BR_{UART}			750		Kbit/s
DIGITAL INPUT		**RX Receive Pin**						
		RX Input Voltage Threshold	V_{RX_IH}		2.0			V
			V_{RX_IL}				0.8	V
		RX rise time	t_{RX_RISE}	10% to 90%		150		ns
		RX fall time	t_{RX_FALL}	10% to 90%		30		ns
		RX internal R_{PULLUP}	R_{RX_PLP}	Pull up to V_{VDD_IN}		1.5		kΩ
		RX external Capacitance	C_{RX_EXT}				120	pF
DIGITAL OUTPUT		**TX Transmit Pin**						
		TX Output Voltage Threshold	V_{TX_OH}	× = V_{VDD_IN}	× - 0.4			V
			V_{TX_OL}				0.4	V
		TX rise time	t_{TX_RISE}	10% to 90%		150		ns
		TX fall time	t_{TX_FALL}	10% to 90%		30		ns
		TX source current	I_{TX}		-24		24	mA
		TX output impedance	Z_{TX}			12.5		Ω

Serial Address (SADDR) Pin

- The Digital Supervisor supports only a fixed and persistent child address.
- Using a voltage divider from VDD to signal ground.
- The address is sampled during startup and is used until power is reset.
- 16 Addresses are available. Relative to V_{VDD_NOM}, a 206.25mV range per address.

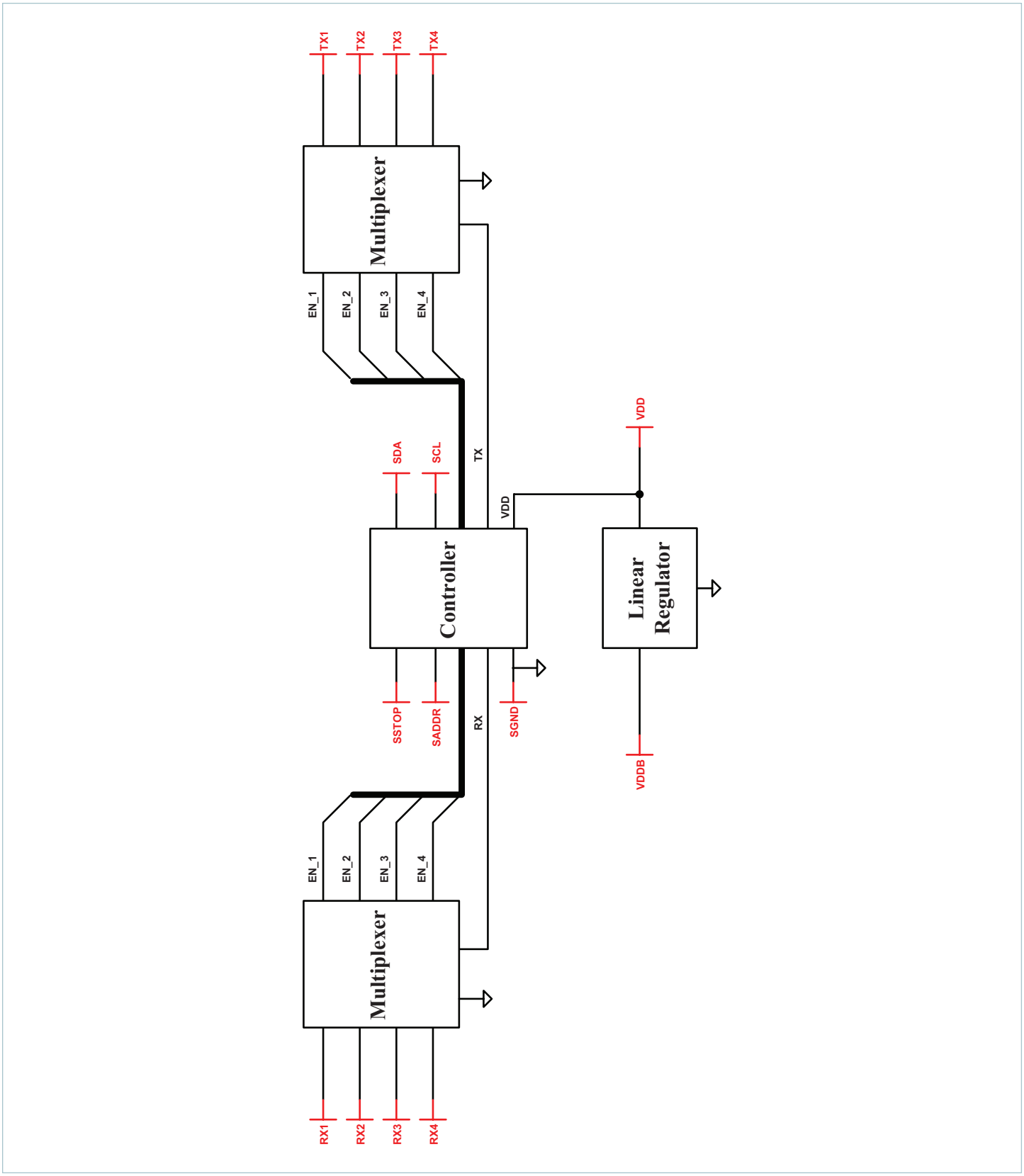
SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
MULTI–LEVEL INPUT	Regular Operation	SADDR Input Voltage	V_{SADDR}	See address section; × = V_{VDD_IN}	0		×	V
		SADDR leakage current	I_{SADDR}	Leakage current			1	µA
	Startup	SADDR registration time	t_{SADDR}	From $V_{VDD\_IN\_MIN}$		1		ms

Serial STOP (SSTOP) Pins

- Input from a Flip-flop to drive SSTOP used to decode a REPEATED START signal. See system diagram section for more details.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
DIGITAL INPUT	Regular Operation	SSTOP Voltage Threshold	V_{SSTOP_IH}	× = V_{VDD_IN}	0.7 • ×			V
			V_{SSTOP_IL}	× = V_{VDD_IN}			0.3 • ×	V

Block Diagram

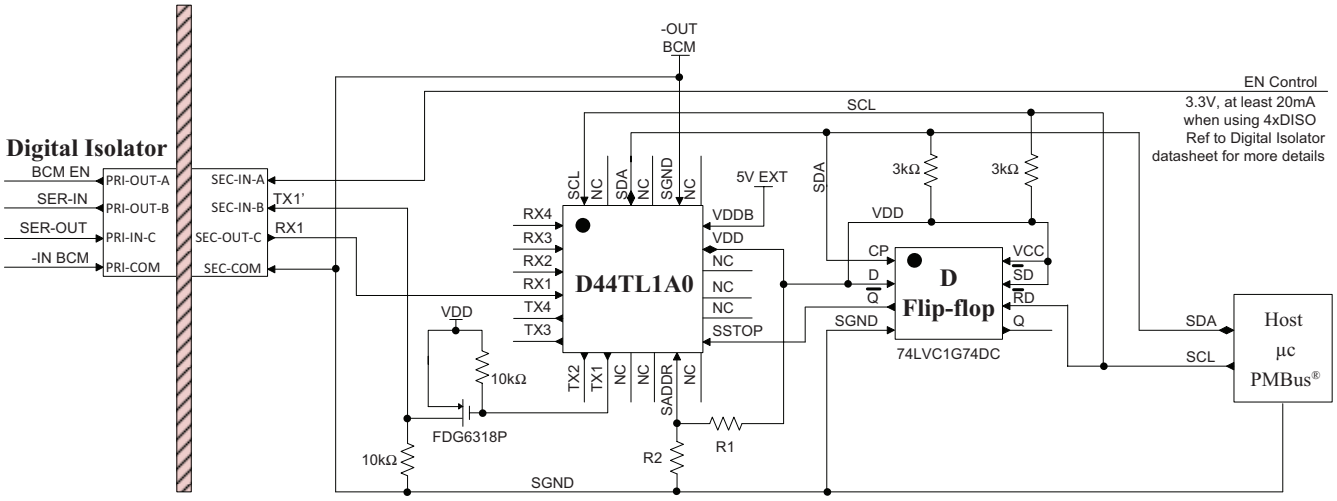


General Characteristics

Specifications apply over the rated supply range (VDD or VDDB), unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L		9.90 / [0.390]	10.00 / [0.394]	10.10 / [0.398]	mm / [in]
Width	W		9.90 / [0.390]	10.00 / [0.394]	10.10 / [0.398]	mm / [in]
Height	H		1.89 / [0.075]	1.97 / [0.078]	2.05 / [0.081]	mm / [in]
Weight	W			0.5 / [0.017]		g / [oz]
Thermal						
Operating temperature	$T_{INTERNAL}$	D44TL1A0 (T-Grade)	-40		125	°C
Assembly						
Storage temperature	T_{ST}	D44TL1A0 (T-Grade)	-40		125	°C
Moisture Sensitivity Level	MSL	MSL4, 72hrs out of bag				
ESD Withstand	ESD_{HBM}	Human Body Model, "AEC Q100-002" > 2000V				
	ESD_{CDM}	Charge Device Model, "AEC Q100-011" > 750V				
	ESD_{MM}	Machine Model, "AEC Q100-003" > 200V				
Soldering						
Peak Temperature During Reflow		Under MSL 4 conditions above	235	245	260	°C
Peak Time Above 217°C			30	60	90	s
Peak Heating Rate During Reflow			0.5	1.5	3.0	°C / s
Peak Cooling Rate Post Reflow			0.5	2.0	6.0	°C / s
Quality / Reliability						
MTBF		MIL–HDBK–217Plus Parts Count – 25°C Ground Benign, Stationary, Indoors / Computer		21.6		MHrs
		Telcordia Issue 2 – Method I Case III; 25°C Ground Benign, Controlled		24.4		

System Functional Description



The Digital Supervisor provides the host system telemetry access to an array of up to four Bus Converter Modules (BCMs). The D44TL1A0 Digital Supervisor is a PMBus® child and will respond only to host commands listed in subsequent sections.

A Single D-type flip-flop is required to signal a STOP condition to a PMBus message.

The Digital Supervisor is a self-powered device as defined by the SMBus specification. The Digital Supervisor has two power input pins. VDDB is a wide range input that powers an internal regulator. When power is applied to VDDB, the VDD pin acts as a 3.3V auxiliary power source. VDD can also be used as a 3.3V nominal power input. In this case, VDDB must be left unconnected.

The TX1, TX2, TX3, TX4 pins of the Digital Supervisor require external buffering in order to fully bias the Digital Isolator channel. All signals are inverted by the Digital Isolator. Please refer to the Digital Isolator datasheet for additional details.

The Digital Isolator allows UART communication interface between the Digital Supervisor and the associated primary referenced BCM UART pins. Each Digital Isolator provides enough signal channels for one BCM. Each transmission channel is able to draw its bias power directly from the input signal being transmitted to the output.

The Digital Supervisor regularly polls the UART interface and stores the BCMs telemetry, faults and warnings. This updated data is then available for access by the host processor via the PMBus interface. BCM reported parameters calibration coefficient and calibration gain are factory set and are stored in individual BCMs ensuring specified telemetry accuracy is met. Refer to the respective BCM datasheet for more details.

A startup order of the Digital Supervisor or the BCM array is not required. The Digital Supervisor is constantly probing all UART pins to discover connected BCMs. Stored telemetry update rate is constant for a given number of BCMs. Worst case telemetry update is 12ms and worst case update of non-volatile parameter after a write command is 200ms.

The PMBus output voltage level setting commands and faults do not apply to the BCM. The BCM during normal operation will provide an output voltage proportional to its transfer ratio referred to as BCM K Factor.

Any available communication enabled BCM may be used with a Digital Supervisor. It is not required for the complete array of four BCMs to be of equivalent K factor in order to report to a single Digital Supervisor.

PMBus® Interface

Refer to "PMBus Power System Management Protocol SpecificationRevision 1.2, Part I and II" for complete PMBus specifications details visit http://pmbus.org.

Device Address

The PMBus address (SADDR Pin) should be set to one of a predetermined 16 possible addresses shown in the table below using a voltage divider from VDD to SGND.

The Digital Supervisor accepts only a fixed and persistent address and does not support SMBus address resolution protocol. At initial power-up, the Digital Supervisor will sample the address pin voltage, and will hold this address until device power is removed.

ID	Child Address	HEX	Recommended Resistor Divider (Ω)	
			R1	R2
1	1010 000b	50h	13700	442
2	1010 001b	51h	13300	1370
3	1010 010b	52h	5760	1070
4	1010 011b	53h	7320	2050
5	1010 100b	54h	7150	2800
6	1010 101b	55h	5230	2740
7	1010 110b	56h	10700	7320
8	1010 111b	57h	16200	14300
9	1011 000b	58h	14300	16200
10	1011 001b	59h	7320	10700
11	1011 010b	5Ah	2740	5230
12	1011 011b	5Bh	5360	13700
13	1011 100b	5Ch	1690	6040
14	1011 101b	5Dh	1070	5760
15	1011 110b	5Eh	1370	13300
16	1011 111b	5Fh	442	13700

BCM Enable Control Pin

The BCM EN Control pin input from host processor can be used to turn the BCM powertrain on and off. The host will need to energize the Digital Isolator channels of all used BCMs.

For a synchronous BCM startup, it is possible to connect all four Digital Isolator pins (SER-IN-A) together. The input pin (SER-IN-A) to the Digital Isolator requires at a minimum 2.5V and N times 5mA per N number of channels driven for proper biasing. The output of each Digital Isolator pin (SER-OUT-A) can then drive the respective BCM EN pin. Refer to the Digital Isolator datasheet for more details.

The BCM EN pin has a higher priority level than the OPERATION COMMAND (01h). The BCM powertrain will remain off if the BCM EN pin is disabled.

Reported DATA Formats

The Digital Supervisor employs a direct data format where all reported Digital Supervisor measurements are in Volts, Amperes, Degrees Celsius, or Seconds. The host uses the following PMBus specification to interpret received values metric prefixes. Note that the Coefficients command is not supported:

$$X = \left(\frac{1}{m}\right) \bullet (Y \bullet 10^{-R} - b)$$

Where:

X, is a "real world" value in units (A, V, °C, s)

Y, is a two's complement integer received from the Digital Supervisor

m, b and R are two's complement integers defined as follows:

Command	Code	m	R	b
TON_DELAY	60h	1	3	0
READ_VIN	88h	1	1	0
READ_IIN	89h	1	3 [3]	0
READ_VOUT [1]	8Bh	1	1	0
READ_IOUT	8Ch	1	2	0
READ_TEMPERATURE_1 [2]	8Dh	1	0	0
READ_POUT	96h	1	0	0
MFR_VIN_MIN	A0h	1	0	0
MFR_VIN_MAX	A1h	1	0	0
MFR_VOUT_MIN	A4h	1	0	0
MFR_VOUT_MAX	A5h	1	0	0
MFR_IOUT_MAX	A6h	1	0	0
MFR_POUT_MAX	A7h	1	0	0
READ_K_FACTOR	D1h	65536	0	0
READ_BCM_ROUT	D4h	1	5	0

[1] Default READ Output Voltage returned when BCM unit is disabled = -300V.
[2] Default READ Temperature returned when BCM unit is disabled = -273°C.
[3] READ_IIN command listed value valid for HV BCM products. Use R = 2 for LV BCM products.

No special formatting is required when lowering the supervisory limits and warnings.

Supported Command List

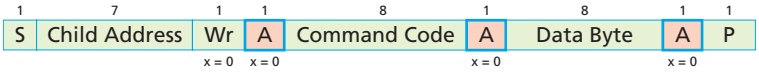
Command	Code	Function	Default Data Content	Data Bytes
PAGE	00h	Access Digital Supervisor stored information for all connected devices	00h	1
OPERATION	01h	Turn BCMs on or off	80h	1
ON_OFF_CONFIG	02h	Defines startup when power is applied as well as immediate on/off control over the BCMs	1Dh	1
CLEAR_FAULTS	03h	Clear all BCM and all Digital Supervisor faults	N/A	None
CAPABILITY	19h	Digital Supervisor PMBus® key capabilities set by factory	20h	1
OT_FAULT_LIMIT	4Fh[1]	BCM over temperature protection	64h	2
OT_WARN_LIMIT	51h[1]	BCM over temperature warning	64h	2
VIN_OV_FAULT_LIMIT	55h[1]	BCM V_{IN} overvoltage warning	64h	2
VIN_OV_WARN_LIMIT	57h[1]	BCM V_{IN} overvoltage protection	64h	2
IIN_OC_FAULT_LIMIT	5Bh[1]	BCM I_{OUT} overcurrent protection	64h	2
IIN_OC_WARN_LIMIT	5Dh[1]	BCM I_{OUT} overcurrent warning	64h	2
TON_DELAY	60h[1]	Startup delay additional to any BCM fixed delays	00h	2
STATUS_BYTE	78h	Summary of BCM faults	00h	1
STATUS_WORD	79h	Summary of BCM fault conditions	00h	2
STATUS_IOUT	7Bh	BCM overcurrent fault status	00h	1
STATUS_INPUT	7Ch	BCM overvoltage and under voltage fault status	00h	1
STATUS_TEMPERATURE	7Dh	BCM over temperature and under temperature fault status	00h	1
STATUS_CML	7Eh	Digital Supervisor PMBus Communication fault	00h	1
STATUS_MFR_SPECIFIC	80h	Other BCM status indicator	00h	1
READ_VIN	88h	BCM input voltage	FFFFh	2
READ_IIN	89h	BCM input current	FFFFh	2
READ_VOUT	8Bh	BCM output voltage	FFFFh	2
READ_IOUT	8Ch	BCM output current	FFFFh	2
READ_TEMPERATURE_1	8Dh	BCM temperature	FFFFh	2
READ_POUT	96h	BCM output power	FFFFh	2
PMBUS_REVISION	98h	Digital Supervisor PMBus compatible revision	22h	1
MFR_ID	99h	Digital Supervisor ID	"VI"	2
MFR_MODEL	9Ah	Digital Supervisor or BCM model	Part Number	18
MFR_REVISION	9Bh	Digital Supervisor or BCM revision	FW and HW revision	18
MFR_LOCATION	9Ch	Digital Supervisor or BCM factory location	"AP"	2
MFR_DATE	9Dh	Digital Supervisor or BCM manufacturing date	"YYWW"	4
MFR_SERIAL	9Eh	Digital Supervisor or BCM serial number	Serial Number	16
MFR_VIN_MIN	A0h	BCM Minimum rated V_{IN}	Varies per BCM	2
MFR_VIN_MAX	A1h	BCM Maximum rated V_{IN}	Varies per BCM	2
MFR_VOUT_MIN	A4h	BCM Minimum rated V_{OUT}	Varies per BCM	2
MFR_VOUT_MAX	A5h	BCM Maximum rated V_{OUT}	Varies per BCM	2
MFR_IOUT_MAX	A6h	BCM Maximum rated I_{OUT}	Varies per BCM	2
MFR_POUT_MAX	A7h	BCM Maximum rated P_{OUT}	Varies per BCM	2
BCM_EN_POLARITY	D0h[1]	Set BCM EN pin polarity	02h	1
READ_K_FACTOR	D1h	BCM K factor	Varies per BCM	2
READ_BCM_ROUT	D4h	BCM R_{OUT}	Varies per BCM	2
SET_ALL_THRESHOLDS	D5h[1]	Set BCM supervisory warning and protection thresholds	646464646464h	6
DISABLE_FAULT	D7h[1]	Disable BCM overvoltage, overcurrent or under voltage supervisory faults	00h	2

[1] The BCM must be in a disabled state during a write message.

Command Structure Overview

Write Byte protocol:

The Host always initiates PMBus® communication with a START bit. All messages are terminated by the Host with a STOP bit. In a write message, the parent sends the child device address followed by a write bit. Once the child acknowledges, the parent proceeds with the command code and then similarly the data byte.



S Start Condition

Sr Repeated start Condition

Rd Read

Wr Write

X Indicated that field is required to have the value of x

A Acknowledge (bit may be 0 for an ACK or 1 for a NACK)

P Stop Condition

From Parent to Child

From Child to Parent

... Continued next line

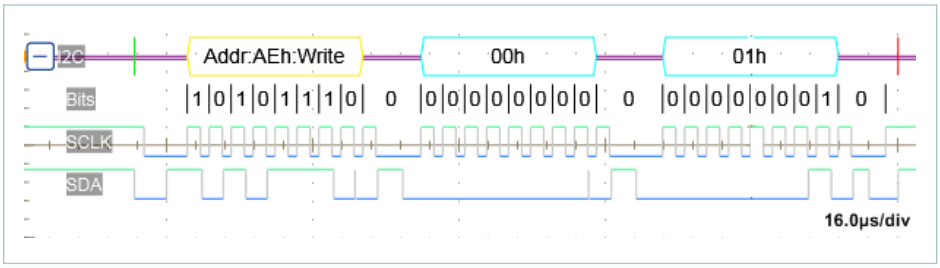
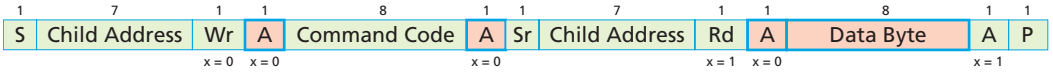


Figure 1 *— PAGE COMMAND (00h), WRITE BYTE PROTOCOL*

Read Byte protocol:

A Read message begins by first sending a Write Command, followed by a REPEATED START Bit and a child Address. After receiving the READ bit, the Digital Supervisor begins transmission of the Data responding to the Command. Once the Host receives the requested Data, it terminates the message with a NACK preceding a stop condition signifying the end of a read transfer.



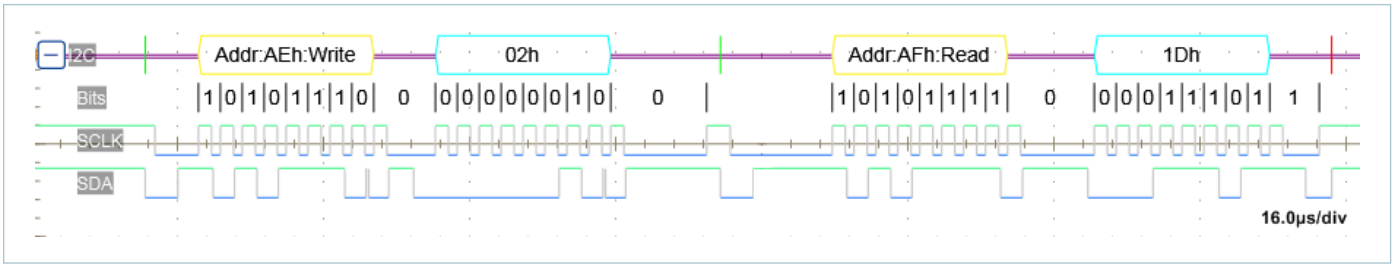


Figure 2 *— ON_OFF_CONFIG COMMAND (02h), READ BYTE PROTOCOL*

Write Word protocol:

When transmitting a word, the lowest order byte leads the highest order byte. Furthermore, when transmitting a Byte, the least significant bit (LSB) is sent last. Refer to System Management Bus (SMBus) specification version 2.0 for more details.

Note: Extended command and Packet Error Checking Protocols are not supported.

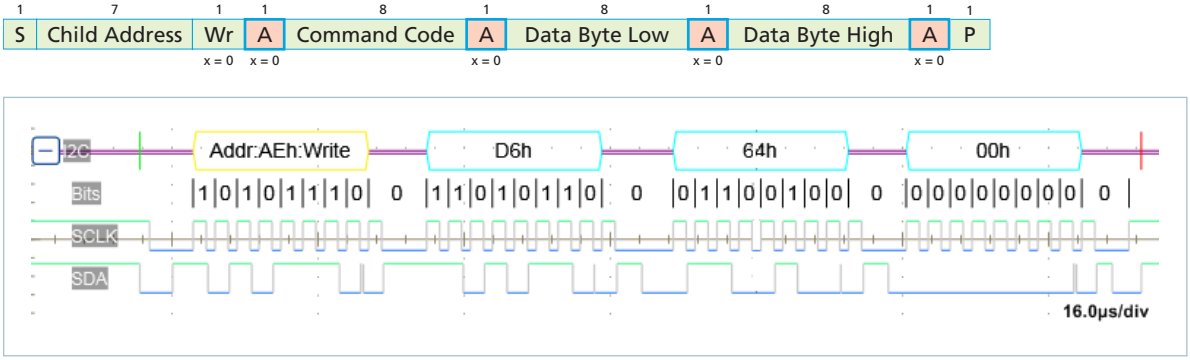


Figure 3 *— TON_DELAY COMMAND (60h)_WRITE WORD PROTOCOL*

Read Word protocol:

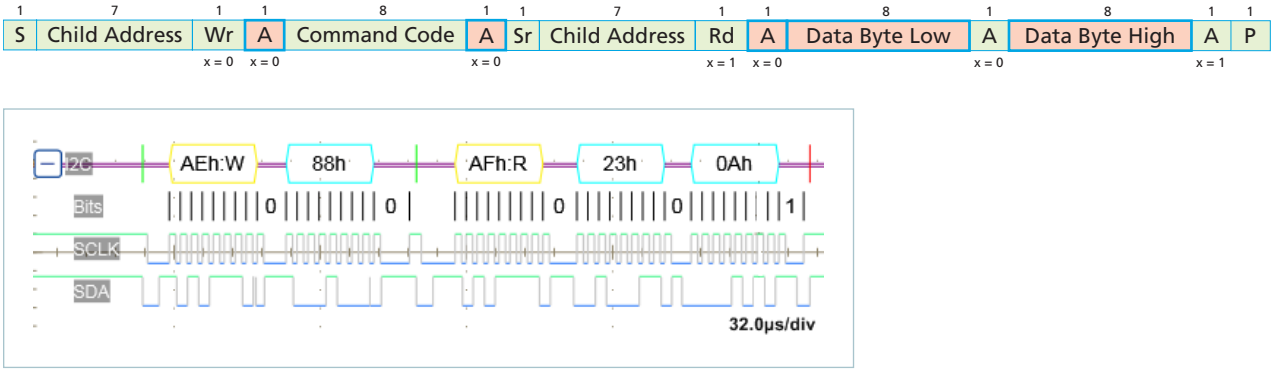


Figure 4 *— MFR_VIN_MIN COMMAND (A0h)_READ WORD PROTOCOL*

Write Block protocol:

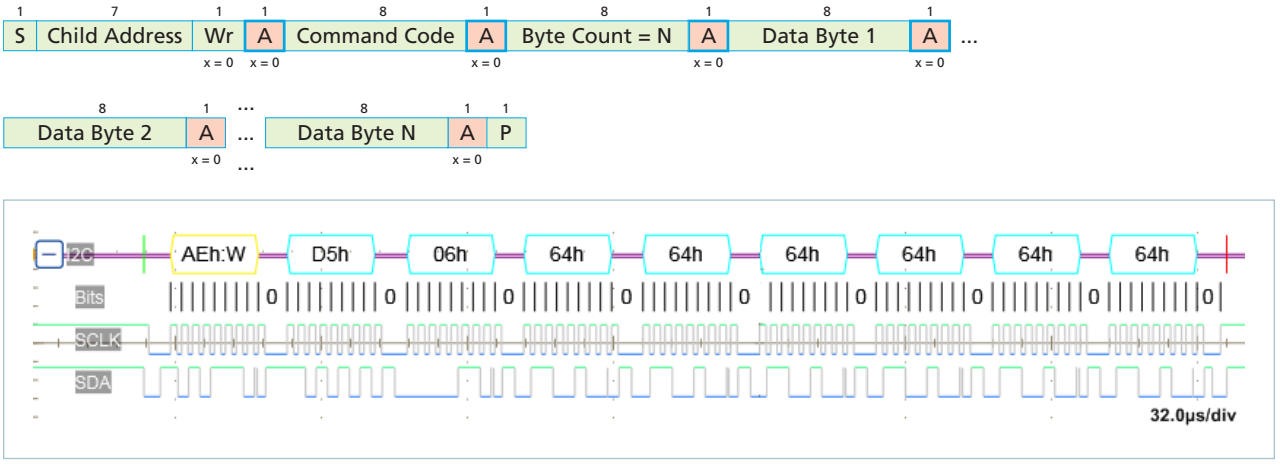
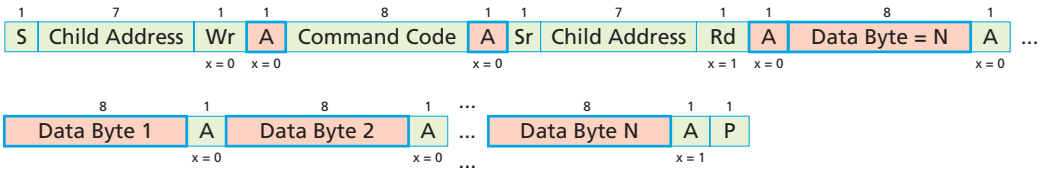


Figure 5 *— SET_ALL_THRESHOLDS COMMAND (D5h)_WRITE BLOCK PROTOCOL*

Read Block protocol:



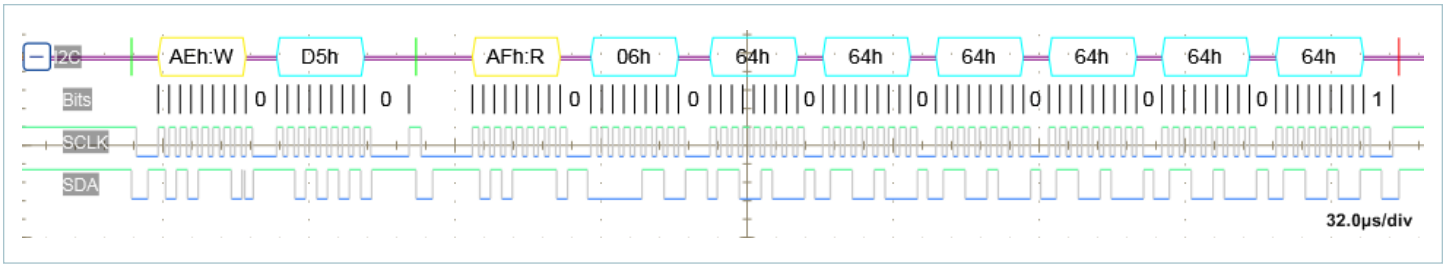
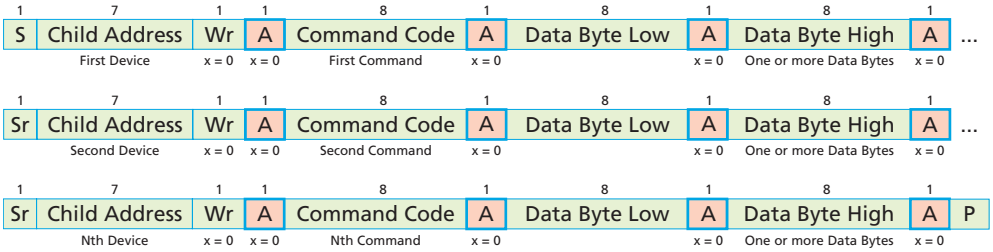


Figure 6 *— SET_ALL_THRESHOLDS COMMAND (D5h)_READ BLOCK PROTOCOL*

Write Group Command protocol:

Note that only one command per device is allowed in a group command.



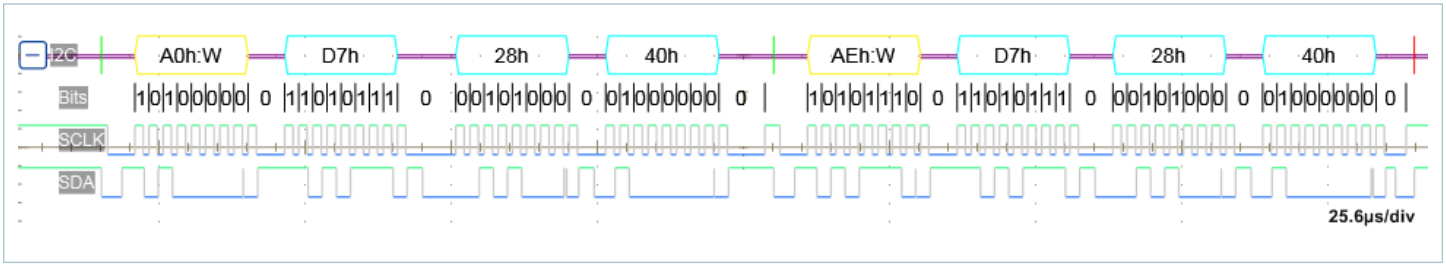


Figure 7 *— DISABLE_FAULT COMMAND (D7h)_WRITE*

Supported Commands Transaction type

A direct communication to the Digital Supervisor and a simulated communication to non-PMBus® devices is enabled by a page command. Supported command access privileges with a pre-selected PAGE are defined in the following table. Deviation from this table generates a communication error in STATUS_CML register.

Command	Code	PAGE Data Byte Access Type		
		00h	01h – 04h	FFh
PAGE	00h	R/W	R/W	R/W
OPERATION	01h	R[1]	R/W	W
ON_OFF_CONFIG	02h		R	
CLEAR_FAULTS	03h	W	W	W
CAPABILITY	19h	R		
OT_FAULT_LIMIT	4Fh		R/W	W
OT_WARN_LIMIT	51h		R/W	W
VIN_OV_FAULT_LIMIT	55h		R/W	W
VIN_OV_WARN_LIMIT	57h		R/W	W
IIN_OC_FAULT_LIMIT	5Bh		R/W	W
IIN_OC_WARN_LIMIT	5Dh		R/W	W
TON_DELAY	60h		R/W	W
STATUS_BYTE	78h	R/W[1]	R	
STATUS_WORD	79h	R[1]	R	
STATUS_IOUT	7Bh	R[1]	R/W	W
STATUS_INPUT	7Ch	R[1]	R/W	W
STATUS_TEMPERATURE	7Dh	R[1]	R/W	W
STATUS_CML	7Eh	R/W		
STATUS_MFR_SPECIFIC	80h	R[1]	R/W	W
READ_VIN	88h		R	
READ_IIN	89h	R[2]	R	
READ_VOUT	8Bh		R	
READ_IOUT	8Ch	R[2]	R	
READ_TEMPERATURE_1	8Dh	R[3]	R	
READ_POUT	96h	R[2]	R	
PMBUS_REVISION	98h	R		
MFR_ID	99h	R		
MFR_MODEL	9Ah	R	R	
MFR_REVISION	9Bh	R	R	
MFR_LOCATION	9Ch	R	R	
MFR_DATE	9Dh	R	R	
MFR_SERIAL	9Eh	R	R	
MFR_VIN_MIN	A0h	R[4]	R	
MFR_VIN_MAX	A1h	R[5]	R	
MFR_VOUT_MIN	A4h	R[4]	R	
MFR_VOUT_MAX	A5h	R[5]	R	
MFR_IOUT_MAX	A6h	R[6]	R	
MFR_POUT_MAX	A7h	R[5]	R	
BCM_EN_POLARITY	D0h		R/W	W
READ_K_FACTOR	D1h		R	
READ_BCM_ROUT	D4h		R	
SET_ALL_THRESHOLDS	D5h		R/W	W
DISABLE_FAULT	D7h		R/W	W

[1] Returns logical OR of all BCMs OPERATION states
[2] Returns sum of all BCMs recently measured value
[3] Returns highest BCM measured value
[4] Returns highest rated BCM value
[5] Returns lowest rated BCM value
[6] Returns sum of all rated connected BCMs value

Page Command (00h)

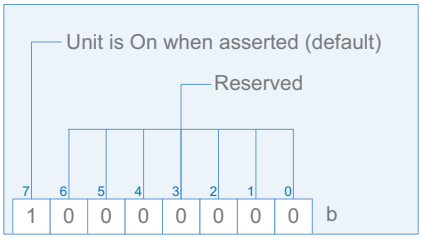
The page command data byte of 00h prior to a command call will address the Digital Supervisor specific data and a page data byte of FFh would broadcast to all of the connected BCMs. The value of the Data Byte corresponds to the pin name trailing number with the exception of 00h and FFh.

Data Byte	Description
00h	Digital Supervisor
01h	BCM at TX1 and RX1
02h	BCM at TX2 and RX2
03h	BCM at TX3 and RX3
04h	BCM at TX4 and RX4
FFh	All UART Connected BCMs

OPERATION Command (01h)

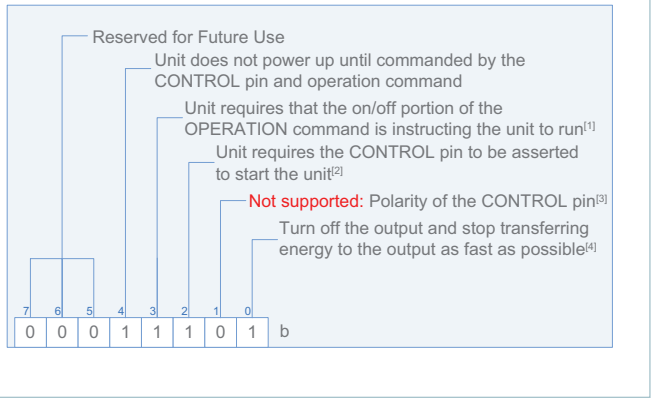
The Operation command and the BCM EN can both be used to turn on and off the connected BCM. Note that the host OPERATION command will not enable the BCM if the BCM EN pin is disabled in hardware with respect to the pre-set pin polarity. Only with the EN pin active, will the OPERATION command provide ON/OFF control.

If synchronous startup is required in the system, it is recommended to use the BCM EN pin in order to achieve simultaneous array startup.



This command accepts only two data values: 00h and 80h. If any other value is sent the command will be rejected and a CML Data error will result.

ON_OFF_CONFIG Command (02h)



[1] The BCM Enable pin is ALWAYS to be asserted for powerup. The BCM_EN_POLARITY command (D0h) bit[(1) defines the logic level required for the control pin (i.e BCM Enable pin) to be asserted.

[2] With respect to the BCM EN Control Pin if used in system

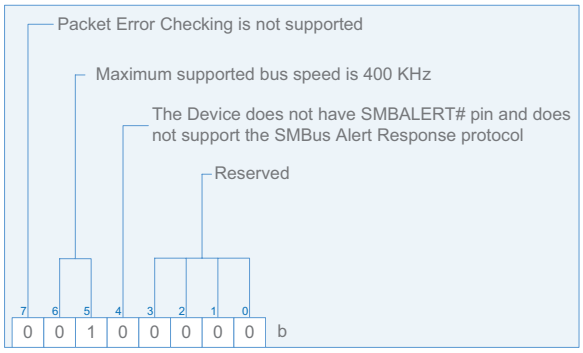
[3] See MFR_SPECIFIC_00 / BCM_EN_POLARITY to change the Polarity of the BCM Enable Pin

[4] The BCM powertrain once disabled cannot sink current

CLEAR_FAULTS Command (03h)

This command clears all status bits that have been previously set. Persistent or active faults are re-asserted again once cleared. All faults are latched once asserted in the Digital Supervisor. Registered faults will not be cleared when shutting down the BCM powertrain by recycling the BCM input voltage, or toggling the BCM EN pin, or sending the OPERATION command.

CAPABILITY Command (19h)



The Digital Supervisor returns a default value of 20h. This value indicates that the PMBus® frequency supported is up to 400KHz and that both Packet Error Checking (PEC) and SMBALERT# are not supported.

OT_FAULT_LIMIT Command (4Fh), OT_WARN_ LIMIT Command (51h), VIN_OV_FAULT_ LIMIT Command (55h), VIN_OV_WARN_ LIMIT Command (57h), IIN_OC_FAULT_ LIMIT Command (5Bh), IIN_OC_WARN_ LIMIT Command (5Dh)

The values of these registers are set in non-volatile memory and can only be written when the BCMs are disabled.

The values of the above mentioned fault and warning are set by default to a 100% of the respective BCM model supervisory limits. However these limits can be set to a lower value. For example: In order for a limit percentage to be set to 80% one would send a write command with a (50h) Data Word.

Any values outside the range of (00h – 64h) sent by a host will be rejected, will not override the currently stored value and will set the Unsupported Data bit in STATUS_CML.

The SET_ALL_THRESHOLDS COMMAND (D5h) combines in one block over temperature fault and warning limits, VIN overvoltage fault and warning limits as well as IOUT overcurrent fault and warning limits. A delay prior to a read command of up to 200ms following a write of new value is required.

The VIN_UV_WARN_LIMIT (58h) and VIN_UV_FAULT_LIMIT (59h) are set by the factory and cannot be changed by the host. However, a host can disable the under voltage setting using the DISABLE_FAULT COMMAND (D7h).

All FAULT_RESPONSE commands are unsupported. The BCM powertrain supervisory limits and powertrain protection will behave as described in the BCM datasheet. In general, once a fault is detected, the BCM powertrain will shut down and attempt to auto-restart after a predetermined delay.

TON_DELAY Command (60h)

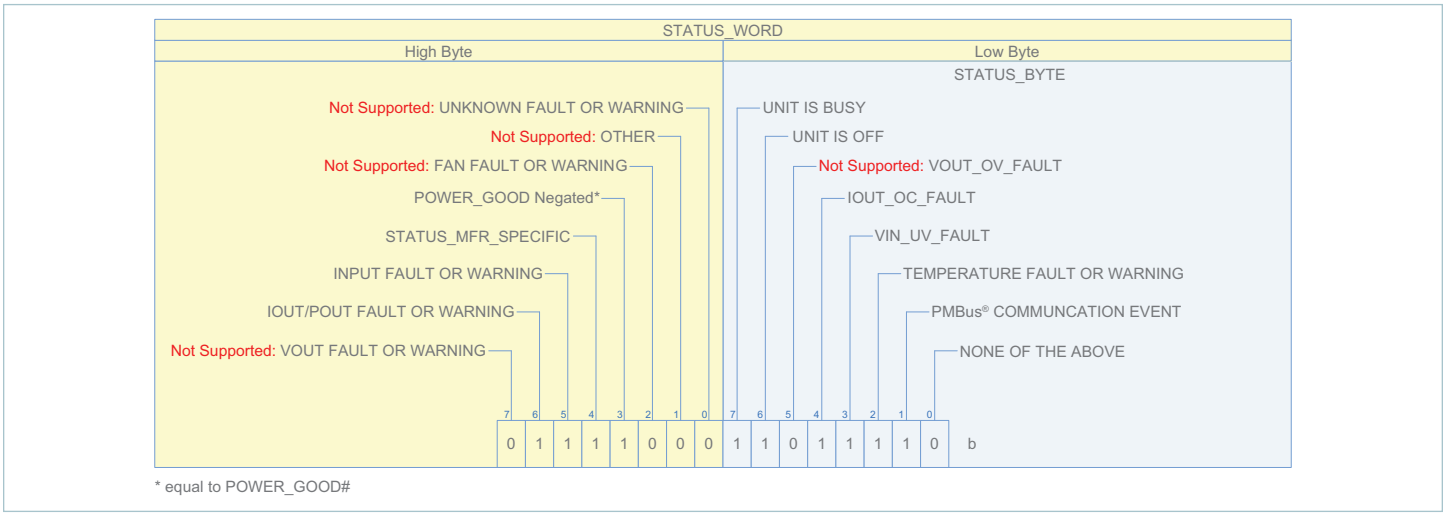
The value of this register word is set in non-volatile memory and can only be written when the BCMs are disabled.

The maximum possible delay is 100ms. Default value is set to (00h). Follow this equation below to interpret the reported value.

$$TON\_DELAY_{ACTUAL} = t_{REPORTED} \bullet 10^{-3}(s)$$

Staggering startup in an array is possible with TON_DELAY Command. This delay will be in addition to any startup delay inherent in the BCM module. For example: startup delay from application of V_{IN} is typically 20ms whereas startup with EN pin is typically 250µs. When TON_DELAY is greater than zero, the set delay will be added to both.

STATUS_BYTE (78h) and STATUS_WORD (79h)



All fault or warning flags, if set, will remain asserted until cleared by the host or once the Digital Supervisor power is removed. This includes under voltage fault, overvoltage fault, overvoltage warning, overcurrent warning, over temperature fault, over temperature warning, under temperature fault, reverse operation, communication faults and analog controller shutdown fault.

Asserted status bits in all status registers, with the exception of STATUS_WORD and STATUS_BYTE, can be individually cleared. This is done by sending a data byte with one in the bit position corresponding to the intended warning or fault to be cleared. Refer to the PMBus® Power System Management Protocol Specification – Part II – Revision 1.2 for details.

The POWER_GOOD# bit reflects the state of the device and does not reflect the state of the POWER_GOOD# signal limits. The POWER_GOOD_ON COMMAND (5Eh) and POWER_GOOD_OFF COMMAND (5Fh) are not supported. The POWER_GOOD# bit is set anytime the BCM is not in the enabled state, to indicate that the powertrain is inactive and not switching. The POWER_GOOD# bit is cleared when the BCM completes the enabling state, 5ms after the powertrain is activated allowing for soft-start to elapse. POWER_GOOD# and OFF bits cannot be cleared as they always reflect the current state of the device.

When Page (00h) is used the POWER_GOOD# bit reflects the OR-ing of all active BCMs' POWER_GOOD# bits. When Page (01h – 04h) is used POWER_GOOD# is clear only when the BCM is active.

When Page (00h) is used UNIT IS OFF is SET when all BCMs are not active. When Page (01h – 04h) is used UNIT IS OFF is clear only when the BCM is active.

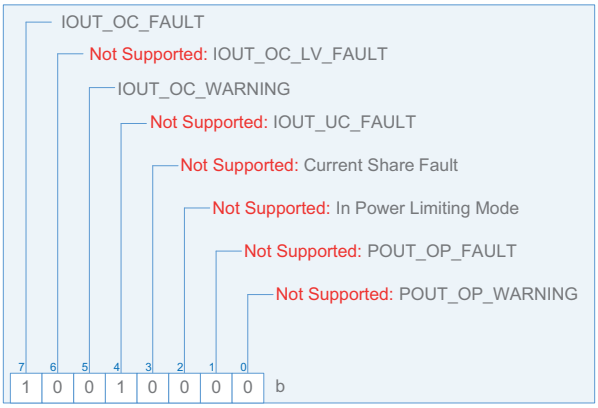
The Busy bit can be cleared using CLEAR_ALL Command (03h) or by writing either data value (40h, 80h) to PAGE (00h) using the STATUS_BYTE (78h).

Fault reporting, such as SMBALERT# signal output, and host notification by temporarily acquiring bus parent status is not supported.

If the Digital Supervisor is still powered, it will retain the last status it received from the BCM and this information will be available to the user via a PMBus Status request. This is in agreement with the PMBus standard which requires that status bits remain set until specifically cleared. Note that in this case where the BCM V_{IN} is lost, the status will always indicate an under voltage fault, in addition to any other fault that occurred.

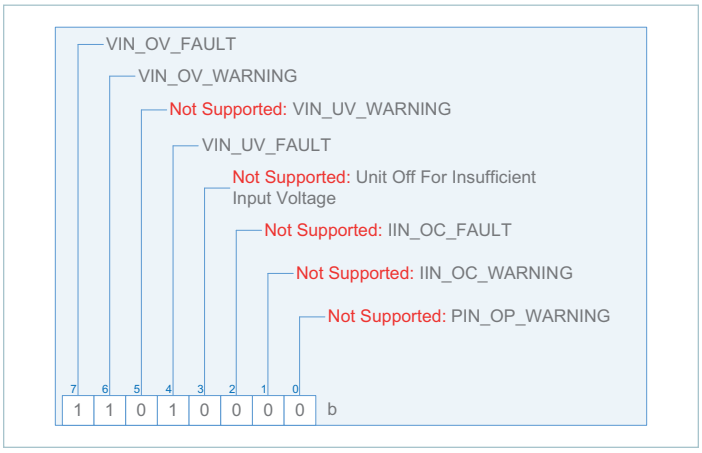
NONE OF THE ABOVE bit will be asserted if either the STATUS_MFR_SPECIFIC (80h) or the High Byte of the STATUS WORD is set.

STATUS_IOUT (7Bh)



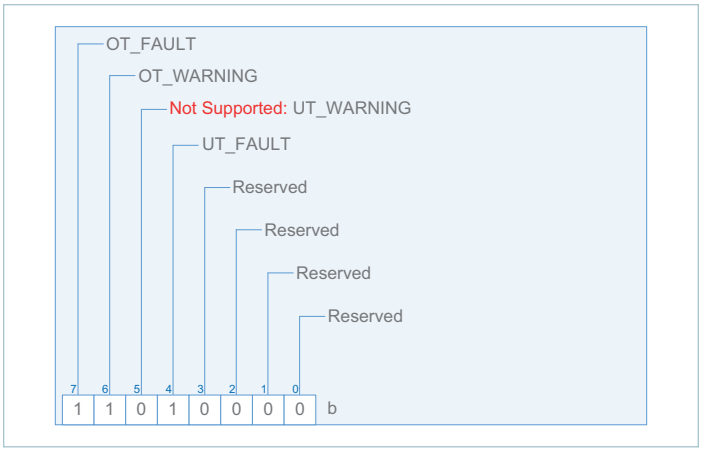
Unsupported bits are indicated above. A one indicates a fault.

STATUS_INPUT (7Ch)



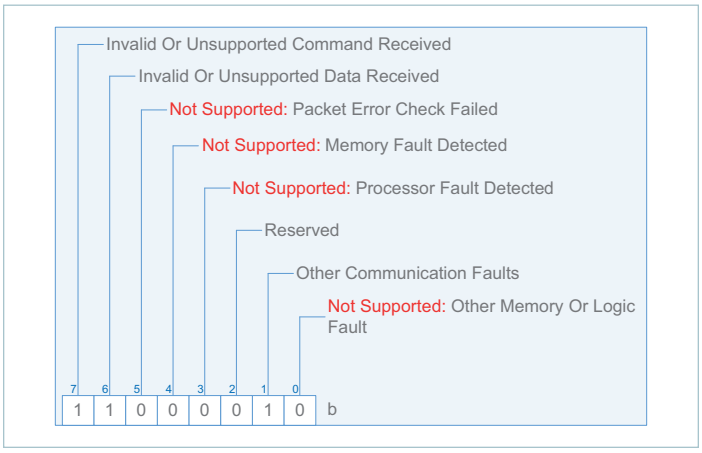
Unsupported bits are indicated above. A one indicates a fault.

STATUS_TEMPERATURE (7Dh)



Unsupported bits are indicated above. A one indicates a fault.

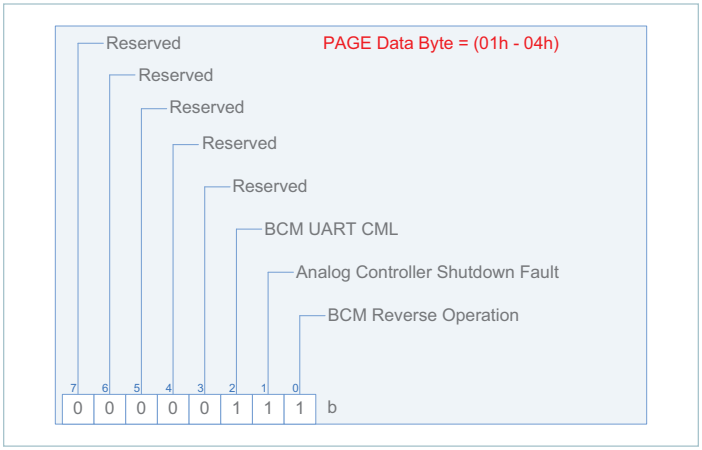
STATUS_CML (7Eh)



Unsupported bits are indicated above. A one indicates a fault.

The STATUS_CML data byte will be asserted when an unsupported PMBus® command or data or other communication fault occured.

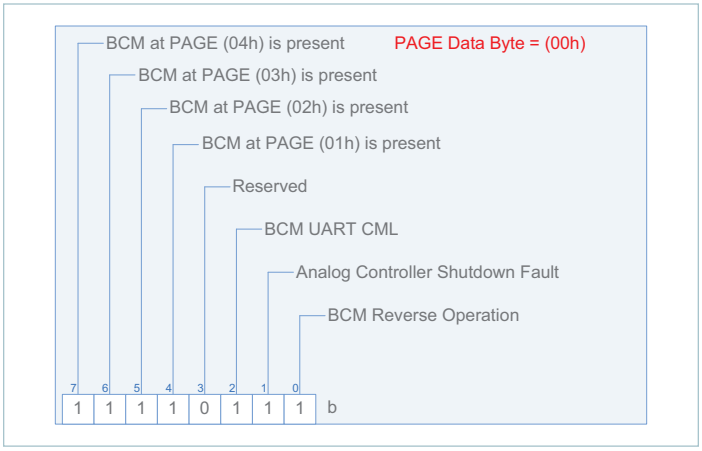
STATUS_MFR_SPECIFIC (80h)



The reverse operation bit, if asserted, indicates that the BCM is processing current in reverse. Reverse current reported value is not supported.

The BCM has analog protections and Digital Supervisory protections. The analog controller provides an additional layer of protection and has the fastest response time. The analog controller shutdown fault, when asserted, indicates that at least one of the powertrain protection faults is triggered. This fault will also be asserted if a disabled fault event occurs after asserting any bit using the DISABLE_FAULTS COMMAND.

The BCM UART is designed to operate with the Digital Supervisor UART. If the BCM UART CML is asserted, it may indicate a hardware or connection issue between both devices.



When PAGE COMMAND (00h) data byte is equal to (00h), the BCM Reverse operation, Analog Controller Shutdown Fault, and BCM UART CML bit will return OR-ing result of active BCMs. The BCM UART CML will also be asserted if any of the active BCMs stops responding. The BCM must communicate at least once to the Digital Supervisor in order to trigger this FAULT. The BCM UART CML can be cleared from the culprit BCM once the Digital Supervisor is able to communicate with it once again or can be cleared using PAGE (00h) CLEAR_FAULTS (03h) Command.

READ_VIN Command (88h)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual BCM's input voltage in the following format:

$$V_{VIN\_ACTUAL} = V_{VIN\_REPORTED} \bullet 10^{-1}(V)$$

READ_IIN Command (89h)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual BCM's input current in the following format:

$$I_{IN\_ACTUAL} = I_{IN\_REPORTED} \bullet 10^{-R}(A)$$

The value of R is specified in Reported DATA Formats section.

If PAGE data byte is equal (00h) command will return the sum of active BCMs' input current.

READ_VOUT Command (8Bh)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual BCM's output voltage in the following format:

$$V_{VOUT\_ACTUAL} = V_{VOUT\_REPORTED} \bullet 10^{-1}(V)$$

READ_IOUT Command (8Ch)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual BCM's output current in the following format:

$$I_{IOUT\_ACTUAL} = I_{IOUT\_REPORTED} \bullet 10^{-2}(A)$$

If PAGE data byte is equal (00h) command will return the sum of active BCMs' output current.

READ_TEMPERATURE_1 Command (8Dh)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual BCM's temperature in the following format:

$$T_{ACTUAL} = \pm T_{REPORTED}\ (°C)$$

If PAGE data byte is equal (00h) command will return the maximum temperature of active BCMs.

READ_POUT Command (96h)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual BCM's output power in the following format:

$$POUT_{ACTUAL} = POUT_{REPORTED}\ (W)$$

If PAGE data byte is equal to (00h) command will return the sum of active BCMs' ouput power.

MFR_VIN_MIN Command (A0h), MFR_VIN_MAX Command (A1h), MFR_VOUT_MIN Command (A4h), MFR_VOUT_MAX Command (A5h), MFR_IOUT_MAX Command (A6h), MFR_POUT_MAX Command (A7h)

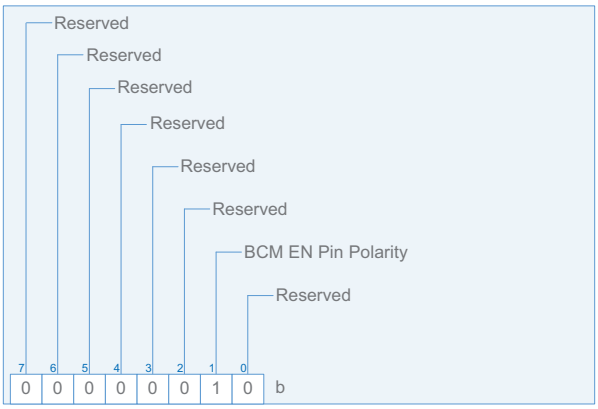
These values are set by the factory and indicate the device input output voltage and output current range and output power capacity.

The Digital Supervisor will report rated BCM input voltage minimum and maximum in Volts, output voltage minimum and maximum in Volts, output current maximum in Amperes and output power maximum in Watts.

If PAGE data byte is equal to (00h) then:

- MFR_VIN_MIN COMMAND (A0h) will return the highest MFR_VIN_MIN of all active BCMs
- MFR_VIN_MAX COMMAND (A1h) will return the lowest MFR_VIN_MAX of all active BCMs
- MFR_VOUT_MIN COMMAND (A4h) will return the highest MFR_VOUT_MIN of all active BCMs
- MFR_VOUT_MAX COMMAND (A5h) will return the lowest MFR_VOUT_MAX of all active BCMs
- MFR_IOUT_MAX COMMAND (A6h) will return the SUM of MFR_IOUT_MAX of all active BCMs
- MFR_POUT_MAX COMMAND (A7h) will return the SUM of MFR_POUT_MAX of all active BCMs

BCM_EN_POLARITY Command (D0h)



The value of this register is set in non-volatile memory and can only be written when the BCMs are disabled.

When PAGE COMMAND (00h) data byte is equal to (01h – 04h), this command defines the polarity of the EN pin. If BCM_EN_POLARITY is set, the BCM will startup once V_{IN} is greater than the under voltage threshold.

The BCM EN PIN is internally pulled-up to 3.3V. If the BCM_EN_POLARITY is cleared, an external pull-down is then required. Applying V_{IN} greater than the under voltage threshold will not suffice to start the BCM.

READ_K_FACTOR Command (D1h)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual BCM's K factor in the following format:

$$K\_FACTOR_{ACTUAL} = K\_FACTOR_{REPORTED} \bullet 2^{-16} (V/V)$$

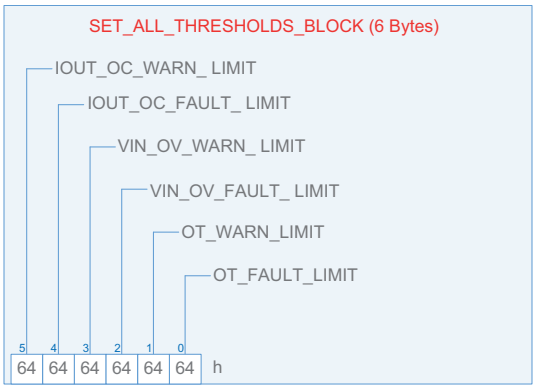
The K factor is defined in a BCM to represent the ratio of the transformer winding and hence is equal to V_{OUT} / V_{IN}.

READ_BCM_ROUT Command (D4h)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual BCM's output resistance in the following format:

$$BCM\_ROUT_{ACTUAL} = BCM\_ROUT_{REPORTED} \bullet 10^{-5} (\Omega)$$

SET_ALL_THRESHOLDS Command (D5h)



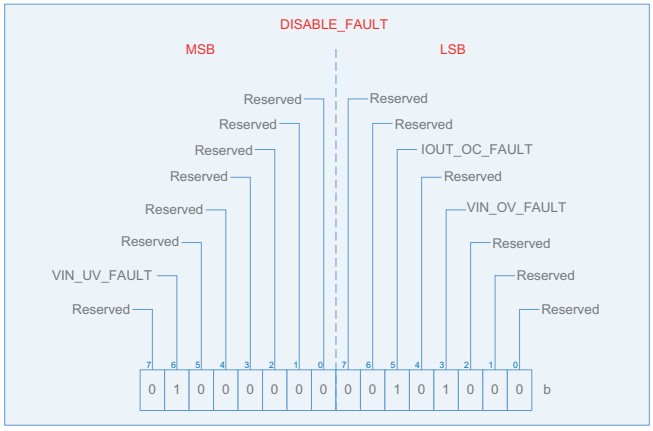
Values of this register block is set in non-volatile memory and can only be written when the BCMs are disabled.

This command provides a convenient way to configure all the limits, or any combination of limits described previously using one command.

V_{IN} Overvoltage, Overcurrent and Overtemperature values are all set to 100% of the BCM datasheet supervisory limits by default and can only be set to a lower percentage.

To leave a particular threshold unchanged, set the corresponding threshold data byte to a value greater than (64h).

DISABLE_FAULT Command (D7h)



Unsupported bits are indicated above. A one indicates that the supervisory fault associated with the asserted bit is disabled.

The value of these registers is set in non-volatile memory and can only be written when the BCMs are disabled.

This command allows the host to disable the supervisory faults and respective statuses. It does not disable the powertrain analog protections or warnings with respect to the set limits in the SET_ALL_THRESHOLDS Command.

The input under-voltage can only be disabled to a pre-set low limit as shown in the functional reporting range in the BCM data sheet.

The Digital Supervisor Implementation vs. PMBus® Specification Rev 1.2

The Digital Supervisor is an I2C compliant, SMBus™ compatible device and PMBus command compliant device. This section denotes some deviation, perceived as differences from the PMBus Part I and Part II specification Rev 1.2.

1. The Digital Supervisor meets all Part I and II PMBus specification requirements with the following differences to the transport requirement.

Unmet DC parameter Implementation vs SMBus™ spec						
Symbol	Parameter	D44TL1A0		SMBus™ Rev 2.0		Units
		Min	Max	Min	Max	
V_{IL}[a]	Input Low Voltage	-	0.99	-	0.8	V
V_{IH}[a]	Input High Voltage	2.31	-	2.1	V_{VDD_IN}	V
I_{LEAK_PIN}[b]	Input Leakage per Pin	10	22	-	±5	µA

[a] V_{VDD_IN} = 3.3V
[b] V_{BUS} = 5V

2. The Digital Supervisor accepts 38 PMBus command codes. Implemented commands execute functions as described in the PMBus specification.

- Deviations from the PMBus specification:
  - **a.** Section 15, fault related commands
    - The limits and Warnings unit implemented is percentage (%) a range from decimal (0-100) of the factory set limits.

3. The Digital Supervisor unsupported PMBus command code response as described in the Fault Management and Reporting:

- Deviations from the PMBus specification:
  - **a.** PMBus section 10.2.5.3, exceptions
    - The busy bit of the STATUS_BYTE as implemented can be cleared (80h). In order to maintain compatibility with the specification (40h) can also be used.
- Manufacturer Implementation of the PMBus Spec
  - **a.** PMBus section 10.5, setting the response to a detected fault condition
    - All powertrain responses are pre-set and cannot be changed. Refer to the BCM datasheet for details.
  - **b.** PMBus section 10.6, reporting faults and warnings to the Host
    - SMBALERT# signal and Direct PMBus Device to Host Communication are not supported. However, the Digital Supervisor will set the corresponding fault status bits and will wait for the host to poll.
  - **c.** PMBus section 10.7, clearing a shutdown due to a fault
    - There is no RESET pin or EN pin in the Digital Supervisor. Cycling power to the Digital Supervisor will not clear a BCM Shutdown. The BCM will clear itself once the fault condition is removed. Refer to the BCM datasheet for details.
  - **d.** PMBus Section 10.8.1, corrupted data transmission faults:
    - Packet error checking is not supported.

Data Transmission Faults Implementation

This section describes data transmission faults as implemented in the Digital Supervisor.

Section	Description	Response to Host		STATUS_BYTE	STATUS_CML		Notes
		NAK	FFh	CML	Other Fault	Unsupported Data	
10.8.1	Corrupted data						No response; PEC not supported
10.8.2	Sending too few bits			X	X		
10.8.3	Reading too few bits			X	X		
10.8.4	Host sends or reads too few bytes			X	X		
10.8.5	Host sends too many bytes	X		X		X	
10.8.6	Reading too many bytes		X	X	X		
10.8.7	Device busy	X	X				Device will ACK own address BUSY bit in STATUS_BYTE even if STATUS_WORD is set

Data Content Faults Implementation

This section describes data content fault as implemented in the Digital Supervisor.

Section	Description	Response to Host	STATUS_BYTE	STATUS_CML			Notes
		NAK	CML	Other Fault	Unsupported Command	Unsupported Data	
10.9.1	Improperly Set Read Bit In The Address Byte	X	X	X			
10.9.2	Unsupported Command Code	X	X		X		
10.9.3	Invalid or Unsupported Data		X			X	
10.9.4	Data Out of Range		X			X	
10.9.5	Reserved Bits						No response; not a fault

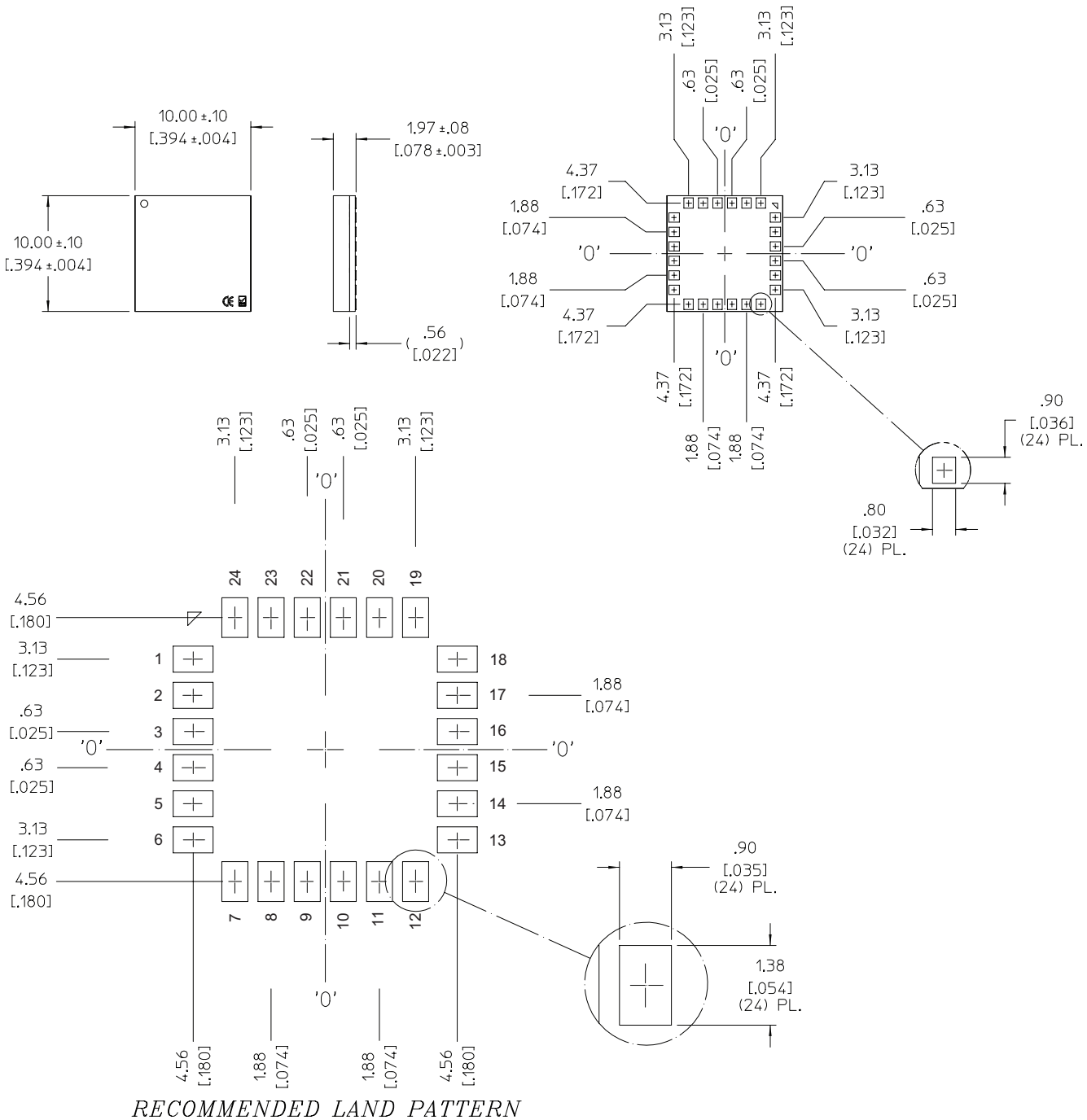
Layout Considerations

Application Note AN:016 details board layout recommendations using VI Chip® modules to attain the design goals of good power connections, reducing EMI, and shielding of control signals.

The Digital Supervisor signal should be properly shielded from external noise sources, including the BCM itself. The preferred method is to route (RX, TX) signals in internal layers and to envelop both signals with continuous reference planes referenced to –OUT of the respective BCM. These digital signals can have fast edges. Standard digital design practices should be used.

Avoid routing BCM signals ENABLE, SER-IN and SER-OUT directly underneath the BCM.

Mechanical Drawing and Recommended Land Pattern



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