

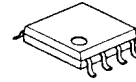
## DOUBLE BALANCED MODULATION / DEMODULATION

■ **GENERAL DESCRIPTION**

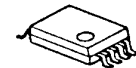
The **NJM2594** is a double balanced modulation/demodulation circuit, applied to suppressed carrier modulation, amplitude modulation, synchronous detection, FM or PM detection circuit.

Single input voltage and simplification of external circuit offers wider applications.

■ **PACKAGE OUTLINE**



**NJM2594M**

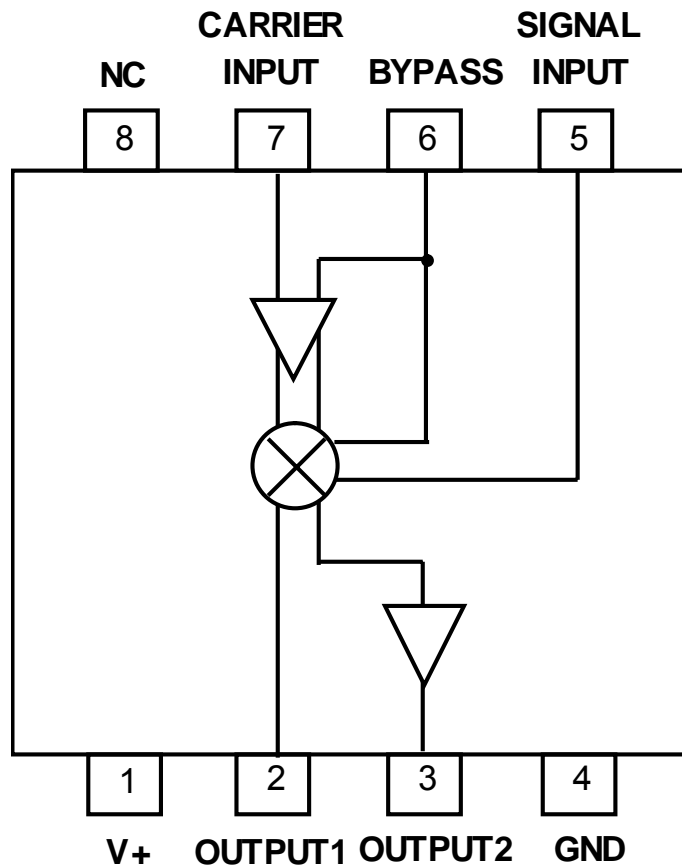


**NJM2594V**

■ **FEATURES**

- Operating Voltage                                      4.5 to 9V
- Excellent Carrier Suppression
- Simplification of External Circuit
- Bipolar Technology
- Package Outline    DMP8, SSOP8

■ **BLOCK DIAGRAM**



BLOCK DIAGRAM

# NJM2594

## ■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V <sup>+</sup>	14.0	V
Power Dissipation	P <sub>D</sub>	250(SSOP-8), 300(DMP-8)	mW
Operating Temperature	T <sub>opr</sub>	- 40 to +85	°C
Storage Temperature	T <sub>stg</sub>	- 40 to +125	°C
Output 2 Drive Current	I <sub>d</sub>	10	mA

## ■ RECOMMENDED OPERATIONAL CONDITION

(Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V <sup>+</sup>		4.5	5.0	9.0	V

## ■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V<sup>+</sup>=5.0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Current Consumption	I <sub>cc</sub>	No Signal	-	11	14	mA
Conversion Gain	G <sub>c</sub>	note(1)	- 2.0	0	+ 2.0	dB
Signal Leakage Level	L <sub>s</sub>	note(1)	-	-35	-20	dB
Carrier Leakage Level	L <sub>c</sub>	note(1)	-	-40	-20	dB
Intermodulation	IMD	note (2)	-	- 60	-	dB
Signal Input Resistance	R <sub>s</sub>		-	600	-	Ω
Signal Input Capacitance	C <sub>s</sub>	note (7)	-	3.8	-	pF
Carrier Input Resistance	R <sub>c</sub>		-	1200	-	Ω
Carrier Input Capacitance	C <sub>c</sub>	note (7)	-	2.2	-	pF
Output Resistance	R <sub>o</sub>	OUTPUT1 terminal	-	350	-	Ω
Output Capacitance	C <sub>o</sub>	OUTPUT1 terminal note (7)	-	2.6	-	pF

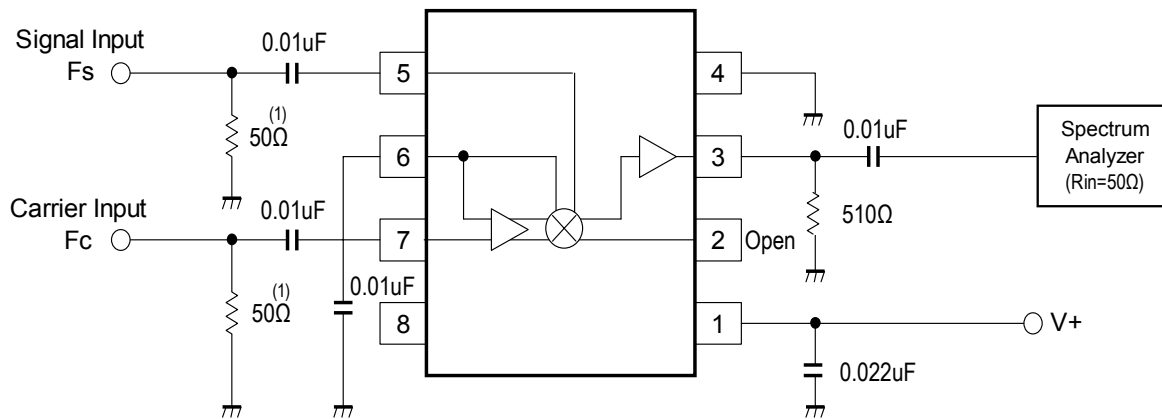
Notes :

- (1) Input signal : Fs=1.75MHz, 70mVrms(-10dBm)  
Carrier signal : Fc=28.25MHz, 100mVrms(-7dBm)  
Desired output signal : fundamental carrier upper-sideband output, Fd=30MHz
- (2) Input signal 1 : Fs1=1.75MHz, 42.5mVrms(-14.42dBm)  
Input signal 2 : Fs2=2.00MHz, 42.5mVrms(-14.42dBm)  
Carrier signal : Fc=28.25MHz, 100mVrms(-7dBm)
- (3) The ratio of desired output signal level to input signal level
- (4) The ratio of output signal at input signal frequency to desired output signal
- (5) The ratio of output signal at carrier signal frequency to desired output signal
- (6) The ratio of 29.75MHz Intermodulation signal to desired output signal
- (7) Measured at 10MHz

■ MEASUREMENT CIRCUIT

● Emitter - follower Output

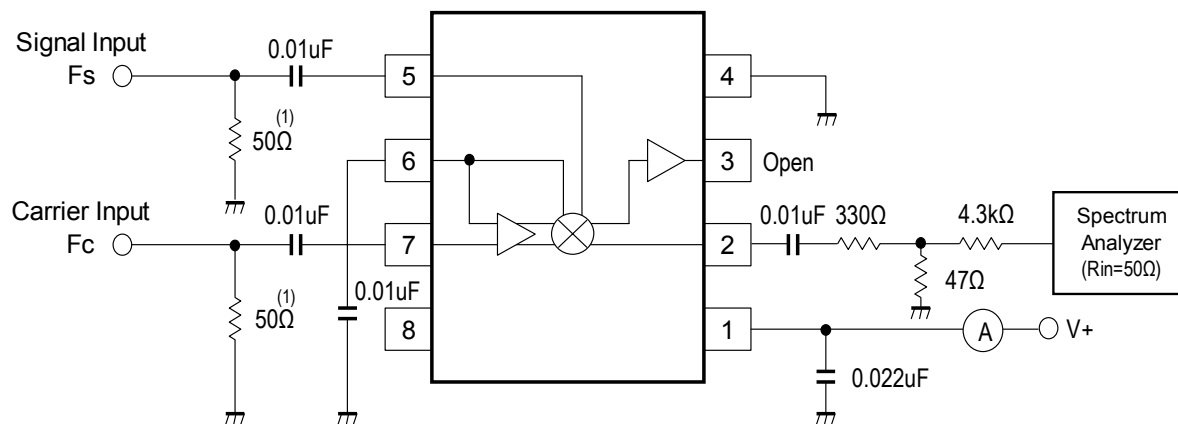
Items for measurement : Conversion Gain, Signal Leakage Level, Carrier Leakage Level, Intermodulation  
 Measured at OUTPUT2 (pin 3)



TEST CIRCUIT 1

● Collector Output

Items for measurement : Current Consumption  
 Measured at OUTPUT1 (pin2)



TEST CIRCUIT 2

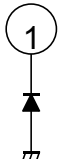
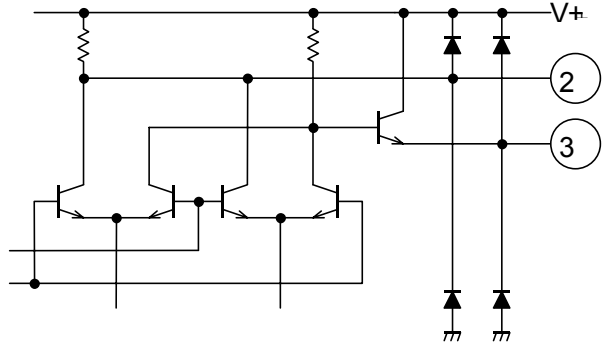
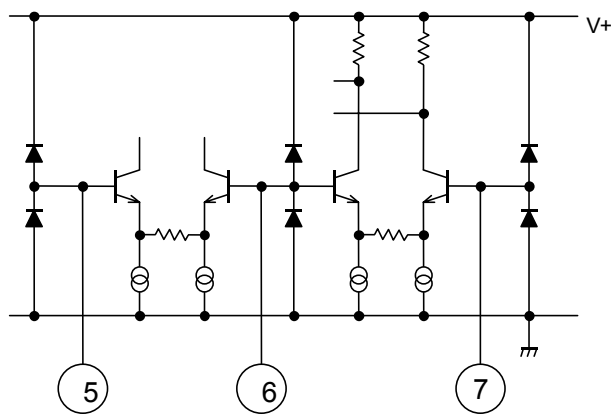
Notes :

(1) Impedance-matching resistor

# NJM2594

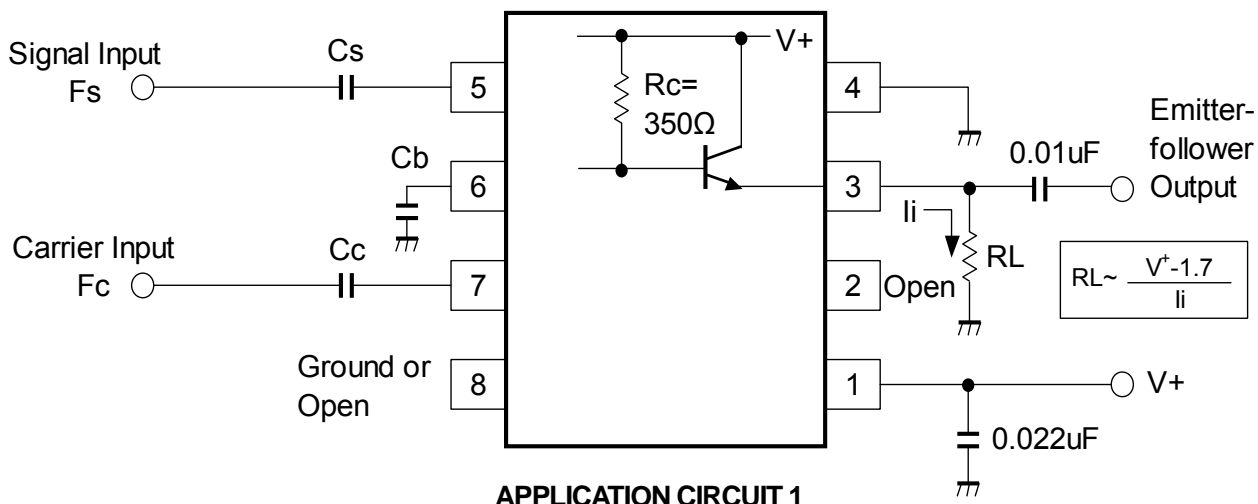
## ■ TERMINAL FUNCTION

(Ta=25°C, V+=5.0V)

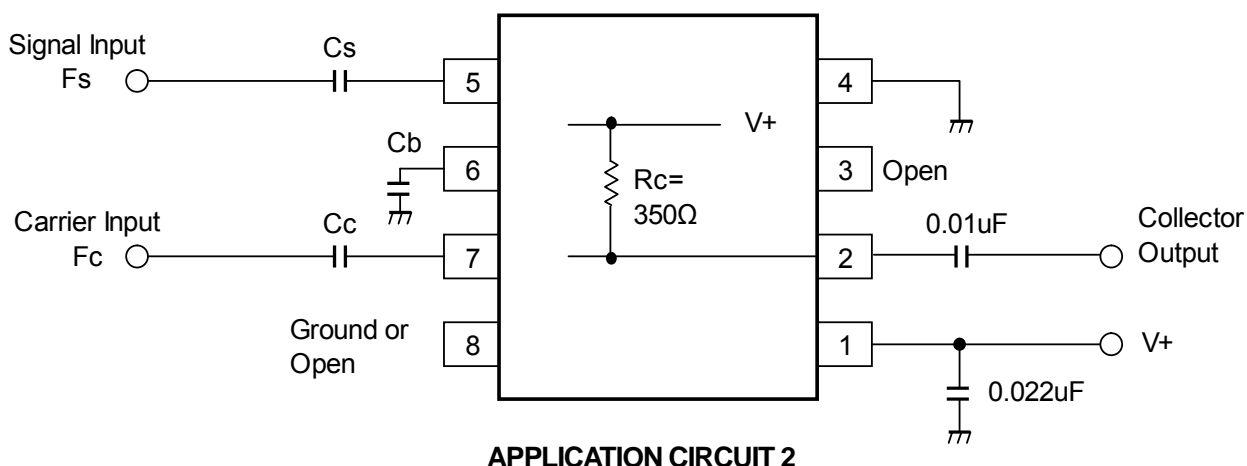
Pin No.	SYMBOL	EQUIVALENT CIRCUIT	VOLTAGE	FUNCTION
1	V+		5V	Power Supply.
2	OUTPUT1		4.0V	Collector Output.
3	OUTPUT2		3.3V	Emitter Output. Since there is no internal resistor to the ground, emitter current may be obtained by connecting an external resistor. This terminal voltage is obtained with a 510Ω external resistor.
4	GND		--	Ground.
5	SIGNAL INPUT		2.2V	Signal Input Terminal.
6	BYPASS		2.2V	Common base lead of two differential circuits. This terminal should be connected externally to AC ground.
7	CARRIER INPUT		2.2V	Carrier Input Terminal.
8	NC		--	No Connect. The NC terminal is not connected to internal circuit so that this terminal can be open or grounded.

■ APPLICATION CIRCUIT

● Emitter - follower output



● Collector output



- The impedance of AC coupling capacitor connected to input / output terminals should be adequately low at the frequency of input / output signals, respectively.
- The impedance of base-coupling capacitor connected to BYPASS terminal should be adequately low against the both of input/output signals to keep better performance on leakage and distortion characteristics.
- In case of APPLICATION CIRCUIT 1, idle (emitter) current may be supplied by adding an external resistor between OUTPUT2 (pin3) and ground.

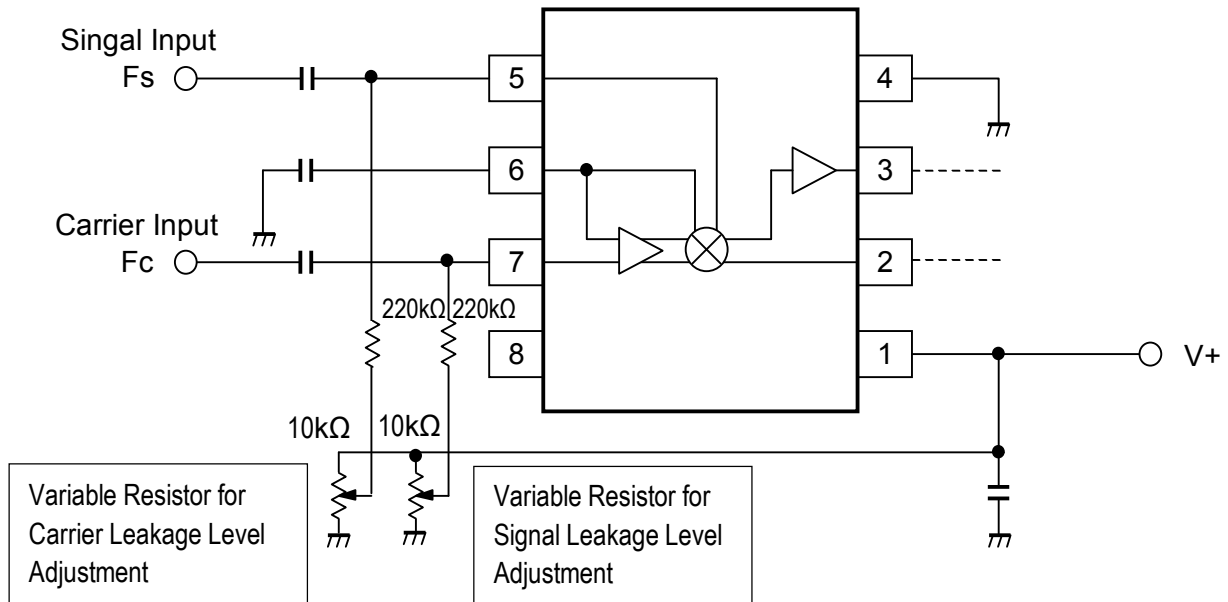
The relation of idle current  $I_i$  and external resistance  $R_L$  is determined by :

$$R_L \sim \frac{V^+ - 1.7}{I_i}$$

- Note that there is some degradation in intermodulation characteristics with increasing the external resistance  $R_L$ , or decreasing a load impedance of Emitter-follower output.
- The level of output signal comes constant at carrier input signal level over 100mV ( see Typical Characteristics).

## ■ HOW TO DECREASE LEAKAGE LEVEL

By adjusting DC bias of SIGNAL INPUT terminal, carrier leakage level may be decreased. By adjusting DC bias of CARRIER INPUT terminal, signal leakage level may be decreased. In actual circuit, it can be seen the case that either of these adjustment is provided, not both.



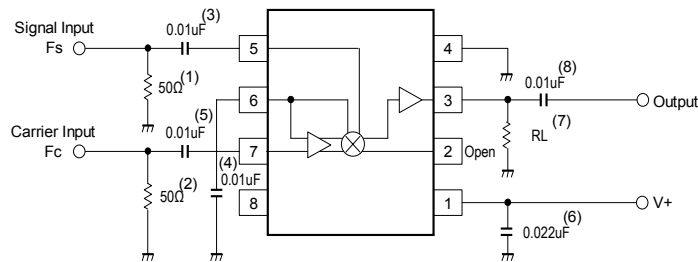
LEAKAGE ADJUSTMENT CIRCUIT

## ■ EVALUATION PC BOARD

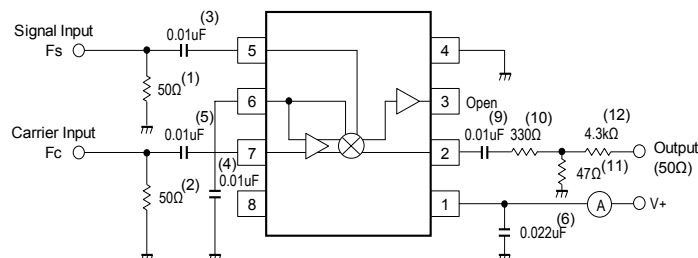
The evaluation PC board shown in next page is useful for your design and is intended to have more understanding of the usage and performance of this device. Two kinds of board are prepared for two packages, SSOP and DMP, respectively. Each board can be applied to two kinds of circuit, emitter-follower output type and collector output type, as shown below. This circuit is the same as MEASUREMENT CIRCUIT. For other electrical conditions, it should be necessary to reconsider each value of components, especially of capacitance.

Note that this board is not prepared to show the recommendation of pattern and parts layout.

### ● Emitter - follower output

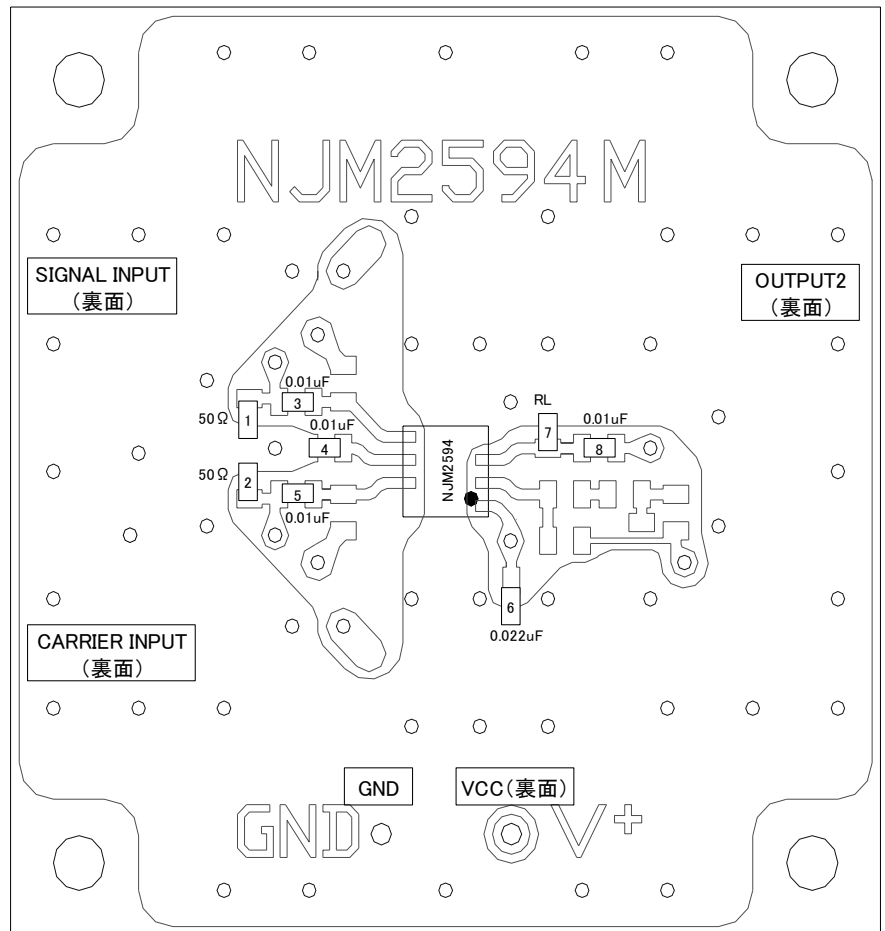


### ● Collector output

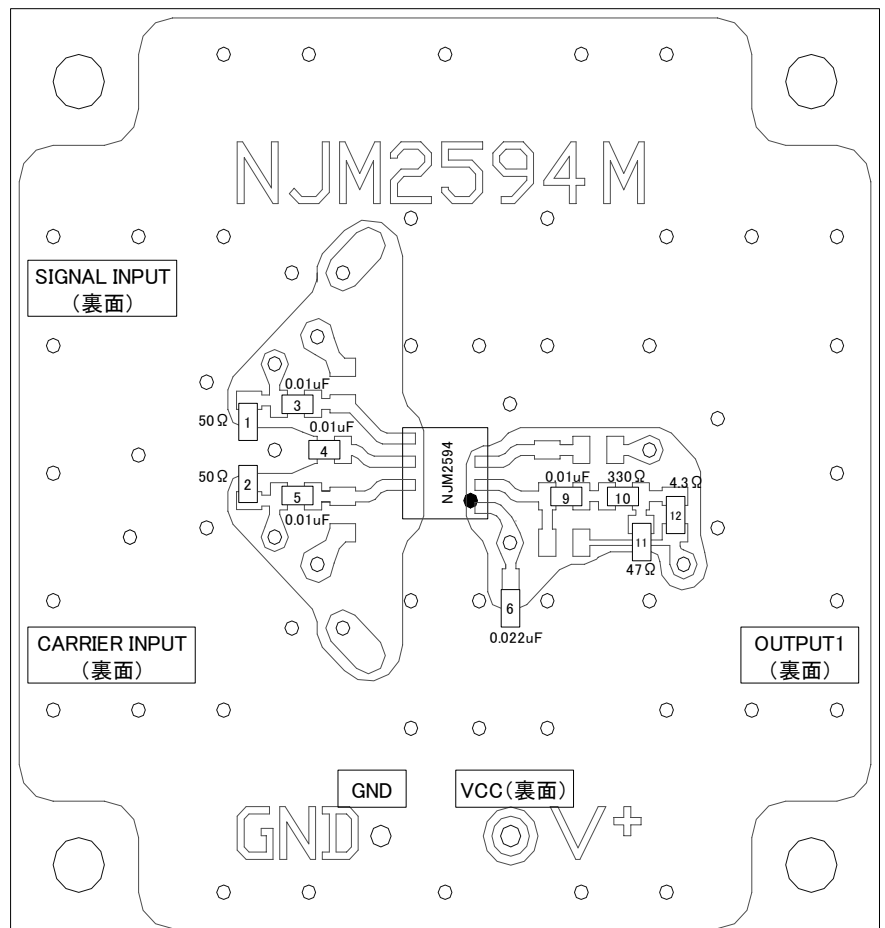


## Evaluation PC Board Component Placement View

- Emitter - follower output

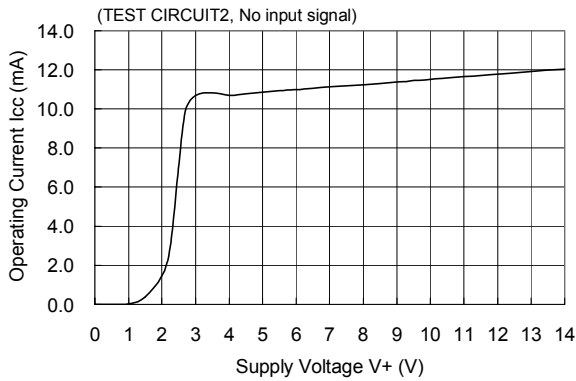


- Collector output

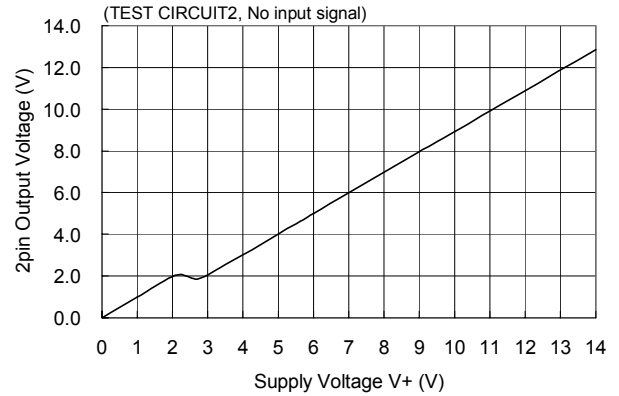


## ■ TYPICAL CHARACTERISTICS (Ta=25°C, V+=5.0V, unless otherwise noted)

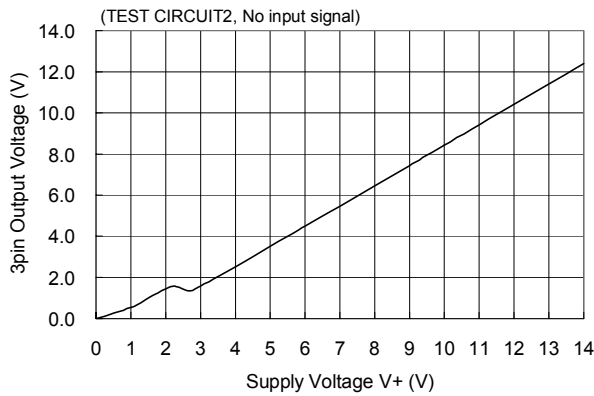
**Operating Current versus Supply Voltage**



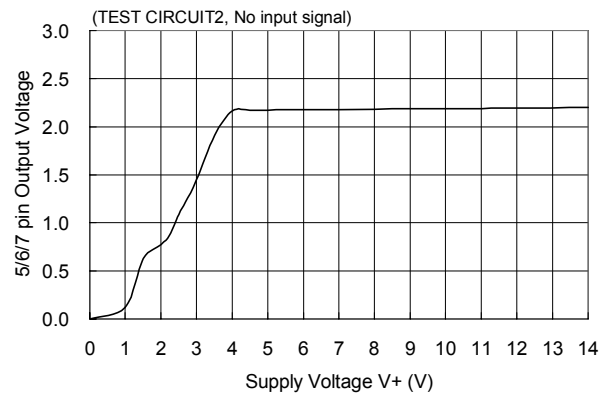
**2pin Output Voltage versus Supply Voltage**



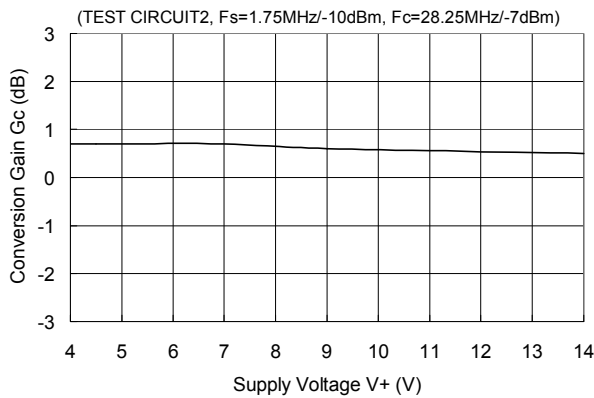
**3pin Output Voltage versus Supply Voltage**



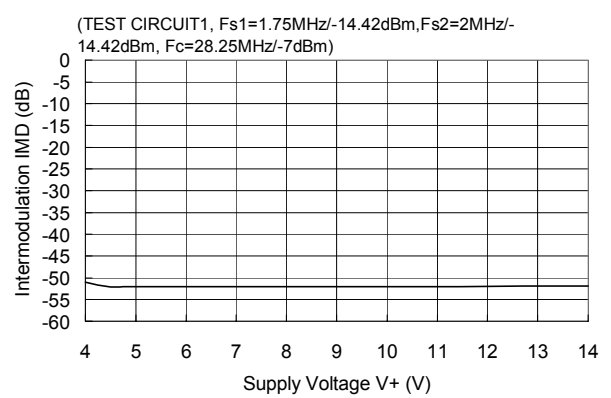
**5/6/7 pin Output Voltage versus Supply Voltage**



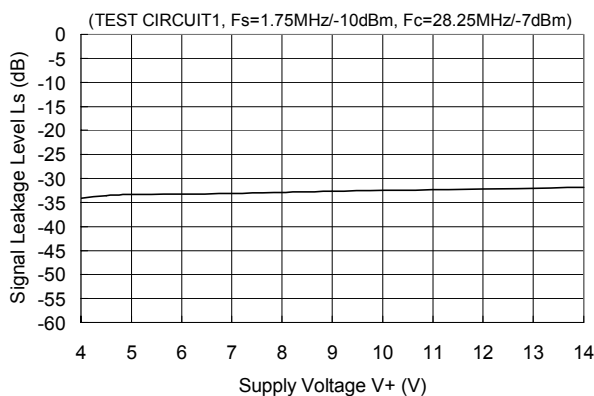
**Conversion Gain versus Supply Voltage**



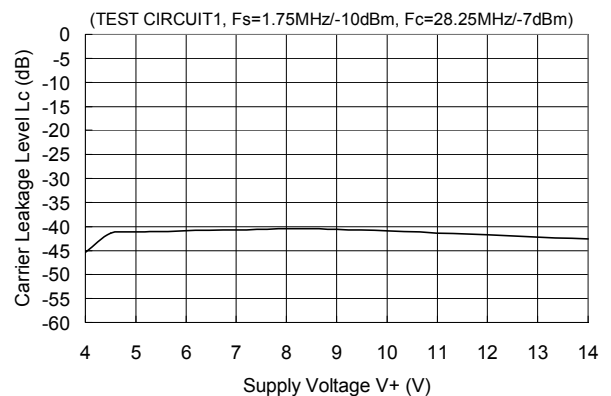
**Intermodulation versus Supply Voltage**



**Signal Leakage Level versus Supply Voltage**

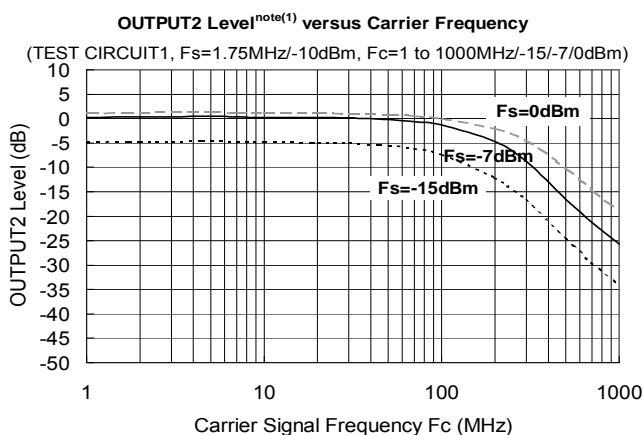
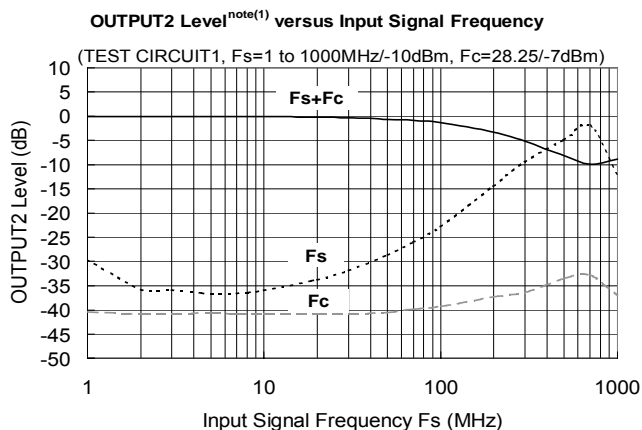
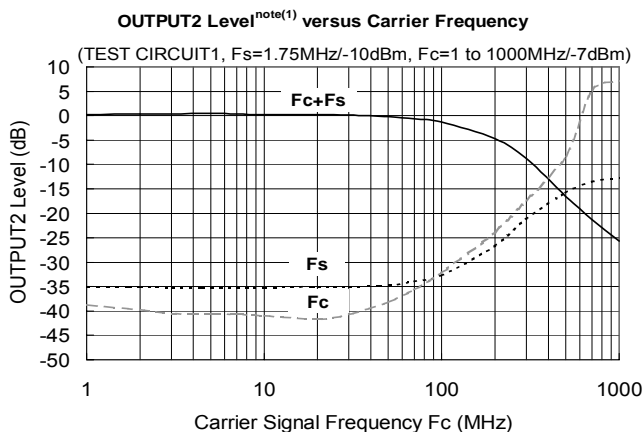


**Carrier Leakage Level versus Supply Voltage**

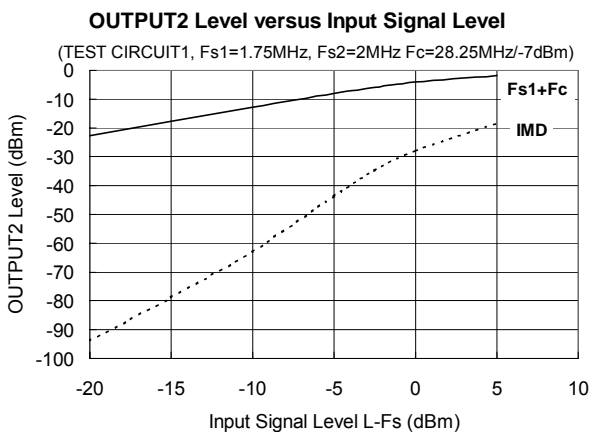
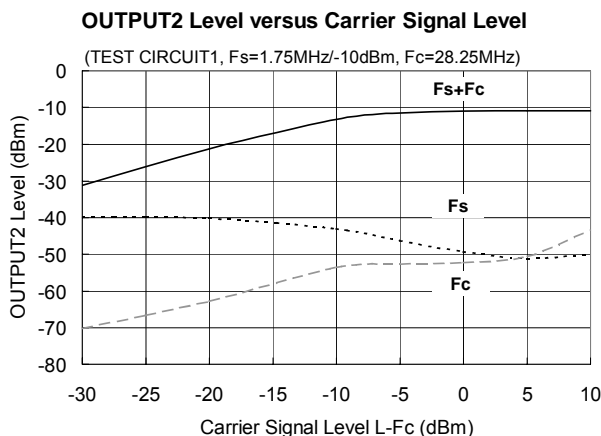
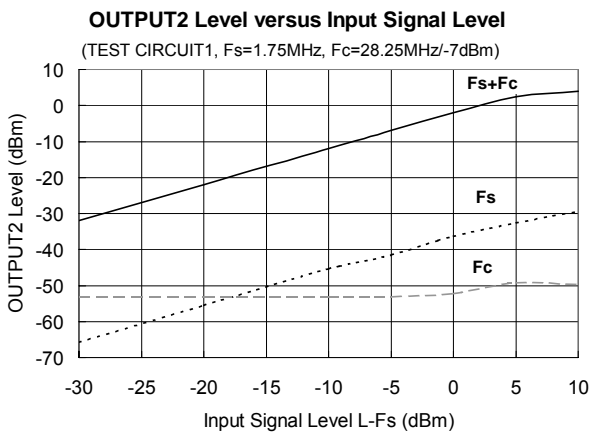




■ TYPICAL CHARACTERISTICS ( Ta=25°C, V+=5.0V, unless otherwise noted )

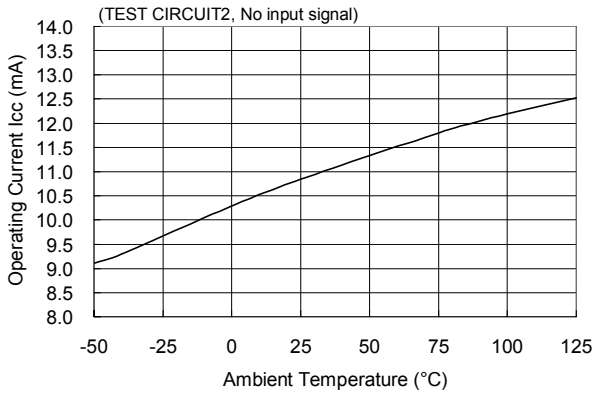


Note :  
 (1) OUTPUT2 level (dB):  
 the ratio of OUTPUT2 Level to input signal level.

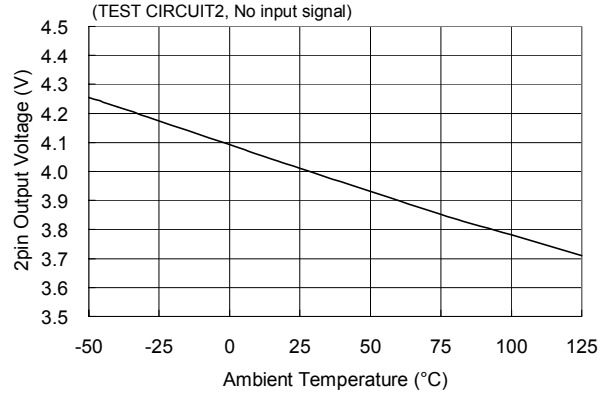


## ■ TYPICAL CHARACTERISTICS ( $T_a=25^\circ\text{C}, V^+=5.0\text{V}$ , unless otherwise noted )

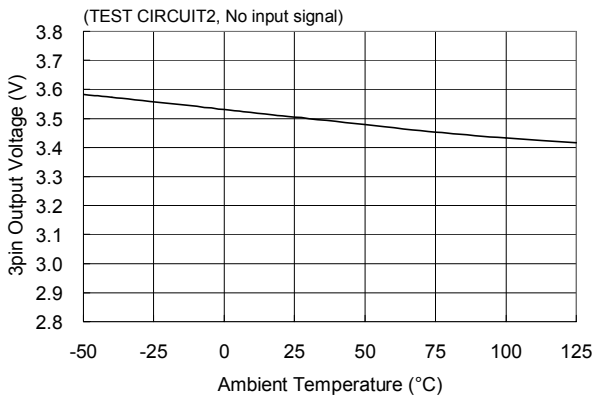
**Operating Current versus Ambient Temperature**



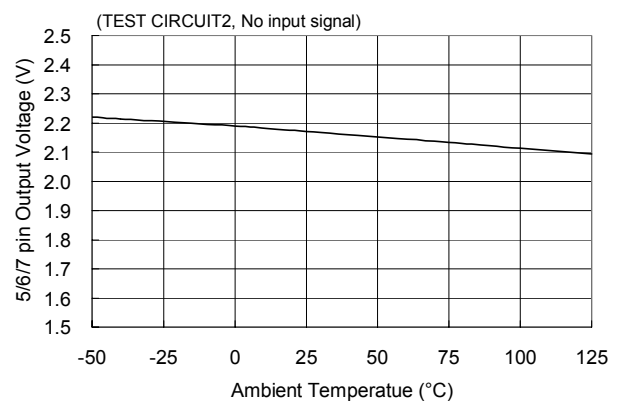
**2pin Output Voltage versus Ambient Temperature**



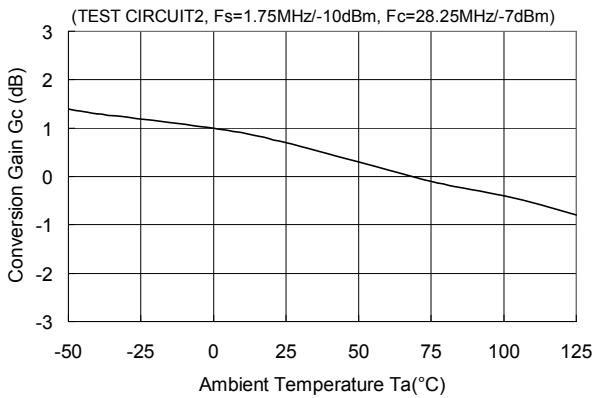
**3pin Output Voltage versus Ambient Temperature**



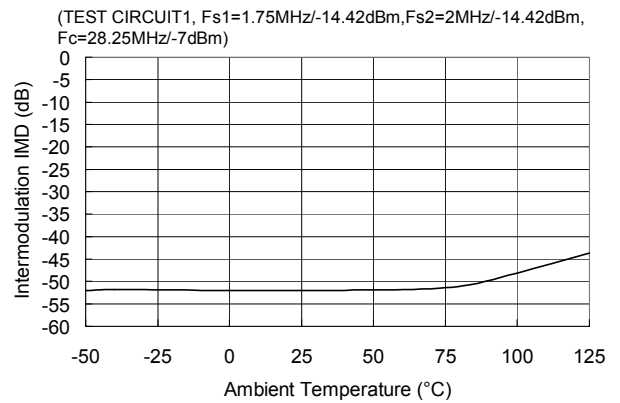
**5/6/7 pin Output Voltage versus Ambient Temperature**



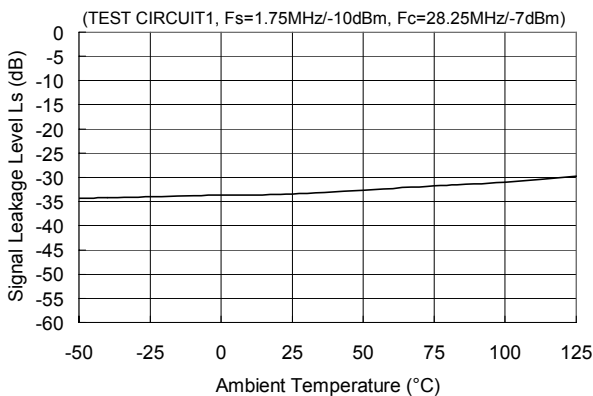
**Conversion Gain versus Ambient Temperature**



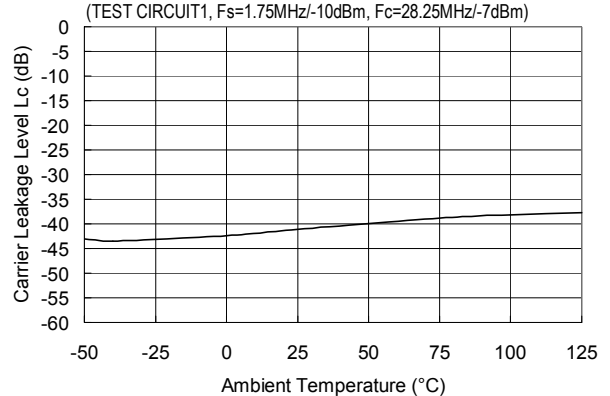
**Intermodulation versus Ambient Temperature**



**Signal Leakage Level versus Ambient Temperature**



**Carrier Leakage Level versus Ambient Temperature**



[CAUTION]

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