

# Enhanced Current Mode PWM Controller

## Description

The CS51021/22/23/24 Fixed Frequency PWM Current Mode Controller family provides all necessary features required for AC-DC or DC-DC primary side control. Several features are included eliminating the additional components needed to implement them externally. In addition to low start-up current (75µA) and high frequency operation capability, the CS51021/22/23/24 family includes overvoltage and undervoltage monitoring, externally programmable dual

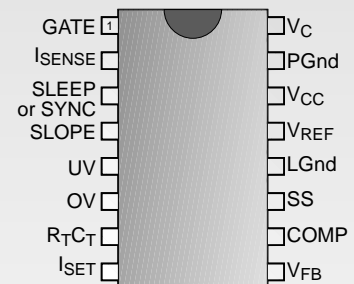
threshold overcurrent protection, current sense leading edge blanking, current slope compensation, accurate duty cycle control and an externally available 5V reference. The CS51021 and CS51023 feature bidirectional synchronization capability, while the CS51022 and CS51024 offer a sleep mode with 100µA maximum IC current consumption. The CS51021/22/23/24 family is available in a 16 lead narrow body SO package.

## Features

- 75µA Max. Startup Current
- Fixed Frequency Current Mode Control
- 1MHz Switching Frequency
- Undervoltage Protection Monitor
- Overvoltage Protection Monitor with Programmable Hysteresis
- Programmable Dual Threshold Overcurrent Protection with Delayed Restart
- Programmable Soft Start
- Accurate Maximum Duty Cycle Limit
- Programmable Slope Compensation
- Leading Edge Current Sense Blanking
- 1A Sink/Source Gate Drive
- Bidirectional Synchronization (CS51021/23)
- 50ns PWM Propagation Delay
- 100µA Max Sleep Current (CS51022/24)

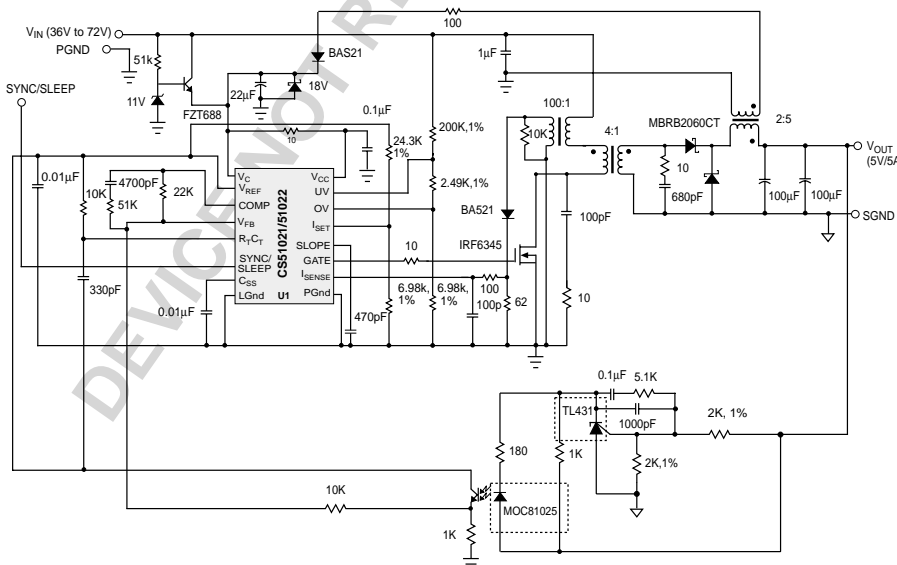
## Package Options

16 Lead SO Narrow & PDIP



Consult factory for other package options.

## Typical Application Diagram



36-72V to 5V, 5A DC-DC Converter



ON Semiconductor

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## Absolute Maximum Ratings

Power Supply Voltage, $V_{CC}$ .....	-0.3V, 20V
Driver Supply Voltage, $V_C$ .....	-0.3V, 20V
SYNC, SLEEP, $R_T C_T$ , SOFT START, $V_{FB}$ , SLOPE, $I_{SENSE}$ , UV, OV, $I_{SET}$ (Logic Pins).....	-0.25V to $V_{REF}$
Peak GATE Output Current.....	1A
Steady State Output Current.....	$\pm 0.2A$
Operating Junction Temperature, $T_J$ .....	150°C
Storage Temperature Range, $T_S$ .....	-65 to 150°C
ESD (Human Body Model).....	2kV
Lead Temperature Soldering: Reflow (SMD styles only).....	60 sec. max above 183°C, 230°C peak

**Electrical Characteristics: Unless otherwise stated, specifications apply for  $-40^\circ\text{C} < T_A < 85^\circ\text{C}$ ,  $-40^\circ\text{C} < T_J < 150^\circ\text{C}$ ,  $3\text{V} < V_C < 20\text{V}$ ,  $8.2\text{V} < V_{CC} < 20\text{V}$ ,  $R_T = 12\text{k}\Omega$ ,  $C_T = 390\text{pF}$ .**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>■ Under Voltage Lockout</b>					
START Threshold (CS51021/22)		7.95	8.25	8.8	V
START Threshold (CS51023/24)		12.4	13	13.4	V
STOP Threshold		7.4	7.7	8.2	V
Hysteresis (CS51021/22)		0.50	0.75	1.00	V
Hysteresis (CS51023/24)		4	5	6	V
$I_{CC}$ @ Startup (CS51021/22)	$V_{CC} < UV_{START}$ Threshold		40	75	$\mu\text{A}$
$I_{CC}$ @ Startup (CS51023/24)	$V_{CC} < UV_{START}$ Threshold		45	75	$\mu\text{A}$
$I_{CC}$ Operating (CS51021/23)			7	9	mA
$I_{CC}$ Operating (CS51022/24)			6	8	mA
$I_C$ Operating	Includes 1nF Load		7	12	mA
<b>■ Voltage Reference</b>					
Initial Accuracy	$T_A = 25^\circ\text{C}$ , $I_{REF} = 2\text{mA}$ , $V_{CC} = 14\text{V}$ (Note1)	4.95	5	5.05	V
Total Accuracy	$1\text{mA} < I_{REF} < 10\text{mA}$	4.9	5	5.15	V
Line Regulation	$8.2\text{V} < V_{CC} < 18\text{V}$ , $I_{REF} = 2\text{mA}$		6	20	mV
Load Regulation	$1\text{mA} < I_{REF} < 10\text{mA}$		6	15	mV
NOISE Voltage	(Note 1)		50		$\mu\text{V}$
OP Life Shift	$T = 1000$ Hours (Note 1)		4	20	mV
FAULT Voltage	Force $V_{REF}$	$.92 \times V_{REF}$	$.95 \times V_{REF}$	$.97 \times V_{REF}$	V
OK Voltage	Force $V_{REF}$	$.94 \times V_{REF}$	$.96 \times V_{REF}$	$.98 \times V_{REF}$	V
OK Hysteresis	Force $V_{REF}$	50	105	160	mV
Current Limit	Force $V_{REF}$	-20			mA
<b>■ Error Amplifier</b>					
Initial Accuracy	$T_A = 25^\circ\text{C}$ , $I_{REF} = 2\text{mA}$ , $V_{CC} = 14\text{V}$ , $V_{FB} = \text{COMP}$ (Note 1)	2.465	2.515	2.565	V
Reference Voltage	$V_{FB} = \text{COMP}$	2.440	2.515	2.590	V
$V_{FB}$ Leakage Current	$V_{FB} = 0\text{V}$		-0.2	-2	$\mu\text{A}$
Open Loop Gain	$1.4\text{V} < \text{COMP} < 4\text{V}$ (Note 1)	60	90		dB
Unity Gain Bandwidth	(Note 1)	1.5	2.5		MHz
COMP Sink Current	$\text{COMP} = 1.5\text{V}$ , $V_{FB} = 2.7\text{V}$	2	6		mA
COMP Source Current	$\text{COMP} = 1.5\text{V}$ , $V_{FB} = 2.3\text{V}$	-0.2	-0.5		mA

Electrical Characteristics:  $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ ,  $-40^{\circ}\text{C} < T_J < 150^{\circ}\text{C}$ ,  $3\text{V} < V_C < 20\text{V}$ ,  $8.2\text{V} < V_{CC} < 20\text{V}$ ,  
 $R_T = 12\text{k}\Omega$ ,  $C_T = 390\text{pF}$ , unless otherwise stated

CS51021/22/23/24

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>■ Error Amplifier continued</b>					
COMP High Voltage	$V_{FB} = 2.3\text{V}$	4.35	4.8	5	V
COMP Low Voltage	$V_{FB} = 2.7\text{V}$	0.4	0.8	1.2	V
PS Ripple Rejection	FREQ = 120Hz (Note 1)	60	85		dB
SS Clamp, $V_{COMP}$	$V_{SS} = 2.5\text{V}$ , $V_{FB} = 0\text{V}$ , $I_{SET} = 2\text{V}$	2.4	2.5	2.6	V
$I_{LIM(SET)}$ Clamp	(Note 1)	0.95	1	1.15	V

<b>■ Oscillator</b>					
Accuracy	$R_T = 12\text{k}$ , $C_T = 390\text{pF}$	230	255	280	kHz
Voltage Stability	Delta Frequency $8.2\text{V} < V_{CC} < 20\text{V}$		2	3	%
Temperature Stability	$T_{MIN} < T_A < T_{MAX}$ (Note1)		8		%
Min Charge & Discharge Time	(Note1)	0.333			$\mu\text{s}$
Duty Cycle Accuracy	$R_T = 12\text{k}$ , $C_T = 390\text{pF}$	70	77	83	%
Peak Voltage	(Note 1)		3		V
Valley Voltage	(Note 1)		1.5		V
Valley Clamp Voltage	10k Resistor to ground on $R_T C_T$	1.2	1.4	1.6	V
Discharge Current		0.8	1	1.2	mA
Discharge Current	$T_A = 25^{\circ}\text{C}$ (Note 1)	0.925	1	1.075	mA

<b>■ Synchronization (CS51021/23)</b>					
Input Threshold		1.0	1.5	2.7	V
Output Pulsewidth		160	260	360	ns
Output High Voltage	$I_{SYNC} = 100\mu\text{A}$	3.5	4.3	4.8	V
Input Resistance	(Note 1)	35	70	140	$\text{k}\Omega$
Drive Delay	SYNC to GATE RESET	80	120	150	ns
Output Drive Current	1k Load	1.25	2	3.5	mA

<b>■ SLEEP (CS51022/24)</b>					
SLEEP Input Threshold	Active High	1.0	1.5	2.7	V
SLEEP Input Current	$V_{SLEEP} = 4\text{V}$	11	25	46	$\mu\text{A}$
$I_{CC}$ @ SLEEP	$V_{CC} \leq 15\text{V}$		50	100	$\mu\text{A}$

<b>■ GATE Driver</b>					
HIGH Voltage	Measure $V_C$ -GATE, $V_C = 10\text{V}$ , 150mA Load		1.5	2.2	V
LOW Voltage	Measure GATE-PGnd, 150mA SINK		1.2	1.5	V
HIGH Voltage Clamp	$V_C = 20\text{V}$ , 1nF	11	13.5	16	V
LOW Voltage Clamp	Measured at 10mA Output Current		0.6	0.8	V
Peak Current	$V_C = 20\text{V}$ , 1nF (Note 1)		1		A
UVL Leakage	$V_C = 20\text{V}$ , measured at 0V		-1	-50	$\mu\text{A}$
RISE Time	Load = 1nF, $1\text{V} < \text{GATE} < 9\text{V}$ , $V_C = 20\text{V}$ , $T_A = 25^{\circ}\text{C}$		60	100	ns
FALL Time	Load = 1nF, $9\text{V} > \text{GATE} > 1\text{V}$ , $V_C = 20\text{V}$		15	40	ns

Electrical Characteristics: Unless otherwise stated, specifications apply for  $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ ,  $-40^{\circ}\text{C} < T_J < 150^{\circ}\text{C}$ ,  $3\text{V} < V_C < 20\text{V}$ ,  $8.2\text{V} < V_{CC} < 20\text{V}$ ,  $R_T = 12\text{k}\Omega$ ,  $C_T = 390\text{pF}$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>■ SLOPE Compensation</b>					
Charge Current	SLOPE = 2V	-63	-53	-43	$\mu\text{A}$
COMP Gain	Fraction of slope voltage added to $I_{\text{SENSE}}$ (Note 1)	0.095	0.100	0.105	V/V
Discharge Voltage	SYNC = 0V		0.1	0.2	V
<b>■ Current Sense</b>					
OFFSET Voltage	(Note 1)	0.09	0.10	0.11	V
Blanking Time			55	160	ns
Blanking Disable Voltage	Adjust $V_{\text{FB}}$	1.8	2	2.2	V
Second Current Threshold Gain		1.21	1.33	1.45	V/V
$I_{\text{SENSE}}$ Input Resistance			5		k $\Omega$
Minimum On Time	GATE High to Low	30	70	110	ns
Gain	(Note 1)	0.78	0.80	0.82	V/V
<b>■ OV &amp; UV Voltage Monitors</b>					
OV Monitor Threshold		2.4	2.5	2.6	V
OV Hysteresis Current		-10	-12.5	-15	$\mu\text{A}$
UV Monitor Threshold		1.38	1.45	1.52	V
UV Monitor Hysteresis		25	75	100	mV
<b>■ SOFT START (SS)</b>					
Charge Current	SS = 2V	-70	-55	-40	$\mu\text{A}$
Discharge Current	SS = 2V	250	1000		$\mu\text{A}$
Charge Voltage, $V_{\text{SS}}$		4.4	4.7	5	V
Discharge Voltage, $V_{\text{SS}}$		0.25	0.27	0.30	V

Note 1: Guaranteed by Design, not 100% tested in production.

### Package Pin Description

PACKAGE PIN #	PIN SYMBOL	FUNCTION
<b>16L PDIP &amp; SO Narrow</b>		
1	GATE	External power switch driver with 1.0A peak capability.
2	$I_{\text{SENSE}}$	Current sense amplifier input.
3	SYNC (CS51021/23)	Bi-directional synchronization. Locks to the highest frequency.
3	SLEEP (CS51022/24)	Active high chip disable. In sleep mode, $V_{\text{REF}}$ and GATE are turned off.
4	SLOPE	Additional slope to the current sense signal. Internal current source charges the external capacitor.
5	UV	Undervoltage protection monitor.
6	OV	Overvoltage protection monitor.

PACKAGE PIN #	PIN SYMBOL	FUNCTION
<b>16L PDIP &amp; SO Narrow</b>		
7	$R_T C_T$	Timing resistor $R_T$ and capacitor $C_T$ determine oscillator frequency and maximum duty cycle, $D_{MAX}$ .
8	$I_{SET}$	Voltage at this pin sets pulse-by-pulse overcurrent threshold, and second threshold (1.33 times higher) with Soft Start retrigger (hiccup mode).
9	$V_{FB}$	Feedback voltage input. Connected to the error amplifier inverting input.
10	COMP	Error amplifier output. Frequency compensation network is usually connected between COMP and $V_{FB}$ pins.
11	SS	Charging external capacitor restricts error amplifier output voltage during the start or fault conditions (hiccup).
12	LGnd	Logic ground.
13	$V_{REF}$	5.0V reference voltage output.
14	$V_{CC}$	Logic supply voltage.
15	PGnd	Output power stage ground connection.
16	$V_C$	Output power stage supply voltage.

Block Diagram

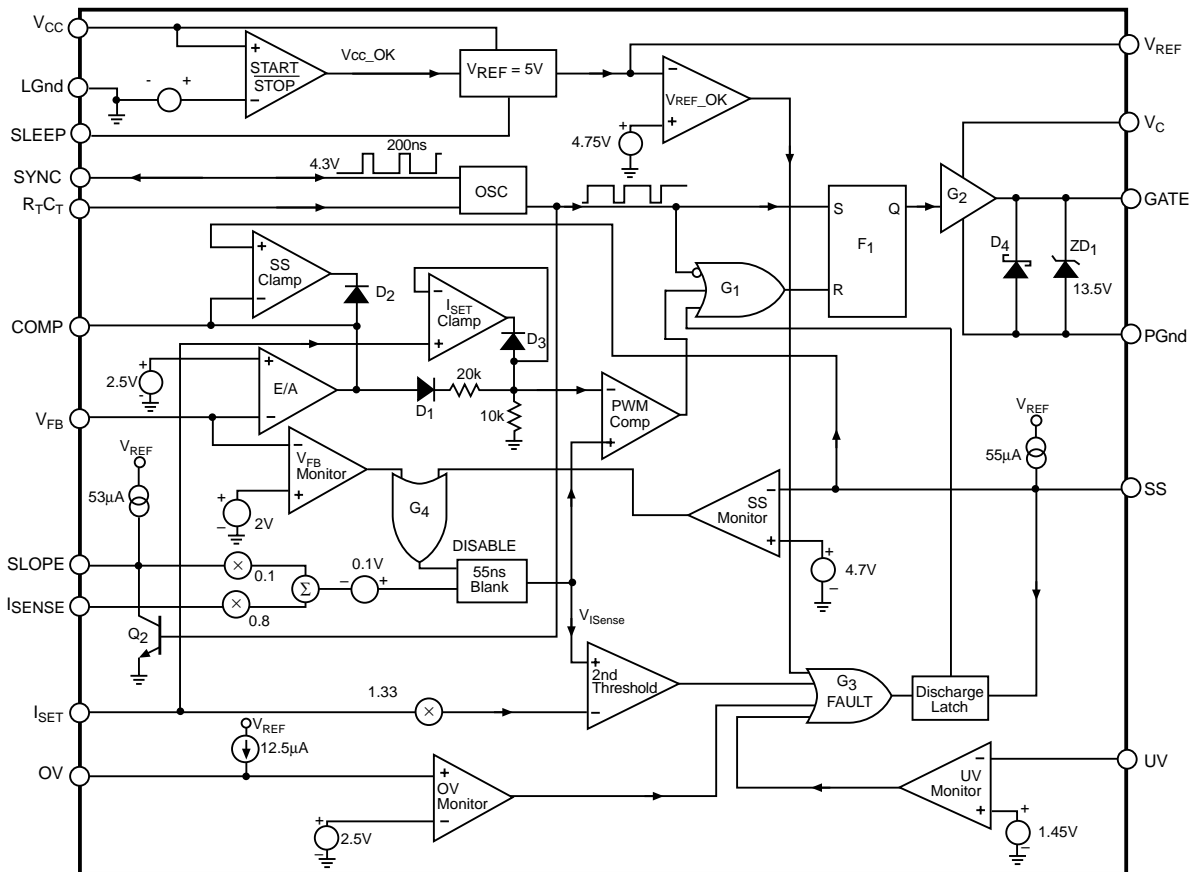


Figure 1: CS51021/22/23/24 Block Diagram

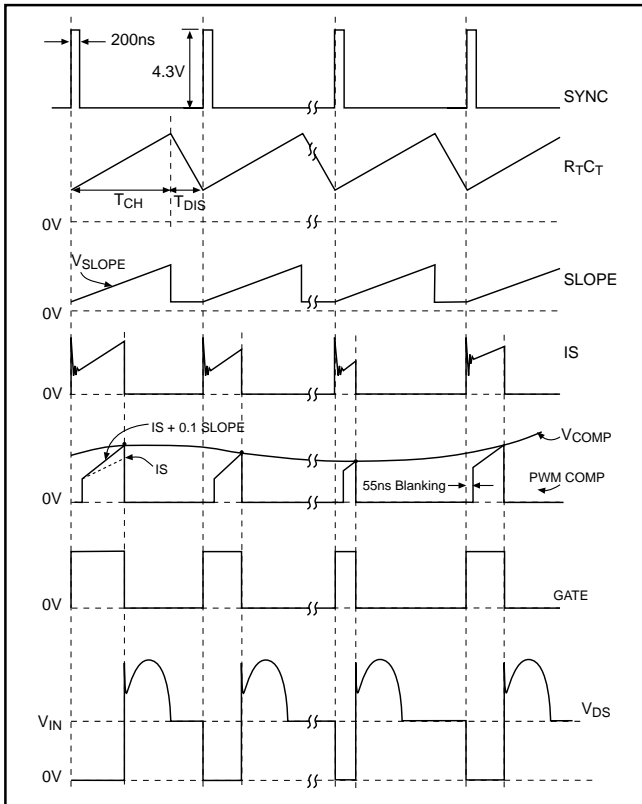


Figure 2: Typical Waveforms

## Theory of Operation

### Powering the IC

The IC has two supply and two ground pins.  $V_C$  and PGnd pins provide high speed power drive for the external power switch.  $V_{CC}$  and LGnd pins power the control portion of the IC. The internal logic monitors the supply voltage,  $V_{CC}$ . During abnormal operating conditions, the output is held low. The CS51021/22/23/24 requires only  $75\mu\text{A}$  of startup current.

### Voltage Feedback

The output voltage is monitored via the  $V_{FB}$  pin and is compared with the internal 2.5V reference. The error amplifier output minus one diode drop is divided by 3 and connected to the negative input of the PWM comparator. The positive input of the PWM comparator is connected to the modified current sense signal. The oscillator turns the external power switch on at the beginning of each cycle. When current sense ramp voltage exceeds the reference side of PWM comparator, the output stage latches off. It is turned on again at the beginning of the next oscillator cycle.

### Current Sense and Protection

The current is monitored at the  $I_{SENSE}$  pin. The CS51021/22/23/24 has leading edge blanking circuitry that ignores the first 55ns of each switching period.

Blanking is disabled when  $V_{FB}$  is less than 2V so that the minimum on-time of the controller does not have an additional 55ns of delay time during fault conditions. For the remaining portion of the switching period, the current sense signal, combined with a fraction of the slope compensation voltage, is applied to the positive input of the PWM comparator where it is compared with the divided by three error amplifier output voltage. The pulse-by-pulse overcurrent protection threshold is set by the voltage at the  $I_{SET}$  pin. This voltage is passed through the  $I_{SET}$  Clamp and appears at the non-inverting input of the PWM comparator, limiting its dynamic range according to the following formula:

Overcurrent Threshold =  $0.8 \times V_{I(SENSE)} + 0.1V + 0.1 V_{SLOPE}$   
where

$V_{I(SENSE)}$  is voltage at the  $I_{SENSE}$  pin

and

$V_{SLOPE}$  is voltage at the SLOPE pin.

During extreme overcurrent or short circuit conditions, the slope of the current sense signal will become much steeper than during normal operation. Due to loop propagation delay, the sensed signal will overshoot the pulse-by-pulse threshold eventually reaching the second overcurrent protection threshold which is 1.33 times higher than the first threshold and is described by the following equation:

$$\text{2nd Threshold} = 1.33 \times V_{I(SET)}$$

Exceeding the second threshold will reset the Soft Start capacitor  $C_{SS}$  and reinitiate the Soft Start sequence, repeating for as long as the fault condition persists.

### Soft Start

During power up, when the output filter capacitor is discharged and the output voltage is low, the voltage across the Soft Start capacitor ( $V_{SS}$ ) controls the duty cycle. An internal current source of  $55\mu\text{A}$  charges  $C_{SS}$ . The maximum error amplifier output voltage is clamped by the SS Clamp. When the Soft Start capacitor voltage exceeds the error amplifier output voltage, the feedback loop takes over the duty cycle control. The Soft Start time can be estimated with the following formula:

$$t_{SS} = 9 \times 10^4 \times C_{SS}$$

The Soft Start voltage,  $V_{SS}$ , charges and discharges between 0.25V and 4.7V.

### Slope Compensation

DC-DC converters with current mode control require a current sense signal with slope compensation to avoid instability at duty cycles greater than 50%. Slope capacitor  $C_S$  is charged by an internal  $53\mu\text{A}$  current source and is discharged during the oscillator discharge time. The slope compensation voltage is divided by 10 and is added to the current sense voltage,  $V_{I(SENSE)}$ . The signal applied to the

input of the PWM comparator is a combination of these two voltages. The slope compensation,  $\frac{dV_{SLOPE}}{dt}$ , is calculated using the following formula:

$$\frac{dV_{SLOPE}}{dt} = 0.1 \times \frac{53\mu A}{C_S}$$

It should be noted that internal capacitance of the IC will cause an error when determining slope compensation capacitance  $C_S$ . This error is typically small for large values of  $C_S$ , but increases as  $C_S$  becomes small and comparable to the internal capacitance. The effect is apparent as a reduction in charging current due to the need to charge the internal capacitance in parallel with  $C_S$ . Figure 3 shows a typical curve indicating this decrease in available charging current.

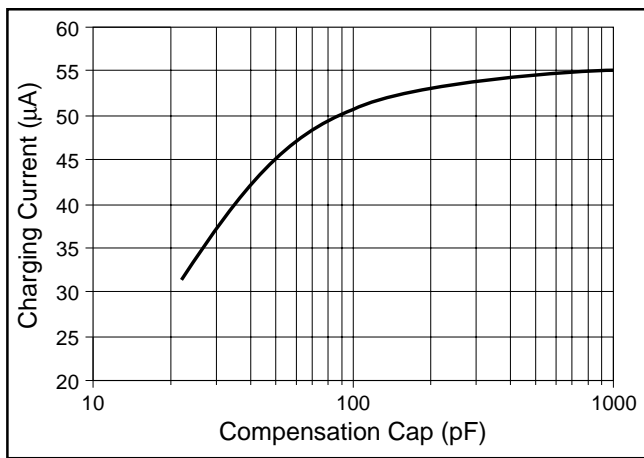


Figure 3: The slope compensation pin charge current reduces when a small capacitor is used.

### Undervoltage (UV) and Overvoltage (OV) Monitor

Two independent comparators monitor OV and UV conditions. A string of three resistors is connected in series between the monitored voltage (usually the input voltage) and ground (see Figure 4). When voltage at the OV pin exceeds 2.5V, an overvoltage condition is detected and GATE shuts down. An internal 12.5µA current source turns on and feeds current into the external resistor,  $R_3$ , creating a hysteresis determined by the value of this resistor (the higher the value, the greater the hysteresis). The hysteresis voltage of the OV monitor is determined by the following formula:

$$V_{OV(HYST)} = 12.5\mu A \times R_3$$

where  $R_3$  is a resistor connected from the OV pin to ground. When the monitored voltage is low and the UV pin is less than 1.45V, GATE shuts down. The UV pin has fixed 75mV hysteresis.

Both OV and UV conditions are latched until the Soft Start capacitor is discharged. This way, every time a fault condition is detected the controller goes through the power up sequence.

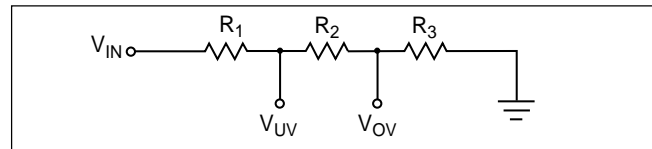


Figure 4: UV/OV Monitor Divider

To calculate the OV/UV resistor divider:

1. Solve for  $R_3$ , based on OV hysteresis requirements.

$$R_3 = \frac{V_{OV(HYST)} \times 2.5V}{V_{MAX} \times 12.5\mu A}$$

where  $V_{OV(HYST)}$  is the desired amount of overvoltage hysteresis, and  $V_{MAX}$  is the input voltage at which the supply will shut down.

2. Find the total impedance of the divider.

$$R_{TOT} = R_1 + R_2 + R_3 = \frac{V_{MAX} \times R_3}{2.5}$$

3. Determine the value of  $R_2$  from the UV threshold conditions.

$$R_2 = \frac{1.45 \times R_{TOT}}{V_{MIN}} - R_3$$

where  $V_{MIN}$  is the UV voltage at which the supply will shut down.

4. Calculate  $R_1$ .

$$R_1 = R_{TOT} - R_2 - R_3$$

5. The undervoltage hysteresis is given by:

$$V_{UV(HYST)} = \frac{V_{MIN} \times 0.075}{1.45}$$

### Synchronization

A bi-directional synchronization is provided to synchronize several controllers. When SYNC pins are connected together, the converters will lock to the highest switching frequency. The fastest controller becomes the master, producing a 4.3V, 200ns pulse train. Only one, the highest frequency SYNC signal, will appear on the SYNC line. For reliable operation, the master frequency should be approximately 20% higher than the free running slave frequency.

### Sleep

The sleep input is an active high input. The CS51022/51024 is placed in sleep mode when SLEEP is driven high. In sleep mode, the controller and MOSFET are turned off. Connect to Gnd for normal operation. The sleep mode operates at  $V_{CC} \leq 15V$ .

### Oscillator and Duty Cycle Limit

The switching frequency is set by  $R_T$  and  $C_T$  connected to the  $R_T C_T$  pin.  $C_T$  charges and discharges between 3V and 1.5V.

The maximum duty cycle is set by the ratio of the on time,  $t_{ON}$ , and the whole period,  $T = t_{ON} + t_{OFF}$ . Because the timing capacitor's discharge current is trimmed, the maximum duty cycle is well defined. It is determined by the ratio between the timing resistor  $R_T$  and the timing capacitor  $C_T$ . Refer to figures 5 and 6 to select appropriate values for  $R_T$  and  $C_T$ .

$$f_{SW} = \frac{1}{T_{SW}}; T_{SW} = t_{CH} + t_{DIS}$$

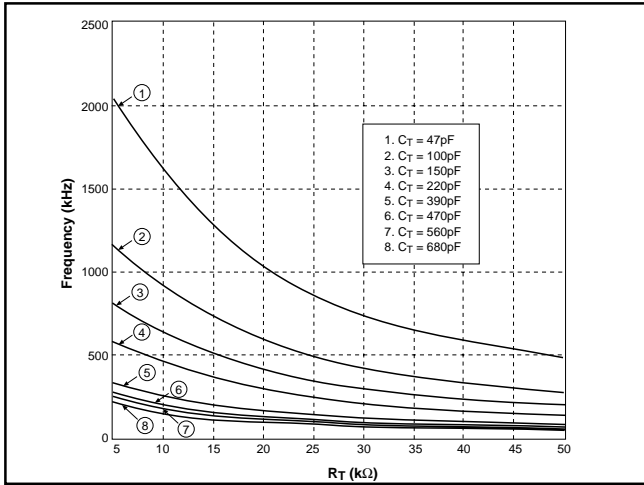


Figure 5: Frequency vs.  $R_T$  for Discrete Capacitor Values.

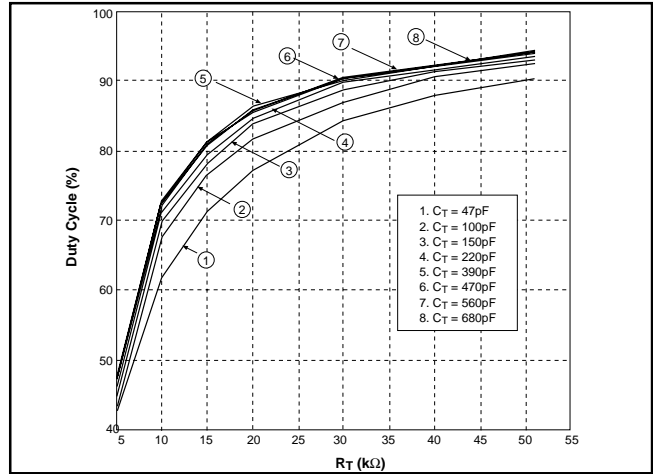


Figure 6: Duty Cycle vs.  $R_T$  for Discrete Capacitor Values.



## Package Specification

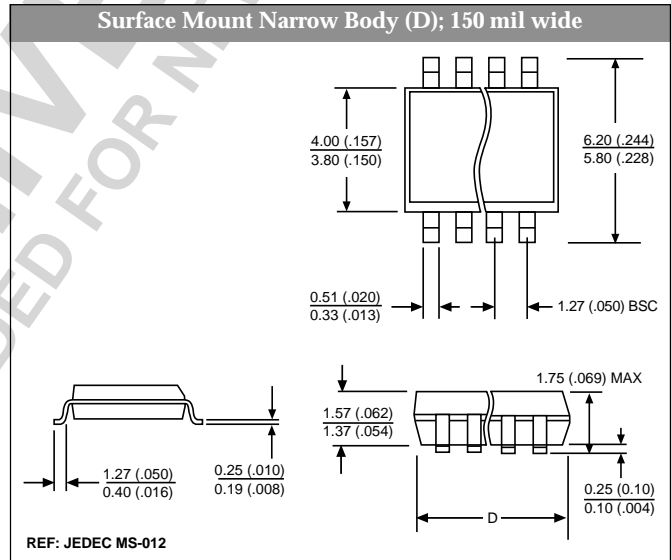
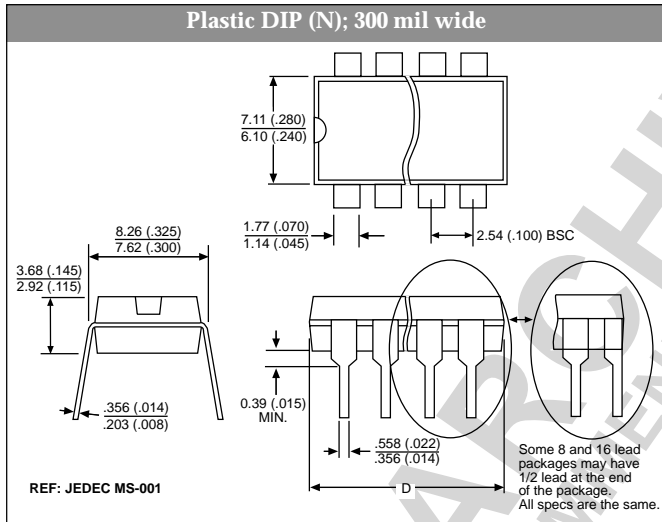
CS51021/22/23/24

### PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
16L SO Narrow	10.00	9.80	.394	.386
16L PDIP	19.69	18.67	.775	.735

### PACKAGE THERMAL DATA

Thermal Data		16L SO Narrow	PDIP	
$R_{\theta JC}$	typ	28	42	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	typ	115	80	$^{\circ}\text{C}/\text{W}$



### Ordering Information

Part Number	Description
CS51021ED16	16L SO Narrow
CS51021EDR16	16L SO Narrow (tape & reel)
CS51022ED16	16L SO Narrow
CS51022EDR16	16L SO Narrow (tape & reel)
CS51023ED16	16L SO Narrow
CS51023EDR16	16L SO Narrow (tape & reel)
CS51024ED16	16L SO Narrow
CS51024EDR16	16L SO Narrow (tape & reel)
CS51021EN16	16L PDIP
CS51022EN16	16L PDIP
CS51023EN16	16L PDIP
CS51024EN16	16L PDIP

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