ANALOG DEVICES

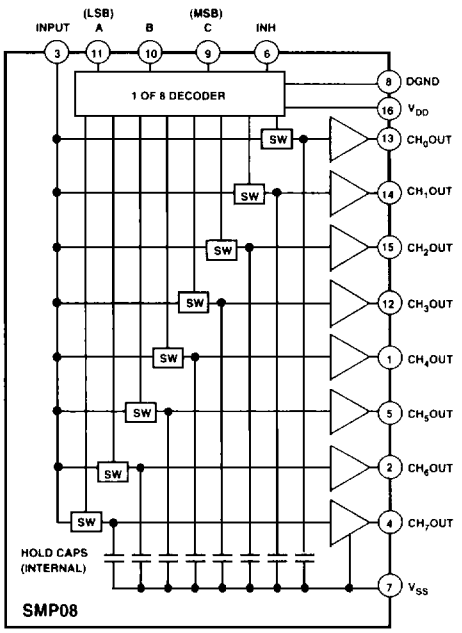
Octal Sample-and-Hold with Multiplexed Input

SMP08*

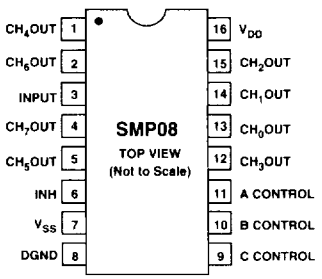
FEATURES
- Internal Hold Capacitors
- Low Droop Rate
- TTL/CMOS Compatible Logic Inputs
- Single or Dual Supply Operation
- Break-Before-Make Channel Addressing
- Compatible With CD4051 Pinout
- Low Cost

APPLICATIONS
- Multiple Path Timing Deskew for A.T.E.
- Memory Programmers
- Mass Flow/Process Control Systems
- Multichannel Data Acquisition Systems
- Robotics and Control Systems
- Medical and Analytical Instrumentation
- Event Analysis
- Stage Lighting Control

FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTION



GENERAL DESCRIPTION

The SMP08 is a monolithic octal sample-and-hold; it has eight internal buffer amplifiers, input multiplexer, and internal hold capacitors. It is manufactured in an advanced oxide isolated CMOS technology to obtain high accuracy, low droop rate, and fast acquisition time. The SMP08 has a typical linearity error of only 0.01% and can accurately acquire a 10-bit input signal to ±1/2 LSB in less than 7 microseconds. The SMP08's output swing includes the negative supply in both single and dual supply operation.

The SMP08 was specifically designed for systems that use a calibration cycle to adjust a multiple of system parameters. The low cost and high level of integration make the SMP08 ideal for calibration requirements that have previously required an ASIC, or high cost multiple D/A converters.

The SMP08 is also ideally suited for a wide variety of sample-and-hold applications including amplifier offset or VCA gain adjustments. One or more SMP08s can be used with single or multiple DACs to provide multiple set points within a system.

The SMP08 offers significant cost and size reduction over discrete designs. It is available in a 16-pin hermetic or plastic DIP, or surface-mount SOIC package.

***Manufactured under the following U.S. patent: 4,739,281**

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
SMP08FQ	–40°C to +85°C	Cerdip	Q-16
SMP08FP	–40°C to +85°C	Plastic DIP	N-16
SMP08FS	–40°C to +85°C	SO-16	R-16A

*For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

SMP08–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

(@ V_{DD} = +5 V, V_{SS} = –5 V, DGND = 0 V, R_L = No Load, T_A = –40°C to +85°C for SMP08F, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Linearity Error		3 V ≤ V_{IN} ≤ +3 V		0.01		%
Buffer Offset Voltage	V_{OS}	T_A = +25°C		2.5	10	mV
		40°C ≤ T_A ≤ +85°C		3.5	20	mV
Hold Step	V_{HS}	V_{IN} = 0 V, T_A = +25°C to +85°C		2.8	4	mV
		V_{IN} = 0 V, T_A = –40°C			5	mV
Droop Rate	$\Delta V_{CH}/\Delta t$	T_A = +25°C, V_{IN} = 0 V		2	20	mV/s
Output Source Current	I_{SOURCE}	V_{IN} = 0 V[1]	1.2			mA
Output Sink Current	I_{SINK}	V_{IN} = 0 V[1]	0.5			mA
Output Voltage Range		R_L = 20 kΩ	3.0		+3.0	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4			V
Logic Input Low Voltage	V_{INL}				0.8	V
Logic Input Current	I_{IN}	V_{IN} = 2.4 V		0.5	1	µA
DYNAMIC PERFORMANCE[2]						
Acquisition Time	t_{AQ}	T_A = +25°C, 3 V to +3 V to 0.1%		3.6		µs
Hold Mode Settling Time	t_H	To +1 mV of Final Value		1		µs
Channel Select Time	t_{CH}			90		ns
Channel Deselect Time	t_{DCS}			45		ns
Inhibit Recovery Time	t_{IR}			90		ns
Slew Rate	SR			3		V/µs
Capacitive Load Stability		< 30% Overshoot		500		pF
Analog Crosstalk		3 V to +3 V Step		72		dB
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	V_S = ±5 V to ±6 V	60	75		dB
Supply Current	I_{DD}	T_A = +25°C		4	7.5	mA
		40°C ≤ T_A ≤ +85°C		5	9.5	

NOTES

[1]Outputs are capable of sinking and sourcing over 20 mA but offset is guaranteed at specified load levels.

[2]All input control signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to DGND ..... 0.3 V, 17 V
V_{DD} to V_{SS} ..... 0.3 V, 17 V
V_{LOGIC} to DGND ..... 0.3 V, V_{DD}
V_{IN} to DGND ..... V_{SS}, V_{DD}
V_{OUT} to DGND ..... V_{SS}, V_{DD}
Analog Output Current ..... +20 mA
(Not short-circuit protected)
Operating Temperature Range
FP, FS ..... –40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature ..... 65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
16-Pin Hermetic DIP (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOIC (S)	92	27	°C/W

NOTES

[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

[2]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and plastic DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the SMP08 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.