HARRIS

RFP50N05
RFG50N05

N-Channel Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

May 1992

Features

- 50A, 50V
- $r_{DS(on)} = 0.022\Omega$
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature

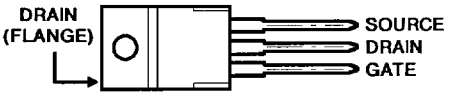
Description

The RFP50N05 and RFG50N05 n-channel power MOSFET's are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors.

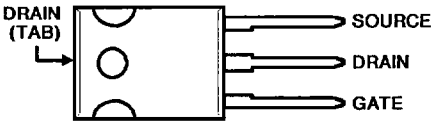
The RFP50N05 is supplied in the JEDEC TO-220AB plastic package and the RFG50N05 is supplied in the TO-247 plastic package.

Package

TO-220AB
TOP VIEW

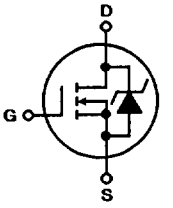


TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	RFP50N05 RFG50N05	UNITS
Drain-Source Voltage ..... V_{DSS}	50	V
Drain-Gate Voltage (R_{GS} = 1 MΩ) ..... V_{DGR}	50	V
Continuous Drain Current ..... I_D	50	A
Pulsed Drain Current ..... I_{DM}	120	A
Gate-Source Voltage ..... V_{GS}	±20	V
Maximum Power Dissipation		
T_C = +25°C ..... P_D	132	W
Derated Above +25°C	0.88	W/°C
Operating and Storage Junction Temperature Range ..... T_{JC}, T_{STG}	-55 to +175	°C
Single-Pulse Avalanche Ratings	Refer to UIS SOA Curve	

Caution: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Copyright © Harris Corporation 1992

File Number 2873.1

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D =0.25mA, V_{GS} = 0V		50	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, I_D = 0.25mA		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =40V, V_{GS} = 0V		-	-	1	µA
		T_C =+150°C		-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(on)}$	I_D = 50A, V_{GS} = 10V		-	-	0.022	Ω
Turn-On Time	$t_{(on)}$	V_{DD} = 25V, I_D = 25A, R_L = 1.0Ω, $I_{G1} = I_{G2}$ = 1.5A, $V_{GS(clamp)}$ = +10V, -0.6V		-	-	100	ns
Turn-On Delay Time	$t_{d(on)}$			-	15	-	ns
Rise Time	t_r			-	55	-	ns
Turn-Off Delay Time	$t_{d(off)}$			-	60	-	ns
Fall Time	t_f			-	15	-	ns
Turn-Off Time	$t_{(off)}$			-	-	100	ns
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = 0-20V	V_{DD} = 40V	-	-	160	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0-10V	I_D = 50A	-	-	80	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} =0-2V	R_L = 0.8Ω	-	-	6	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 50A, V_{DS} = 15V		-	-	7.5	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25V, I_D = 25A, $I_{G1} = I_{G2}$ = 1.5A, $V_{GS(clamp)}$ = +10V, -0.6V, L = 0.2µH, R_L = 1.0Ω		-	-	150	µJ
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.14	°C/W
Thermal Resistance Diode Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 50A	-	-	1.5	V
Reverse Recovery Time	t_{rr}	I_f = 50A, dI_f/dt = 100A/µs	-	-	125	ns

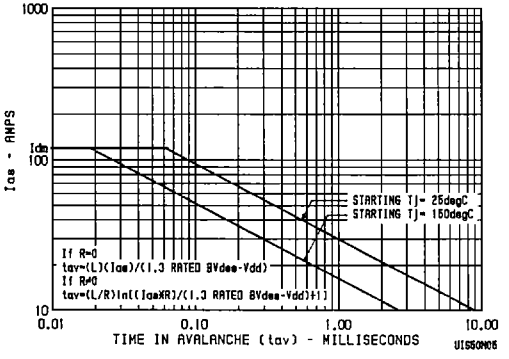


FIGURE 1. UNCLAMPED-INDUCTIVE-SWITCHING SOA (SINGLE PULSE UIS SOA)

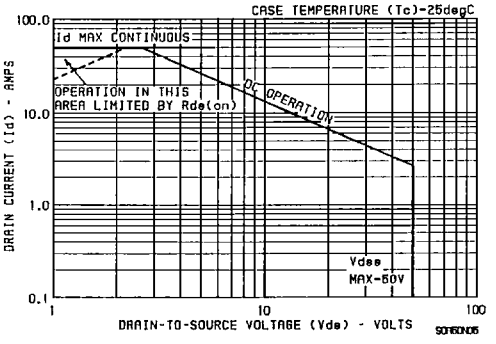


FIGURE 2. SAFE-OPERATING-AREA CURVE. (CURVES MUST BE DERATED LINEARLY WITH INCREASE IN CASE TEMPERATURE)

Performance Curves

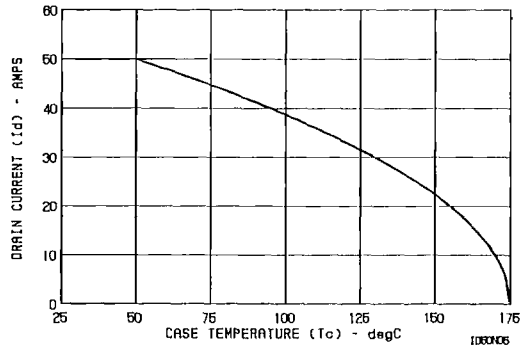


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT VS. TEMPERATURE

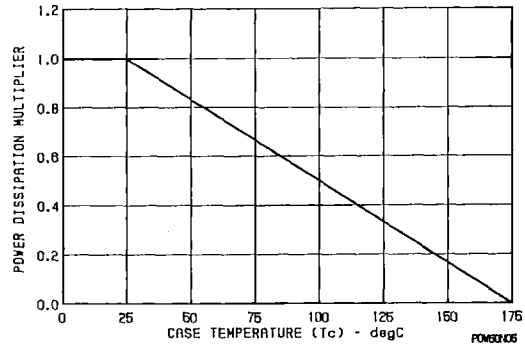


FIGURE 4. NORMALIZED POWER DISSIPTION VS. TEMPERATURE DERATING CURVE

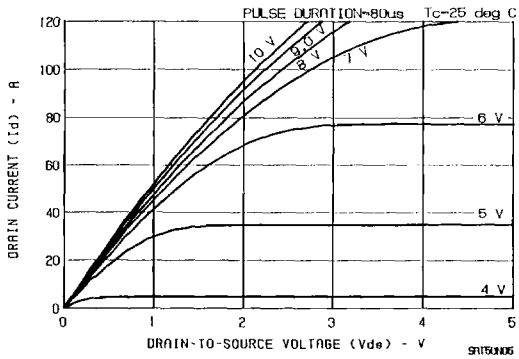


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

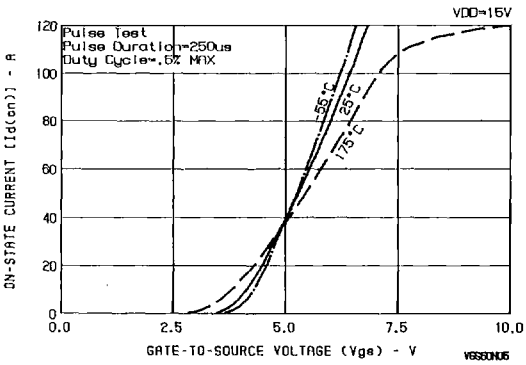


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

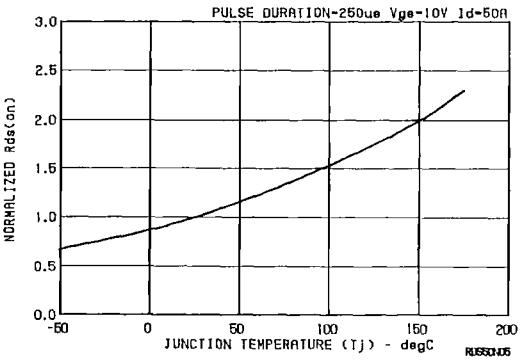


FIGURE 7. NORMALIZED $r_{DS(on)}$ VS. JUNCTION TEMPERATURE

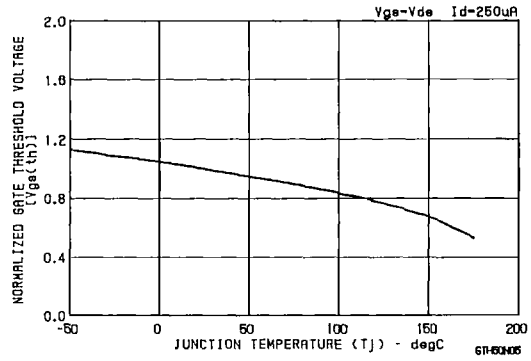


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE

Performance Curves (Continued)

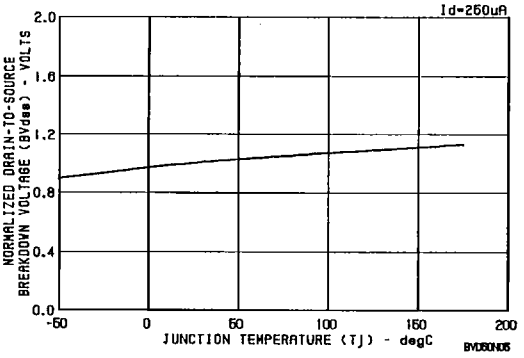


FIGURE 9. NORMALIZED DRAIN-TO-SOURCE BREAKDOWN VOLTAGE VS. TEMPERATURE

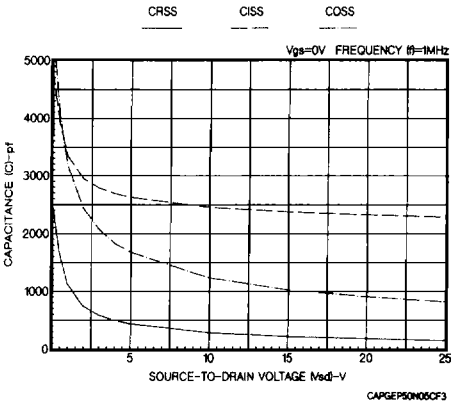


FIGURE 10. TYPICAL CAPACITANCE VS. VOLTAGE FOR ALL TYPES

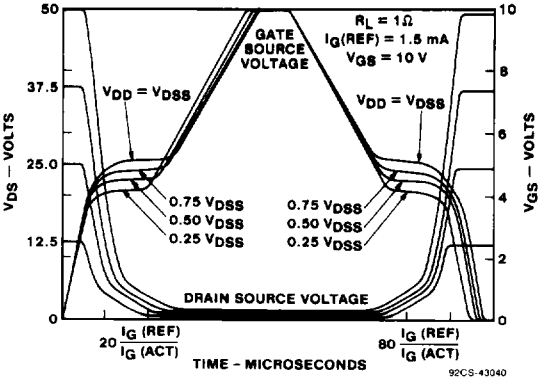


FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE-CURRENT. (REFER TO HARRIS APPLICATION NOTES AN-7254 AND AN-7260)

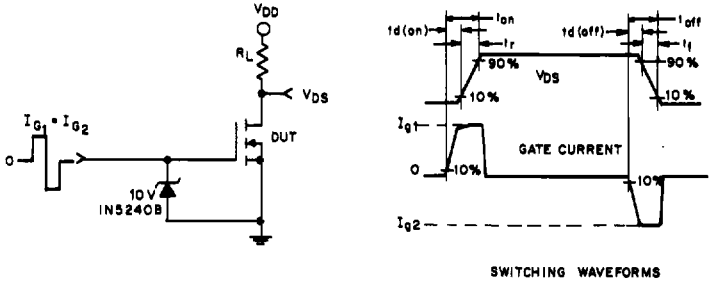


FIGURE 12. RESISTIVE SWITCHING

Performance Curves (Continued)

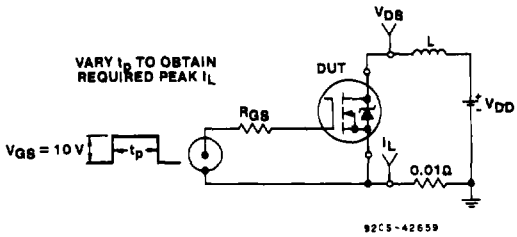


FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

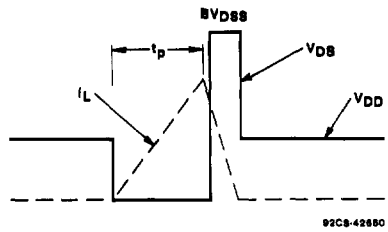


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS