Flexible Condition Monitoring Platform

Data Sheet

ADMW1001

FEATURES

- Enabled by the MeasureWare ecosystem
- Rapid configuration
- Upgradeable firmware enabling new features
- Complete measurement node (sensor excitation, sensor measurement, and sensor compensation)
- Directly digitizes compensated and uncompensated sensors
- Sensors include:
  - RTD
  - Thermocouple
  - Wheatstone bridge
- Embedded linearization for 2-/3-wire PT100/1000 RTDs
- J, K, T, and custom type thermocouples
- Supports custom lookup tables
- Supports selected I²C/SPI sensors
- 2 thermocouple channels
- 2 universal (4-/6-wire bridge, RTD, ratiometric referencing) channels
- Embedded FIFO
- Multiple diagnostics
- Per measurement configuration (sensor type, settling time, gain, excitation currents, linearization, speed)
- Configurable cycle sampling time
- Embedded sequencer
- Simultaneous 50 Hz and 60 Hz antialiasing rejection
- SPI communications interface
- Power supply voltage: 3.3 V
- Operating temperature range: −40°C to +85°C

APPLICATIONS

- Asset health monitoring
- Laboratory instrumentation
- Smart agriculture
- Supply chain health tracking
- Condition profiling

FUNCTIONAL BLOCK DIAGRAM

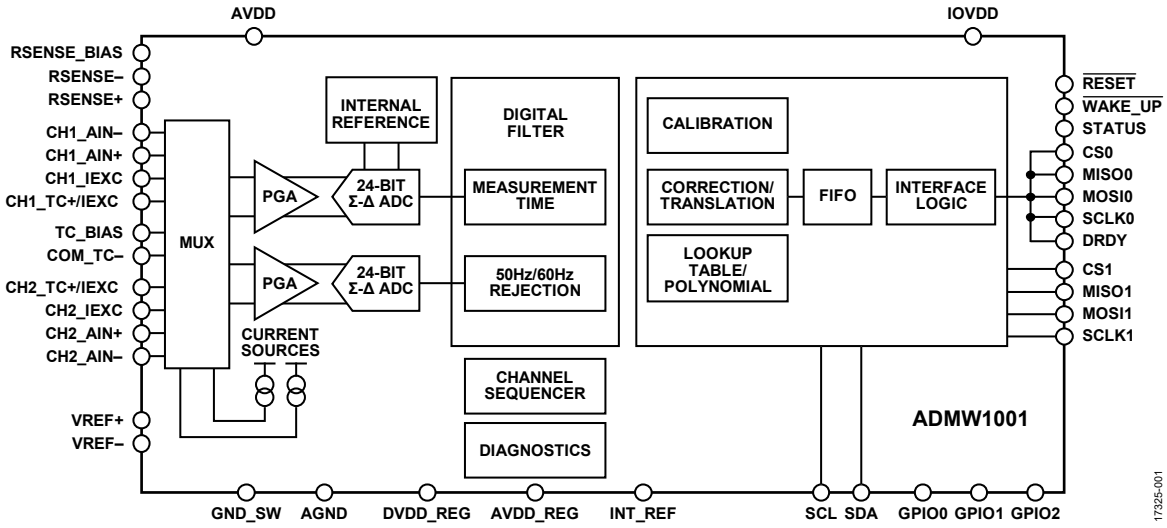

Figure 1.

Rev. 0 Document Feedback

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REVISION HISTORY

7/2019—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADMW1001 offers a flexible and versatile IC that directly connects to a range of sensors, which includes temperature and humidity sensors. The device has all of the building blocks to excite, measure, and correct the sensor and generate an output in sensor related units such as °C, °F, and psi. In conjunction with the MeasureWare® ecosystem, the ADMW1001 can be easily configured and optimized for the sensor types selected to meet the accuracy and measurement times required.

The ADMW1001 is a highly flexible device with a feature set and sensor library that is designed to evolve over time. As additional functionality is developed, it becomes available, and it can be flashed to the device during printed circuit board (PCB) manufacturing or upgraded in the field through the custom flash loader tool set.

The ADMW1001 can also be ordered preprogrammed with a specific revision of the firmware preloaded. Contact Analog Devices, Inc., for more information.

The ADMW1001 is shipped with a firmware loader and requires flashing of the most recent version of ADMW1001 firmware to enable the growing list of measurement techniques and features available with MeasureWare. All firmware revisions for the ADMW1001 are available through the ADMW1001 product page and the MeasureWare Studio.

The ADMW1001 firmware revision 1.0 directly supports compensated J–, K–, and T–type thermocouples, and PT100 (platinum RTD, 100 Ω at 0°C) and PT1000 (platinum RTD, 1000 Ω at 0°C) 2-/3-wire resistance temperature detectors (RTD). Linearization for these sensors is automatically handled by the ADMW1001. The ADMW1001 also allows the user to connect custom sensors. In addition to various types of RTDs and thermocouples, the device can interface to 4-wire bridges, such as pressure or strain transducers. Lookup tables can be written to the ADMW1001, enabling fully corrected measurements for custom sensors. Each revision of the firmware has an associated user guide, which can be found on the ADMW1001 product page.

The device has two universal measurement channels that connect to RTDs, 4-wire bridges, and any custom voltage output sensor.

The device also has two thermocouple inputs. Thermocouple inputs are available on CH1_TC+/IEXC and CH2_TC+/IEXC with a shared COM_TC− pin. The TC_BIAS pin must be used to bias the thermocouples to midscale.

When a channel is configured as a thermocouple or voltage input channel, it can also support compensation sensors per channel, in the form of 2-wire and 3-wire RTDs to be used as temperature compensation or cold junction compensation.

The ADMW1001 includes two I^2C measurement inputs and one serial peripheral interface (SPI) measurement input. These inputs are useful for compensated sensors such as pressure, humidity, and accelerometers. The ADMW1001 measures these sensors and generates an output in sensor related units.

The ADMW1001 features programmable measurement time, which enables customization of measurement, speed, and power consumption. Measurement intervals from seconds to milliseconds are supported. The ADMW1001 also supports simultaneous 50 Hz and 60 Hz antialiasing rejection, which is a key requirement in designs where rejection of interference from the main power supply is required.

With the ADMW1001 per measurement configuration and on-chip measurement sequencer, the user can configure each measurement being used at one time and input the number of measurements required from each measurement channel, and the sequencer automatically steps through the cycle. Via a choice of interface modes, the measurement results can be accessed immediately when available. Alternatively, the on-chip first in, first out (FIFO) can hold the results, and all results can then be read at one time by the host processor. This functionality minimizes the workload on the host processor. Cycle time can be set to determine the interval at which the cycle is repeated. This is useful in systems such as environmental monitoring, where measurements are not needed continuously but at intervals of hours or days. The device enters a low power state during these intervals, which can extend the battery life.

Multiple embedded diagnostics assist the user in designing a robust system. Diagnostics such as open wire detection, short-circuit detection, and checks on customer-entered lookup tables ensure that sensors are connected to the inputs and that the device is configured correctly.

The device operates with a single power supply of 3.3 V. It is specified for a temperature range of −40°C to +85°C, has a size of 7 mm × 7 mm, and is a 48-lead LFCSP.

SPECIFICATIONS

AVDD/IOVDD = 3.3 V, internal 1.2 V reference, all specifications at T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC SPECIFICATIONS	ADC0 and ADC1				
Conversion Rate[1]		5		976	Hz
No Missing Codes[1]	f_{ADC} ≤ 250 Hz	24			Bits
Root Mean Squared Noise and Data Output Rates					
	Gain = 1, ADC speed = 5 Hz			10	µV
	Gain = 8, ADC speed = 5 Hz			1	µV
	Gain = 1, ADC speed = 122 Hz			20	µV
	Gain = 8, ADC speed = 122 Hz			4	µV
Integral Nonlinearity[1]	Gain = 1	−30	±10	+30	ppm of FSR
	Gain = 8	−50		+50	ppm of FSR
	Gain = 2, 4, or 16		±15		ppm of FSR
	Gain = 32, 64, or 128		±20		ppm of FSR
Offset Error[2, 3, 4, 5, 6]	Chop off		±230/gain		µV
	Chop on, gain = 1	−10	±1.0	+10	µV
	Chop on, gain = 8	−2		+2	µV
	Chop on. gain ≥ 16		±1.0		µV
Offset Error Drift vs. Temperature[1, 4, 5]	Chop off, gain ≤ 4		1/gain		µV/°C
	Chop off, gain ≥ 8		230		nV/°C
	Chop on		10		nV/°C
Offset Error Lifetime Stability[7]	Gain = 128		1		µV/1000 Hr
Full-Scale Error[1, 4, 5, 6, 8]	Gain = 1	−500		+500	µV
	Gain = 8	−500		+500	µV
Full-Scale Error Lifetime Stability[7]	Gain = 128		70		µV/1000 Hr
Gain Error Drift vs. Temperature[1, 4, 5]	External reference				
	Gain = 1, 2, 4, 8, or 16		±3		ppm/°C
	Gain = 32, 64, or 128		±6		ppm/°C
Programmable Gain Amplifier (PGA) Gain Mismatch Error			±0.15		%
Power Supply Rejection[1]	External reference				
	Chop on, ADC input = 0.25 V, gain = 4	95			dB
	Chop off, ADC input = 7.8 mV, gain = 128	80			dB
	Chop off, ADC input = 1 V, gain = 1	90			dB
Absolute Input Voltage Range					
Unbuffered Mode		AGND		AVDD	V
Buffered Mode	Available for all gain settings G = 1 to 128	AGND + 0.1		AVDD − 0.1	V
Differential Input Voltage Ranges[1]					
	Gain = 1			$\pm V_{REF}$	V
	Gain = 2			±500	mV
	Gain = 4			±250	mV
	Gain = 8			±125	mV
	Gain = 16			±62.5	mV
Common-Mode Voltage (V_{CM})[1]	Ideally, V_{CM} = ((AIN+) + (AIN−))/2, gain = 2 to 128, input current varies with V_{CM}	AGND		AVDD	V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Input Current					
Buffered Mode	Gain 1, 8	−20	+2	+20	nA
	Gain 2, 4, ≥16		2		nA
Unbuffered Mode	Input current varies with input voltage		860		nA/V
Average Input Current Drift[1]					
Buffered Mode	CH1_AIN+, CH1_TC+/IEXC, CH2_IEXC, RSENSE+		±5		pA/°C
	RSENSE−, CH1_IEXC, CH2_AIN−, COM_TC−		±9		pA/°C
	CH1_AIN−, CH2_TC+/IEXC, CH2_AIN+		±15		pA/°C
Unbuffered Mode			±250		pA/V/°C
Common-Mode Rejection, DC[1]	On ADC input				
	ADC gain = 1, AVDD < 2 V	65	100		dB
	ADC gain = 1, AVDD > 2 V	80	100		dB
	ADC gain = 2 to 128	80			dB
Common-Mode Rejection, Simultaneous 50 Hz and 60 Hz Antialiasing Rejection[1]	50 Hz and 60 Hz ± 1 Hz, f_{ADC} = 8.24 Hz				
	ADC gain = 1	97			dB
	ADC gain = 2 to 128	90			dB
Normal Mode Rejection, 50 Hz and 60 Hz[1]	On ADC input				
	50 Hz and 60 Hz ± 1 Hz, f_{ADC} = 8.24 Hz, chop on, f_{ADC} = 50 Hz, chop off	60	80		dB
GROUND SWITCH					
On Resistance (R_{ON})		3.7	10	19	Ω
Allowable Current[1]	20 kΩ resistor off, direct short to ground			20	mA
VOLTAGE REFERENCE	V_{REF} = ADC internal reference				
Internal V_{REF}			1.2		V
Initial Accuracy	Measured at T_A = 25°C	−0.1		+0.1	%
Reference Temperature Coefficient (TC)[1, 9]		−15	±5	+15	ppm/°C
Power Supply Rejection[1]		82	90		dB
EXTERNAL REFERENCE INPUTS					
Input Range					
Buffered Mode		AGND + 0.1		AVDD − 0.1	V
Unbuffered Mode	Minimum differential voltage between VREF+ and VREF− pins is 400 mV	0		AVDD	V
Input Current					
Buffered Mode		−20	+10	+27	nA
Unbuffered Mode			500		nA/V
Normal Mode Rejection[1]			80		dB
Common-Mode Rejection[1]		85	100		dB
Reference Detect Levels[1]			400		mV
EXCITATION CURRENT SOURCES					
Output Current	Available from each current source, value is programmable from 10 µA to 1 mA	10		1000	µA
Initial Tolerance at 25°C[1]	Excitation output current (I_{OUT}) ≥ 50 µA		±5		%
Accuracy	10 µA setting	8		15	µA
	250 µA setting	200		300	µA
Drift[1]	Using an internal reference resistor		100	400	ppm/°C
Initial Current Matching at 25°C[1]	Matching between both current sources		±0.5		%
Drift Matching[1]			50		ppm/°C
Load Regulation	AVDD[1] = 3.3 V		0.2		%/V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Output Compliance[1]	I_{OUT} = 10 µA to 210 µA	AGND – 0.03		AVDD – 0.85	V
	I_{OUT} > 210 µA	AGND – 0.03		AVDD – 1.1	V
POWER-ON RESET (POR)					
POR Trip Level	Voltage at IOVDD pin				
	Power-on level		1.65		V
	Power-down level		1.65		V
Timeout from POR[1]			50		ms
DIGITAL INPUTS	All digital inputs				
Input Leakage Current	Digital inputs except for the $\overline{RESET}$				
Logic 1	Voltage input high (V_{INH}) = IOVDD or V_{INH} = 1.8 V		140		µA
	Internal pull-up disabled		1		nA
Logic 0	Voltage input low (V_{INL}) = 0 V		160		µA
	Internal pull-up disabled		10		nA
Input Leakage Current	$\overline{RESET}$				
Logic 1			140		µA
Logic 0			160		µA
Input Capacitance[1]			10		pF
Logic Input Voltage					
Low, V_{INL}				0.2 × IOVDD	V
High, V_{INH}		0.7 × IOVDD			V
Logic Output Voltage					
High, Voltage Output High (V_{OH})	Current Source (I_{SOURCE}) = 1 mA	IOVDD – 0.4			V
Low, Voltage Output Low (V_{OL})	Current Sink (I_{SINK}) = 1 mA			0.4	V
START-UP TIME[1]					
After Reset Event	Time to first sample		100		ms
Wake-Up Time			50		µs
POWER REQUIREMENTS					
Power Supply Voltages, Supply Voltage (V_{DD})	AVDD, IOVDD		3.3		V
Power Consumption					
Supply Current (I_{DD}) (Active Mode)			5	6	mA
I_{DD} (Hibernation)			15		µA

[1] These numbers are not production tested but are guaranteed by design and/or characterization data at production release.
[2] Tested at gain = 4 after initial offset calibration.
[3] Measured with a short-circuit of the analog input pins. A system zero-scale calibration removes this error.
[4] A recalibration at any temperature removes these errors.
[5] These numbers do not include internal reference temperature drift.
[6] Factory calibrated at gain = 1.
[7] The long-term stability specification is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.
[8] System calibration at a specific gain removes the error at this gain.
[9] Measured using the box method.

TIMING CHARACTERISTICS

SPI Master Interface Timing Specifications

Table 2. SPI Slave Mode Timing

Parameter	Description	Min	Typ	Max	Unit
t_{CS0}	CS0 to SCLK0 edge	62.5			ns
t_{SL}	SCLK0 low pulse width[1]	125			ns
t_{SH}	SCLK0 high pulse width[1]	125			ns
t_{DAV}	Data output valid after SCLK0 edge			49.1	ns
t_{DSU}	Data input setup time before SCLK0 edge	20.2			ns
t_{DHD}	Data input hold time after SCLK0 edge	10.1			ns
t_{DF}	Data output fall time		12	35.5	ns
t_{DR}	Data output rise time		12	35.5	ns
t_{SR}	SCLK0 rise time		12	35.5	ns
t_{SF}	SCLK0 fall time		12	35.5	ns
t_{SFS}	CS0 high after SCLK0 edge	0			ns
t_{12}	CS0 low to CS0 high time		60		µs

[1] Slave SPI interface operates in Mode 0. Clock polarity (CPOL) = clock phase (CPHA) = 0.

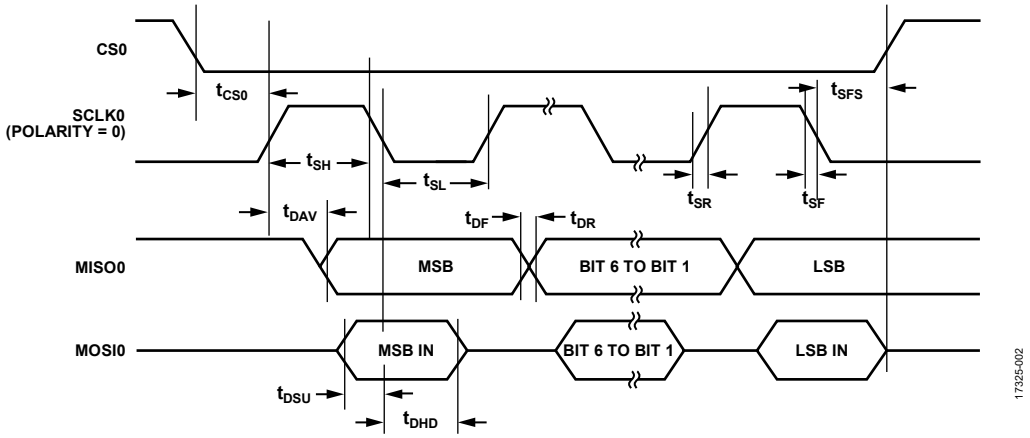

Figure 2. SPI Slave Mode Timing

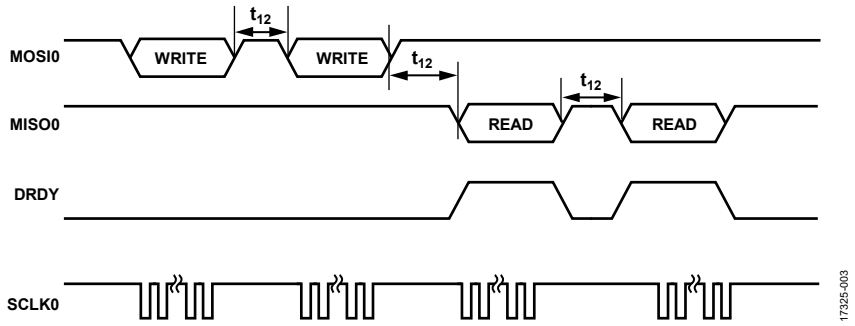

Figure 3. Delay Between Consecutive Serial Operations

SENSOR INTERFACE TIMING SPECIFICATIONS

SPI Timing Specifications

Table 3. SPI Master Mode Timing

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK1 low pulse width[1]	62.5	500		ns
t_{SH}	SCLK1 high pulse width[1]		500		ns
t_{DAV}	Data output valid after SCLK1 edge		0	35.5	ns
t_{DOSU}	Data output setup time before SCLK1 edge[1]	((SPIDIV + 1) × t_{UCLK})/2			ns
t_{DSU}	Data input setup time before SCLK1 edge	58.7			ns
t_{DHD}	Data input hold time after SCLK1 edge	16			ns
t_{DF}	Data output fall time		12	35.5	ns
t_{DR}	Data output rise time		12	35.5	ns
t_{SR}	SCLK1 rise time		12	35.5	ns
t_{SF}	SCLK1 fall time		12	35.5	ns

[1] SPIDIV = 8 MHz/SPI_CLK_SPEED. There are 16 SPI_CLK_SPEED options available for slave devices from 8 MHz to 244 Hz.

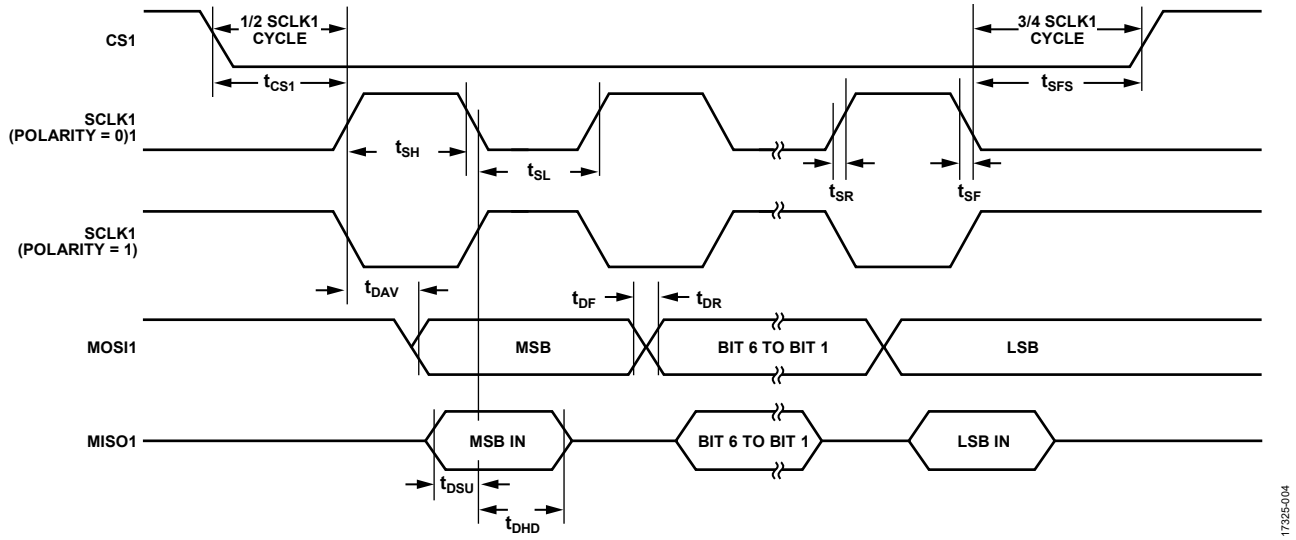

Figure 4. SPI Master Mode Timing (Phase Mode = 1)

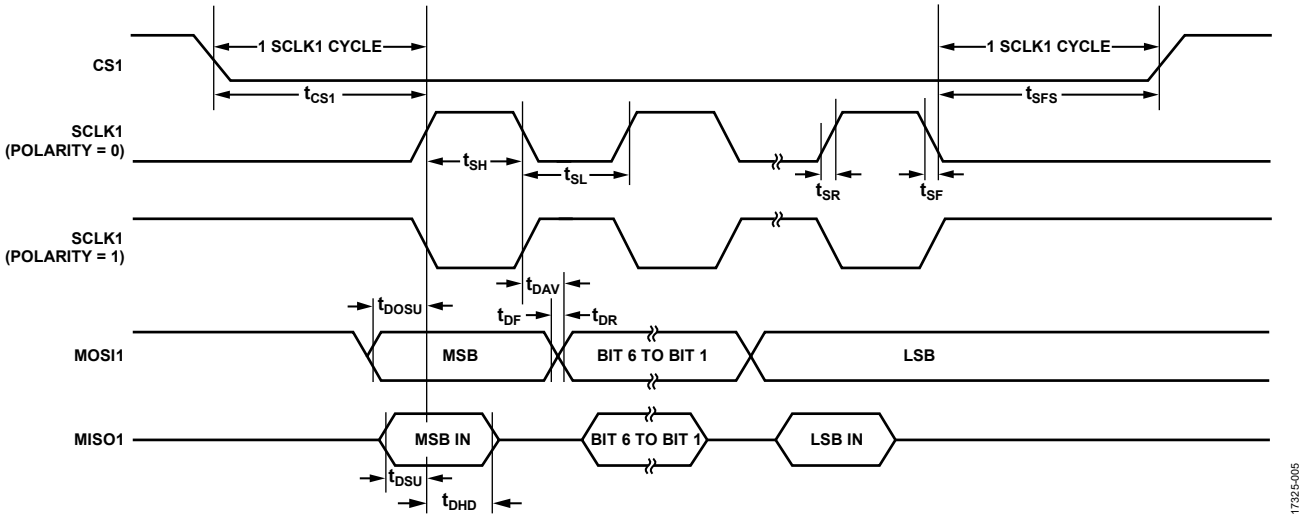

Figure 5. SPI Master Mode Timing (Phase Mode = 0)

I²C Sensor Timing Specifications

The capacitive load for each I²C bus line (C_B) is 400 pF maximum as per the I²C bus specifications. I²C timing is guaranteed by design but is not production tested.

Table 4. I²C Timing in Fast Mode (400 kHz)

Parameter	Description	Min	Max	Unit
t_L	Serial clock (SCL) low pulse width	1300		ns
t_H	SCL high pulse width	600		ns
t_{SHD}	Start condition hold time	600		ns
t_{DSU}	Data setup time	100		ns
t_{DHD}	Data hold time	0		ns
t_{RSU}	Setup time for repeated start	600		ns
t_{PSU}	Stop condition setup time	600		ns
t_{BUF}	Bus free time between a stop condition and a start condition	1.3		µs
t_R	Rise time for both SCL and serial data (SDA)	20 + 0.1 C_B	300	ns
t_F	Fall time for both SCL and SDA	20 + 0.1 C_B	300	ns
t_{SUP}	Pulse width of suppressed spike	0	50	ns

Table 5. I²C Timing in Standard Mode (100 kHz)

Parameter	Description	Min	Max	Unit
t_L	SCL low pulse width	4.7		µs
t_H	SCL high pulse width	4.0		ns
t_{SHD}	Start condition hold time	4.7		µs
t_{DSU}	Data setup time	250		ns
t_{DHD}	Data hold time	0		µs
t_{RSU}	Setup time for repeated start	4.0		µs
t_{PSU}	Stop condition setup time	4.0		µs
t_{BUF}	Bus free time between a stop condition and a start condition	4.7		µs
t_R	Rise time for both SCL and SDA		1	µs
t_F	Fall time for both SCL and SDA		300	ns

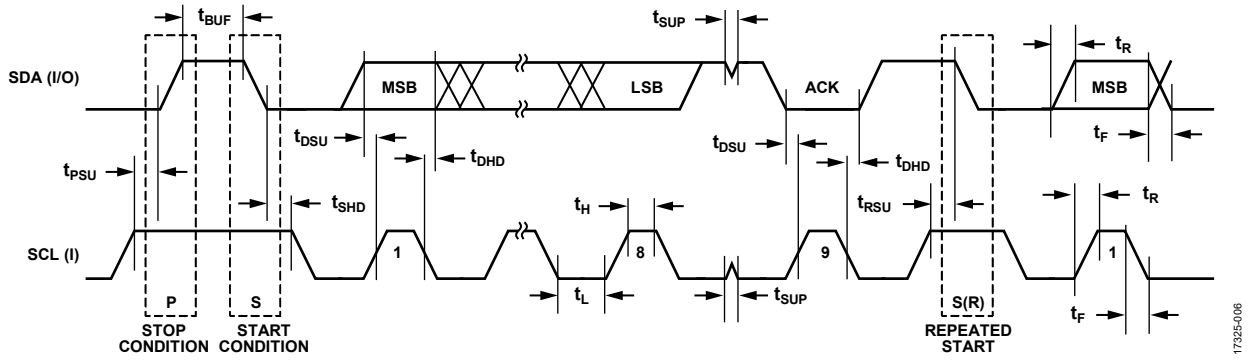

Figure 6. I²C-Compatible Interface Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
AVDD to AGND	−0.3 V to +3.96 V
IOVDD to AGND	−0.3 V to +3.96 V
Digital Input Voltage to DGND	−0.3 V to +3.96 V
Digital Output Voltage to DGND	−0.3 V to +3.96 V
Analog Inputs to AGND	−0.3 V to +3.96 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Electrostatic Discharge (ESD) Rating, All Pins	
Human Body Model (HBM)	±2 kV
Field-Induced Charged Device Model (FICDM)	±850 V
Peak Solder Reflow Temperature	
Tin-Lead (SnPb) Assemblies (10 sec to 30 sec)	240°C
Pb-Free Assemblies (20 sec to 40 sec)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-48-4	27	9.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

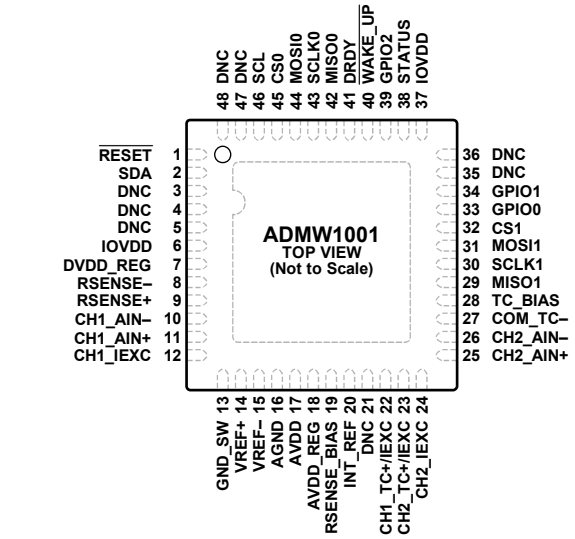

Figure 7. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{RESET}}$	Device Reset Pin. When this pin is taken low, the ADMW1001 is reset to the default state.
2	SDA	Serial Data for I²C Sensor Interface. This serial clock is used in conjunction with the SCL pin to transfer data between the ADMW1001 and an I²C sensor connected to this port. The port accommodates up to two I²C sensors.
3	DNC	Do Not Connect.
4	DNC	Do Not Connect.
5	DNC	Do Not Connect.
6	IOVDD	Digital System Supply Pin. This pin must be connected to AGND via a 0.1 µF capacitor.
7	DVDD_REG	Digital Regulator Supply. This pin must be connected to AGND via a 470 nF capacitor and to Pin 18, AVDD_REG.
8	RSENSE–	Sense Resistor Negative Input. This pin is used for differential readings of an externally supplied reference resistor (RSENSE). This input must be biased to AGND + 100 mV for accurate measurements. Connect to RSENSE_BIAS.
9	RSENSE+	Sense Resistor Positive Input. This pin is used for differential readings of RSENSE. Connect a low temperature coefficient resistor (recommended 1 kΩ, 10 ppm) between RSENSE+ and RSENSE– for RTD measurements.
10	CH1_AIN–	Universal Channel 1 Analog Input 1–.
11	CH1_AIN+	Universal Channel 1 Analog Input 1+.
12	CH1_IEXC	Universal Channel 1 Current Excitation Output. This pin can be configured as the output pin for the excitation current source.
13	GND_SW	Sensor Power Switch to Analog Ground Reference. This pin automatically cycles with measurement sequence.
14	VREF+	External Reference Positive Input. An external reference can be applied between the VREF+ pin and VREF– pin.
15	VREF–	External Reference Negative Input. An external reference can be applied between the VREF+ pin and VREF– pin.
16	AGND	Analog System Ground Reference Pin.
17	AVDD	Analog System Supply Pin. This pin must be connected to AGND via a 0.1 µF capacitor. Connect to a 3.3 V supply.
18	AVDD_REG	Internal Analog Regulator Supply Output. This pin must be connected to AGND via a 470 nF capacitor and to Pin 7, DVDD_REG.
19	RSENSE_BIAS	Bias Voltage Output. Connect to RSENSE–.
20	INT_REF	Internal Reference. This pin must be connected to ground via a 470 nF decoupling capacitor.
21	DNC	Do Not Connect.
22	CH1_TC+/IEXC	Universal Channel 1 Thermocouple Input and Current Excitation Output. This pin can be configured as the output pin for the excitation current source or an input to the ADC.
23	CH2_TC+/IEXC	Universal Channel 2 Thermocouple Input and Current Excitation Output. This pin can be configured as the output pin for the excitation current source or an input to the ADC.

Pin No.	Mnemonic	Description
24	CH2_IEXC	Universal Channel 2 Current Excitation Output. This pin can be configured as the output pin for the excitation current source. This pin can also be configured as an input to the ADC.
25	CH2_AIN+	Universal Channel 2 Analog Input 1+.
26	CH2_AIN−	Universal Channel 2 Analog Input 1−.
27	COM_TC−	Common Thermocouple Input. This pin can be used for thermocouple measurement with CH1_TC+/IEXC and CH2_TC+/IEXC simultaneously.
28	TC_BIAS	Analog Voltage Bias Pin. This pin is used to bias COM_TC− to midscale for TC measurements. Connect to COM_TC− when performing TC measurements.
29	MISO1	SPI Master In/Slave Out. Serial data is transmitted from the SPI sensor to the ADMW1001 on this pin.
30	SCLK1	SPI Serial Clock Output. This pin supplies the serial clock for data transfers between the ADMW1001 and an external SPI sensor that can be connected to the SPI interface. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, the serial clock can be a noncontinuous clock with the information transmitted in smaller batches of data.
31	MOSI1	SPI Master Out/Slave In. Serial data is transmitted from the ADMW1001 to the SPI sensor on this pin.
32	CS1	SPI Chip Select Output. This is an active low logic output that selects the digital SPI sensor. CS1 is used as a frame synchronization signal when communicating with the digital sensor.
33	GPIO0	GPIO Pin. Tie to ground or do not connect if unused.
34	GPIO1	GPIO Pin. Tie to ground or do not connect if unused.
35	DNC	Do Not Connect.
36	DNC	Do Not Connect.
37	IOVDD	Digital System Supply Pin. This pin must be connected to AGND via a 0.1 µF capacitor.
38	STATUS	Status Pin. This pin indicates if an error or alert has occurred. This pin goes high if the error bit in the status register is set or if the alert bit is set. The error bit is set if any of the diagnostics included in the ADMW1001 report an error, and the alert bit is set if the threshold values have been exceeded for any sensor setup.
39	GPIO2	GPIO Pin. Tie to ground or do not connect if unused.
40	$\overline{\text{WAKE\_UP}}$	$\overline{\text{WAKE\_UP}}$ Pin. This pin is required to wake the device up from hibernation mode if enabled. Hibernation mode can be enabled through an SPI command. This pin is active low.
41	DRDY	Data Ready Digital Output. DRDY is a data ready pin, going high to indicate the completion of a sensor measurement. The functionality of this pin is programmable. DRDY can be programmed to go high on the completion of each individual measurement, when a cycle is complete, or when the FIFO is full. If the measurement results are not read before new measurement data is available, the pin goes high before the next update occurs. The DRDY rising edge can also be used as an interrupt to a processor, indicating that valid measurement data is available.
42	MISO0	SPI Master In/Slave Out. Serial data is transmitted from the ADMW1001 to the host processor on this pin.
43	SCLK0	SPI Serial Clock Input. This pin accepts the serial clock for data transfers between the ADMW1001 and the host processor. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, the serial clock can be a noncontinuous clock with the information transmitted in smaller batches of data.
44	MOSI0	SPI Master Out/Slave In. Serial data is transmitted from the host processor to the ADMW1001 on this pin.
45	CS0	SPI Chip Select Input. This is an active low logic input that selects the serial interface of the ADMW1001. CS0 is used as a frame synchronization signal when communicating with the ADMW1001.
46	SCL	Serial Clock for I^2C Sensor Interface. This serial clock is used in conjunction with the SDA pin to transfer data between the ADMW1001 and an I^2C sensor connected to this port. The port accommodates up to two I^2C sensors.
47	DNC	Do Not Connect.
48	DNC	Do Not Connect.
	Exposed Pad	Exposed Pad. The LFCSP has an exposed pad that must be soldered to a metal plate on the PCB and to AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

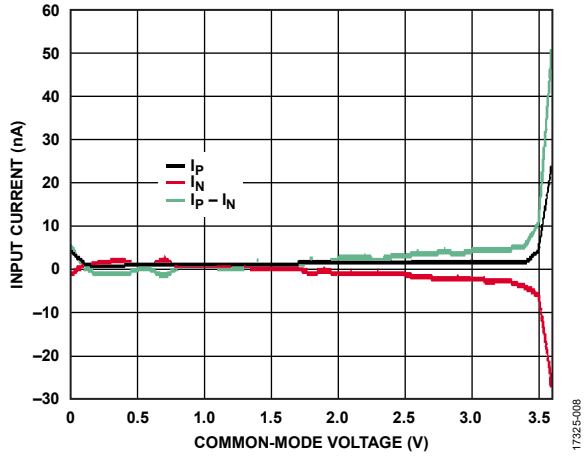

Figure 8. Input Current vs. Common-Mode Voltage (V_{CM}), Gain = 4, ADC Input = 250 mV, AVDD = 3.6 V, T_A = 25°C, V_{CM} = ((AIN+) + (AIN−))/2

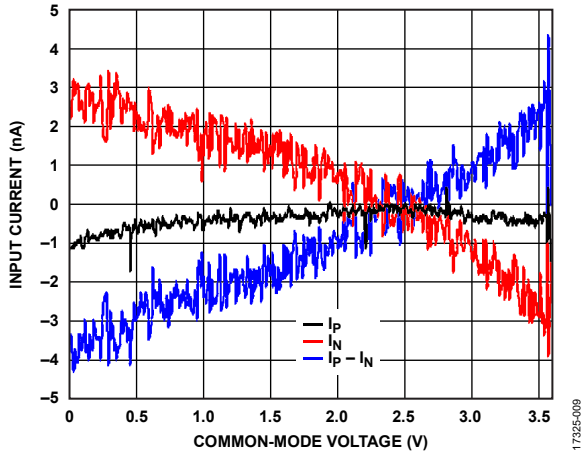

Figure 9. Input Current vs. Common-Mode Voltage (V_{CM}), Gain = 128, ADC Input = 7.8125 mV, AVDD = 3.6 V, T_A = 25°C, V_{CM} = ((AIN+) + (AIN−))/2

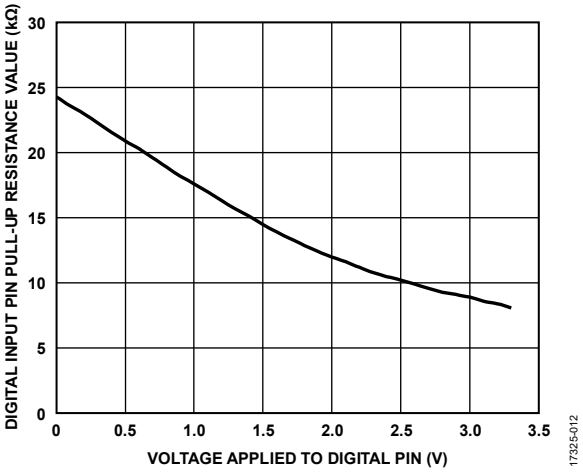

Figure 10. Digital Input Pin Pull-Up Resistance Value vs. Voltage Applied to Digital Pin, T_A = 25°C, IOVDD = 3.4 V

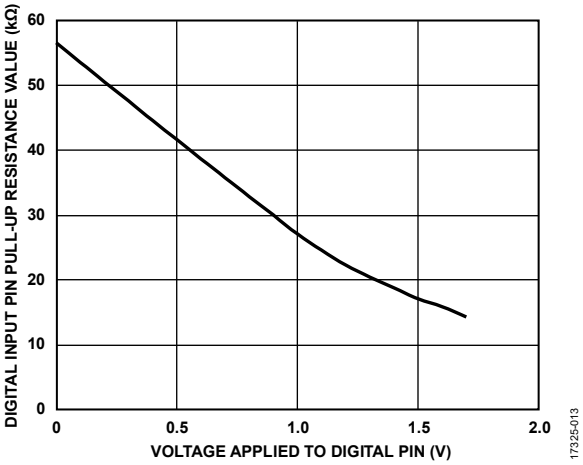

Figure 11. Digital Input Pin Pull-Up Resistance Value vs. Voltage Applied to Digital Pin, T_A = 25°C, IOVDD = 1.8 V

THEORY OF OPERATION

Figure 12 shows the ADMW1001 configured for two RTDs and two thermocouples on the analog channels. A precision 1 kΩ resistor is required as a ratiometric reference for measuring RTDs on the universal channels. The value of this resistor can be programmed into the reference resistor register for greater precision. In this measurement setup, the RTD temperature measurements can be used as cold junction compensation measurements for the thermocouple channels. Optional analog filters can be placed on the analog inputs as antialiasing filters to remove unwanted out of band noise.

Information on firmware flashing and links to the firmware repository can be obtained from the MeasureWare Studio. Each firmware revision is accompanied with a user guide revision detailing sensor compatibility, device configuration, and best practices for the ADMW1001. For information on the features, functionality, and performance of each firmware revision, go to the MeasureWare Studio for the firmware user guide.

For rapid development, visit the MeasureWare Designer to develop a configuration file that can be used with the MeasureWare Lab or exported to a C++ header file that can be used with the ADMW1001 C++ API, which is available in the MeasureWare Studio.

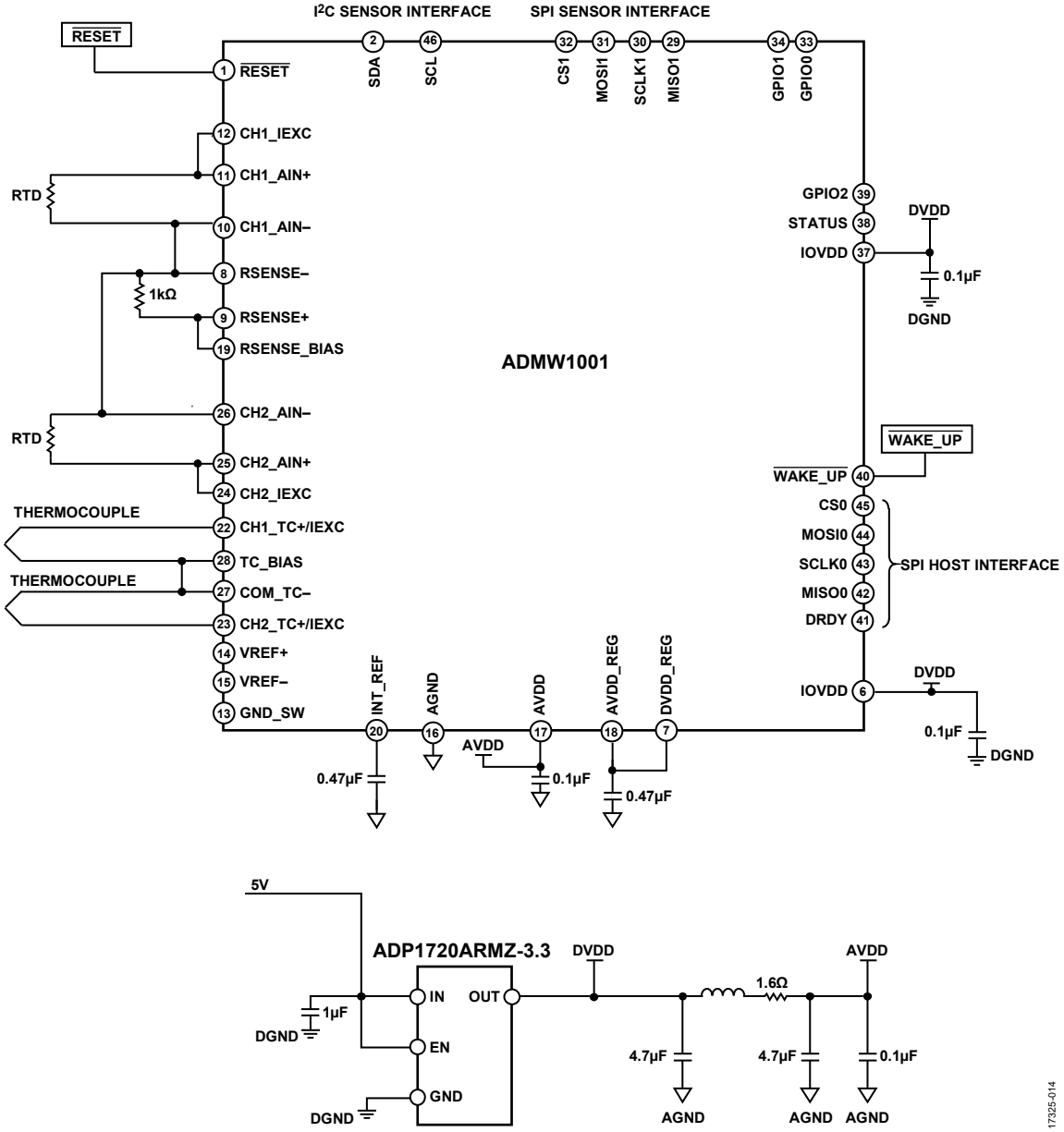

Figure 12. Typical Connection Diagram

APPLICATIONS INFORMATION

The ADMW1001 is ideally suited to precision sensor measurement applications. The benefit of the ADMW1001 is rapid configuration for defined measurement types. The blocks of the ADMW1001 are explained in more detail in this section.

ADC

The ADMW1001 features two 24-bit simultaneous sampling Σ-Δ ADCs. Each ADC is connected to a separate input buffer, PGA, and digital filter. The ADC can use the internal reference or external references from the AVDD supply of the VREF+ and VREF− input pins. ADC conversions can be configured from 5 SPS to 1 kSPS.

POWERING THE ADMW1001

Powering the ADMW1001 requires a 3.3 V dc supply. A precision low dropout regulator (LDO) is recommended with filtering between the analog and digital power inputs to reduce noise coupling into the sensitive analog front end. The AVDD_REG pin and DVDD_REG pin are shorted together and connected to a common decoupling capacitor.

INTERFACE LOGIC

The logic interface that is used for communication and configuration of the ADMW1001 is accomplished using the host SPI interface. A data ready signal is issued by the DRDY pin every time a new conversion is complete and can be used to interrupt a host microcontroller.

The $\overline{\text{WAKE\_UP}}$ signal is active low and requires a pull-up to AVDD or direct connection to a host controller pin. When the device is placed in hibernation mode, only a high to low transition on the $\overline{\text{WAKE\_UP}}$ signal can put the device back into full power mode.

CHANNEL SEQUENCER

The ADMW1001 features a smart channel sequencer. The sequencer creates a measurement cycle from all the enabled channels. The cycle can be programmed to repeatedly sample at programmed intervals in continuous mode, or every time a convert command is issued in single cycle mode.

A 2 kb FIFO allows samples to be buffered on the ADMW1001, which reduces the burden on host processors and allows bulk ready back of samples.

DIGITAL FILTER

The ADMW1001 supports a range of sample rates from as slow as 5 SPS to 1 kSPS. However, there is a noise vs. speed trade-off, and the default values for each sensor are chosen to have the best performance in a wide range of environmental noise conditions. Only a subset of the speed options filter 50 Hz and 60 Hz power line frequency interference.

Lower output data rates offer lower noise measurements and also tune the filter notch. Nine speed modes have been defined for optimized speed and noise.

REFERENCE

The internal reference is a 1.2 V precision reference. The initial tolerance is ±0.1% with a typical drift of 100 ppm/°C. The internal reference is selected by default for all measurement types. The AVDD supply can also be switched internally to the reference supply to enable a large dynamic range when the input buffers are disabled. External referencing can also be selected using the VREF+ and VREF− input pins. This can be used for precision measurement where ratiometric referencing is required.

CALIBRATION AND LUT

The ADMW1001 has a series of calibration features, including per sensor offset and gain configuration options. These values can be stored in the configuration and are loaded on power-up. The ADMW1001 has sensor lookup tables (LUT), which can be used for 4-wire bridge applications and custom sensor configuration.

PGA AND BUFFER

The PGA on the analog front end allows the analog signals to be amplified in gain stages of 1× to 128×. For thermocouple measurement, a gain of 8× is recommended to achieve the best range and accuracy results. For RTD, a gain of 1× is recommended when a value of 1 kΩ is selected for the ratiometric resistors.

The analog input voltage range is constricted when the PGA is enabled. See the Specifications section for more information on analog input ranges.

A separate analog buffer can be enabled or disabled on the front end. For low impendence sensors or buffered sensors, the ADMW1001 analog input buffer can be disabled. When the buffer is disabled, the analog input range is extended to AVDD.

EXCITATION CURRENT SOURCE

The excitation current sources can be used to excite RTDs and other custom sensors. For 2-wire and 3-wire RTD measurement, the CH1_IEXC pin and CH2_IEXC pin are used as the primary excitation source. For 3-wire RTD measurements, the CH1_TC+/IEXC pin and CH2_TC+/IEXC pin are also used as current sources to remove the error introduced from lead resistance. Current source options are 10 μA, 50 μA, 100 μA, 250 μA, 500 μA, and 1000 μA.

CORRECTION AND TRANSLATION

The ADMW1001 allows the selection of specific defined measurement types, such as K–, J–, and T–type thermocouples and PT100 and PT1000 RTDs. The ADMW1001 completes the sampling sequence required for each measurement type and applies the translation from ADC bits to temperature in °C or °F. The thermocouple table and RTD polynomials are stored internally, but custom tables can be loaded through the LUT.

MULTIPLEXER

The multiplexer (MUX) is used to switch in front-end signals to the ADC buffers automatically, depending on the measurement type selected.

OUTLINE DIMENSIONS

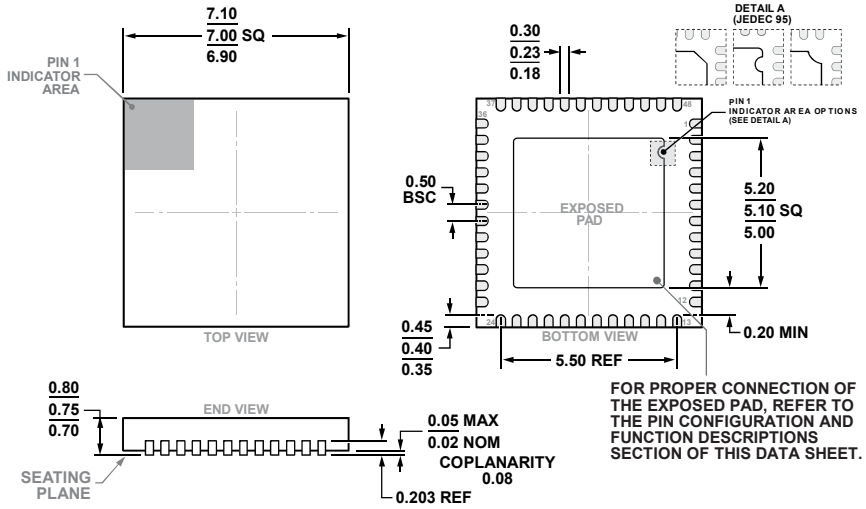

Figure 13. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.75 mm Package Height
(CP-48-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADMW1001BCPZ	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-4	260
ADMW1001BCPZ-RL7	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-4	750
EV-ProMW1001ARDZ		ADMW1001 Prototype Development Kit		1

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).