Product Specification

10Gb/s DWDM 80km Multi-Rate SFP+ Transceiver

FTLX3871MCCxx

PRODUCT FEATURES

- Hot-pluggable SFP+ footprint
- Supports 8.5 and 9.95 to 11.3 Gb/s
- Up to 80km link length
- 100 GHz channel spacing
- -5 /70°C case temperature range
- Single 3.3V power supply
- Cooled 1550nm EML laser
- Limiting electrical interface receiver
- Duplex LC connector
- Built-in digital diagnostic functions
- RoHS-6 compliant (lead-free)

APPLICATIONS

- DWDM 80km links for:
  - Fibre Channel 8.5G and 10G
  - 10G Ethernet
  - 10Gb/s SONET/SDH/OTN
- ITU-T G.698.1 DS100S1-2Dz(C)

Finisar's FTLX3871MCCxx transceivers are Enhanced Small Form Factor Pluggable SFP+ transceivers designed for use in 10-Gigabit multi-rate links up to 80km of G.652 single mode fiber. They are compliant with SFF-8431[1], SFF-8432[2] and G.698.1 DS100S1-2Dz(C), and support SONET OC-192, SDH STM-64, 10G Ethernet ZR and 10G Fibre Channel over 80km fiber. Finisar's FTLX3871MCCxx transceivers use internal retimers (clock and data recovery or CDR) IC's for both the transmitter and the receiver. This guarantees compliance with the SONET/SDH jitter requirements, and they can be used to set the electrical interface XFI-compliant.

Digital diagnostics functions are available via a 2-wire serial interface, as specified in SFF-8472[3]. The optical transceiver is compliant per the RoHS Directive 2011/65/EU[4]. See Finisar Application Note AN-2038 for more details[5].

PRODUCT SELECTION

Product Part Number	Channel Spacing
FTLX3871MCCxx	100 GHz ITU-T grid

Product Channel Selection

Channel (xx)	Product Code	Frequency (THz)	Center Wavelength (nm)
17	FTLX3871MCC17	191.70	1563.86
18	FTLX3871MCC18	191.80	1563.05
19	FTLX3871MCC19	191.90	1562.23
20	FTLX3871MCC20	192.00	1561.42
21	FTLX3871MCC21	192.10	1560.61
22	FTLX3871MCC22	192.20	1559.79
23	FTLX3871MCC23	192.30	1558.98
24	FTLX3871MCC24	192.40	1558.17
25	FTLX3871MCC25	192.50	1557.36
26	FTLX3871MCC26	192.60	1556.55
27	FTLX3871MCC27	192.70	1555.75
28	FTLX3871MCC28	192.80	1554.94
29	FTLX3871MCC29	192.90	1554.13
30	FTLX3871MCC30	193.00	1553.33
31	FTLX3871MCC31	193.10	1552.52
32	FTLX3871MCC32	193.20	1551.72
33	FTLX3871MCC33	193.30	1550.92
34	FTLX3871MCC34	193.40	1550.12
35	FTLX3871MCC35	193.50	1549.32
36	FTLX3871MCC36	193.60	1548.51
37	FTLX3871MCC37	193.70	1547.72
38	FTLX3871MCC38	193.80	1546.92
39	FTLX3871MCC39	193.90	1546.12
40	FTLX3871MCC40	194.00	1545.32
41	FTLX3871MCC41	194.10	1544.53
42	FTLX3871MCC42	194.20	1543.73
43	FTLX3871MCC43	194.30	1542.94
44	FTLX3871MCC44	194.40	1542.14
45	FTLX3871MCC45	194.50	1541.35
46	FTLX3871MCC46	194.60	1540.56
47	FTLX3871MCC47	194.70	1539.77
48	FTLX3871MCC48	194.80	1538.98
49	FTLX3871MCC49	194.90	1538.19
50	FTLX3871MCC50	195.00	1537.40
51	FTLX3871MCC51	195.10	1536.61
52	FTLX3871MCC52	195.20	1535.82
53	FTLX3871MCC53	195.30	1535.04
54	FTLX3871MCC54	195.40	1534.25
55	FTLX3871MCC55	195.50	1533.47
56	FTLX3871MCC56	195.60	1532.68
57	FTLX3871MCC57	195.70	1531.90
58	FTLX3871MCC58	195.80	1531.12
59	FTLX3871MCC59	195.90	1530.33
60	FTLX3871MCC60	196.00	1529.55
61	FTLX3871MCC61	196.10	1528.77

Table 1. Product ordering codes: the central wavelength is defined as per ITU-T 694.1

I. Pin Descriptions

Pin	Symbol	Name/Description	Ref.
1	V_{EET}	Transmitter Ground	1
2	T_{FAULT}	Transmitter Fault	2
3	T_{DIS}	Transmitter Disable. Laser output disabled on high or open.	3
4	SDA	2-wire Serial Interface Data Line	2
5	SCL	2-wire Serial Interface Clock Line	2
6	MOD_ABS	Module Absent. Grounded within the module	2
7	RS0	Rate Select 0.	4
8	RX_LOS	Loss of Signal indication. Logic 0 indicates normal operation.	5
9	RS1	Rate Select 1.	4
10	V_{EER}	Receiver Ground	1
11	V_{EER}	Receiver Ground	1
12	RD-	Receiver Inverted DATA out. AC Coupled.	
13	RD+	Receiver Non-inverted DATA out. AC Coupled.	
14	V_{EER}	Receiver Ground	1
15	V_{CCR}	Receiver Power Supply	6
16	V_{CCT}	Transmitter Power Supply	6
17	V_{EET}	Transmitter Ground	1
18	TD+	Transmitter Non-Inverted DATA in. AC Coupled.	
19	TD-	Transmitter Inverted DATA in. AC Coupled.	
20	V_{EET}	Transmitter Ground	1

Notes:

1. Circuit ground is internally isolated from chassis ground.
2. T_{FAULT} is an open collector/drain output, which should be pulled up with a 4.7k – 10k Ohms resistor on the host board if intended for use. Pull up voltage should be between 2.0V to Vcc + 0.3V. A high output indicates a transmitter fault caused by either the TX bias current or the TX output power exceeding the preset alarm thresholds. A low output indicates normal operation. In the low state, the output is pulled to <0.8V.
3. Laser output disabled on T_{DIS} >2.0V or open, enabled on T_{DIS} <0.8V.
4. Internally pulled down per SFF-8431 Rev 4.1. See Sec. X of this datasheet for the logic table to use for the internal CDRs locking modes.
5. LOS is open collector output. Should be pulled up with 4.7k – 10kΩ on host board to a voltage between 2.0V and 3.6V. Logic 0 indicates normal operation; logic 1 indicates loss of signal.
6. Internally connected

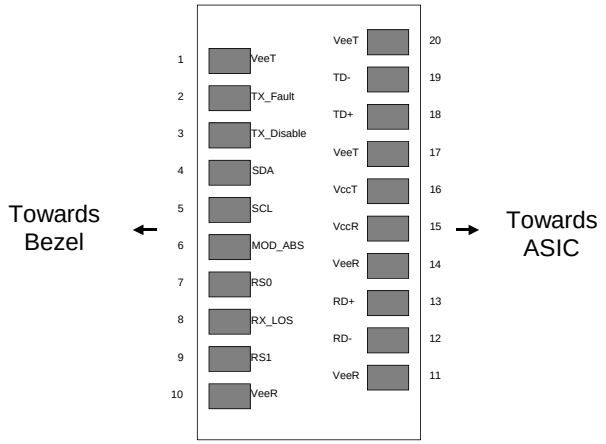


Figure 1. Diagram of Host Board Connector Block Pin Numbers and Names.

II. Absolute Maximum Ratings

Exceeding the limits below may damage the transceiver module permanently.

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage	Vcc	-0.5		4.0	V	
Storage Temperature	T_S	-40		85	°C	
Relative Humidity	RH	0		85	%	1
Receiver Optical Damage Threshold	RxDamage	5			dBm	

Notes:

1. Non-condensing

III. Electrical Characteristics (T_{OP} = -5 to 70 °C)

Parameter	Symbol	Min	Typ.	Max	Unit	Ref.
Supply Voltage	V_{cc}	3.14		3.46		
Transmitter						
Input differential impedance	R_{in}	80	100	120	Ω	
Differential data input swing	Vin,pp	120		850	mV	1
Transmit Disable Voltage	V_D	V_{cc}-0.8		V_{cc}	V	
Transmit Enable Voltage	V_{EN}	V_{ee}		V_{ee}+ 0.8	V	
Receiver						
Output differential impedance	R_{out}	80	100	120	Ω	
Differential data output swing	$V_{out,pp}$	300		850	mV	1
Output rise time and fall time	T_r, T_f	28			ps	2
LOS asserted	$V_{LOS\ A}$	V_{cc}-0.8		V_{cc}	V	3
LOS de-asserted	$V_{LOS\ D}$	V_{ee}		V_{ee}+0.8	V	3
Power Supply Noise Tolerance	V_{ccT}/V_{ccR}	Per SFF-8431 Rev 4.1			mV_{pp}	4
Power Consumption						
Tx and Rx CDR's ON	P_{diss}		1.8	1.9	W	5
Tx CDR OFF and Rx CDR ON			1.7	1.8	W	5
Tx & Rx CDR's OFF and Ethernet spec.			1.6	1.7	W	5

Notes:

1. Internally AC coupled. Data pins connect directly to the CDR.
2. 20 – 80%. Measured with Module Compliance Test Board and OMA test pattern. Use of four 1's and four 0's sequence in the PRBS 9 is an acceptable alternative. SFF-8431 Rev 4.1.
3. LOS is an open collector output. Should be pulled up with 4.7kΩ – 10kΩ on the host board. Normal operation is logic 0; loss of signal is logic 1.
4. See Section 2.8.3 of SFF-8431 Rev 4.1.
5. Typical power consumption values refer to 3.3V, 70°C case temperature and beginning of life.

IV. Optical Characteristics (TOP = -5 to 70 °C, VCC = 3.14 to 3.46 Volts)

Parameter			Symbol	Min	Typ	Max	Unit	Ref.
Transmitter (Tx)								
Average Launch Power			P_{AVE}	-1		+3	dBm	
Optical Wavelength			λ_c	As per ITU-T 694.1			Nm	1
Side-Mode Suppression Ratio			SMSR	30			dB	
Optical Extinction Ratio			ER	8.2			dB	
Average Launch power when Tx is OFF			P_{OFF}			-30	dBm	
Tx Jitter 20kHz - 80MHz			Tx_{j1}			0.3	UI	
Tx Jitter 4MHz - 80MHz			Tx_{j2}			0.1	UI	
Relative Intensity Noise			RIN			-128	dB/Hz	
Center Wavelength			$\lambda_{c\ EOL}$	z-100	z	z+100	Pm	
Receiver (Rx)								
Optical Center Wavelength			λ_C	1260		1600	nm	
Reflectance			R_{rx}			-27	dB	
Rx Power-Limited Performance								
Sensitivity (0km)	Bit Rate (Gb/s)	BER						
	8.5, 9.95-10.7	$<10^{-12}$	R_{SENS1}			-24	dBm	2
	11.1-11.3	$<10^{-4}$	R_{SENS2}			-27	dBm	2
Sensitivity (80km)	8.5, 9.95-10.7	$<10^{-12}$	R_{SENS3}			-21	dBm	2,3.a
	11.1	$<10^{-4}$	R_{SENS4}			-24	dBm	2,3.b
	11.3	$<10^{-4}$	R_{SENS5}			-24	dBm	2,3.c
Power Penalty	8.5, 9.95-10.7	$<10^{-12}$	PP			3	dB	2.3.a
Overload (Average Power)			P_{AVE}	-7			dBm	
LOS De-Assert			LOS_D			-28	dBm	
LOS Assert			LOS_A	-37		-30	dBm	
LOS Hysteresis			LOS_H	0.5			dB	
Rx Noise-Limited Performance (OSNR)								
Bit Rate (Gb/s)	Max CD (ps/nm)	BER		Max OSNR (dB)			RDT	
8.5, 9.95-10.7	0	1E-12	$OSNR_1$	23			Default	4,5
	1450		$OSNR_2$	28			Default	4,5
11.1	0	1E-12	$OSNR_3$	23			Default	4,5
	1300		$OSNR_4$	28			Default	4,5
10.7-11.1	0	1E-7	$OSNR_5$	18			Default	4,5
	1300		$OSNR_6$	23			Default	4,5

Notes:
1. Refer to Tab. 1.
2. Measured with worst ER=8.2dB; $2^{31} - 1$ PRBS.
3. Max chromatic dispersion (CD) tolerance over 80km of G.652 single mode fiber:
   3.a → 1450ps/nm; 3.b →1300ps/nm; 3.c → 1100ps/nm
4. With optical input power at the receiver between -7 and -18 dBm
5. Please see Sec. XII for additional details on the Receiver Decision Threshold (RDT).

V. General Specifications

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Bit Rate	BR	8.5		11.3168	Gb/s	1
Max. Supported Link Length	L_{MAX}			80	km	2

Notes:
1. Tested with a 2^{31} – 1 PRBS pattern at the BER defined in Table IV.
2. Over G.652 single mode fiber.

Timing Parameters

Parameter	Symbol	Min	Max	Units	Ref.
Time to initialize cooled module	t_start_up_cooled		90	s	

VI. Environmental Specifications

Finisar FTLX3871MCCxx transceivers have an operating temperature range from -5°C to +70°C case temperature.

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Case Operating Temperature	T_{op}	-5		70	°C	
Storage Temperature	T_{sto}	-40		85	°C	

VII. Regulatory Compliance

Finisar transceivers are Class 1 Laser Products and comply with US FDA regulations. These products are certified by TÜV and CSA to meet the Class 1 eye safety requirements of EN (IEC) 60825 and the electrical safety requirements of EN (IEC) 60950. Copies of certificates are available at Finisar Corporation upon request.

VIII. Digital Diagnostic Functions

Finisar FTLX3871MCCxx SFP+ transceivers support the 2-wire serial communication protocol as defined in the SFP MSA[1]. It is very closely related to the memory map defined in the GBIC standard, with the same electrical specifications.

The standard SFP serial ID provides access to identification information that describes the transceiver's capabilities, standard interfaces, manufacturer, and other information.

Additionally, Finisar SFP+ transceivers provide a enhanced digital diagnostic monitoring interface, which allows real-time access to device operating parameters such as transceiver temperature, laser bias current, transmitted optical power, received optical power and transceiver supply voltage. It also defines a sophisticated system of alarm and warning flags, which alerts end-users when particular operating parameters are outside of a factory set normal range.

The SFP MSA defines a 256-byte memory map that is accessible over a 2-wire serial interface at the 8 bit address 1010000X (A0h). The digital diagnostic monitoring interface makes use of the 8 bit address 1010001X (A2h), so the originally defined serial ID memory map remains unchanged. The interface is identical to, and is thus fully backward compatible with both the GBIC Specification and the SFP Multi Source Agreement. The complete interface is described in Finisar Application Note AN-2030: "Digital Diagnostics Monitoring Interface for SFP Optical Transceivers" [7].

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through a 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL, Mod Def 1) is generated by the host. The positive edge clocks data into the SFP transceiver into those segments of the E^2PROM that are not write-protected. The negative edge clocks data from the SFP transceiver. The serial data signal (SDA, Mod Def 2) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially.

For more information, please see the SFP MSA documentation[6] and Finisar Application Note AN-2030.

Please note that evaluation board FDB-1027 is available with Finisar ModDEMO software that allows simple to use communication over the 2-wire serial interface.

IX. Digital Diagnostic Specifications

FTLX3871MCCxx transceivers can be used in host systems that require either internally or externally calibrated digital diagnostics.

Parameter	Symbol	Units	Min	Max	Accuracy	Ref.
Accuracy						
Transceiver temperature	Δ_{DDTemp}	ºC	-10	+75	±5ºC	1
Transceiver supply voltage	$\Delta_{DDVoltage}$	V	2.8	4.0	±3%	
Transmitter bias current	Δ_{DDBias}	mA	0	127	±10%	2
Transmitter output power	$\Delta_{DDTx\text{-}Power}$	dBm	-1	+5	±2dB	
Receiver average optical input power	$\Delta_{DDRx\text{-}Power}$	dBm	-28	-5	±2dB	

Notes:
1. Internally measured
2. The accuracy of the Tx bias current is 10% of the actual current from the laser driver to the laser

X. Internal CDRs Locking Modes

The FTLX3871MCCxx is equipped with internal CDR units on both the receiver and the transmitter sides. The host can set the CDR's to lock at 8.5Gb/s, 10G (9.95-11.3Gb/s), or in by-pass mode, by setting the rate select pins or the soft bits (logic OR). The different locking modes are shown in the following logic table:

R/S 0	R/S 1	CDR's Locking Mode
Logic OR of: pin 7 & bit 110.3	**Logic OR of: pin 9 & bit 118.3**	
Low or 0	Low or 0	Both CDR's lock at 8.5Gb/s
Low or 0	High or 1	Tx CDR is in bypass mode. Rx CDR locks at 10G (9.95-11.3Gb/s)
High or 1	Low or 0	Tx & Rx CDR's in bypass mode
High or 1	High or 1	Both CDR's lock at 10G (9.95-11.3Gb/s) The bits 110.3 and 118.3 are set to 1 by default at power-up

The RS0 and RS1 pins are internally pulled-down to ground as per [1]. The soft bits 110.3 and 118.3 are both set to "1" at the transceiver power-up, to select the 10G locking mode by default. The host can change this configuration via the 2-wire communication as described in the SFP MSA [1]. Alternative configurations can be factory set upon request. Please refer to Finisar for additional details.

XI. SFF-8431 Power-up Sequence

If either CDR is enabled, the typical power consumption of the FTLX3871MCCxx may exceed the limit of 1.5W specified for the Power Level II transceivers in [1], for which a power-up sequence is recommended. However, the FTLX3871MCCxx is factory set to power-up directly to its operating conditions. Upon request, it can be factory set to follow the power-up sequence specified for transceivers exceeding 1W, as per [1]. In power level I, the FTLX3871MCCxx does not carry traffic, but the 2-wire serial communication is active.
Please refer to [1] and Finisar Application Note AN-2076 for additional details.

XII. Receiver Decision Threshold Control

The host can control the Receiver Decision Threshold (RxDT) of Finisar FTLX3871MCCxx SFP+ transceivers via the 2-wire serial communication, by setting the byte 131 of Table 02h. The availability of this function is indicated in Bit 3, Byte 64 of A0h in the serial ID section. Byte 131 is a 2's complement 7 bit value (-128 - +127) The decision threshold set is given by:

RxDT = default RxDT + [Byte(131)/256]*100%.

On power-up the byte 131 defaults to 0, corresponding to the RxDT optimum value. The actual RxDT range the formula covers is about ±20% around the default optimum value.

XIII. Mechanical Specifications

Finisar FTLX3871MCCxx SFP+ transceivers are compatible with the SFF-8432 specification for improved pluggable form factor, and shown here for reference purposes only. Bail color is white.

ITEM	DIM (mm)	TOL (mm)
A	9.00	± 0.3
B	9.60	± 0.5
C	11.90	± 0.5
D	13.85	± 0.15
E	13.65	± 0.15
F	2.80	± 0.2
G	1.00	± 0.2
H	4.00	REF
J	2.00	± 0.2
K	56.50	REF
L	1.60	± 0.5
M	2.25	± 0.1
N	1.80	± 0.1
P	37.10	± 0.3
Q	9.15	± 0.15
R	1.00	± 0.1
S	8.55	± 0.15
T	47.50	± 0.2
V	2.55	± 0.1
W	43.00	± 0.2
X	14.70	± 0.5
Z	0.55	± 0.15

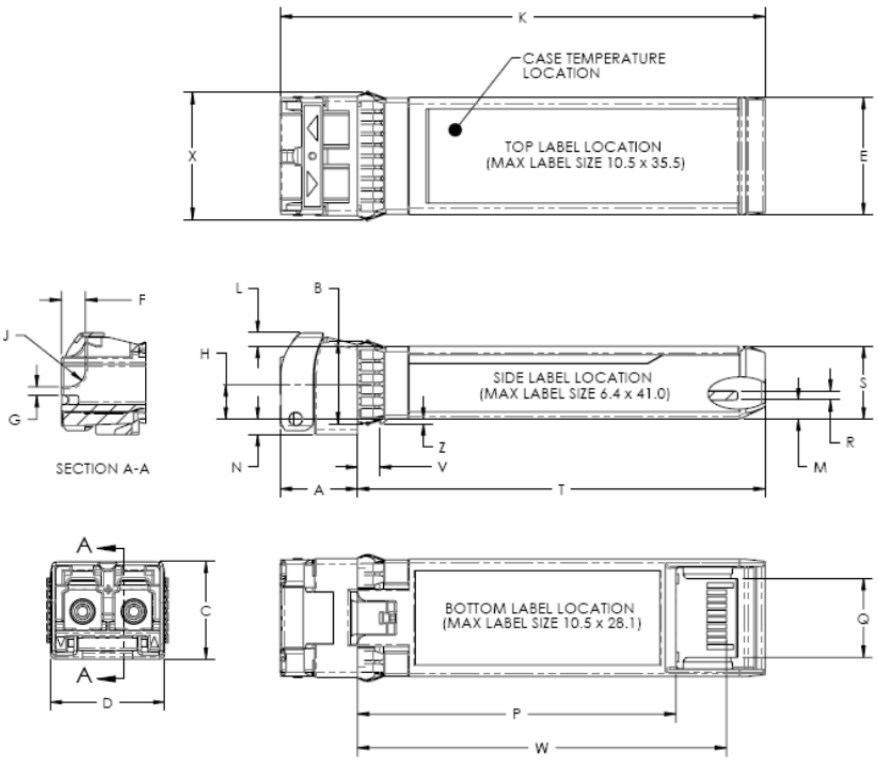


Figure 2. Mechanical Dimensions

Note: the option of the label on the top side of the transceiver is not recommended.

XIV. Host Board SFP+ Connector Recommendations

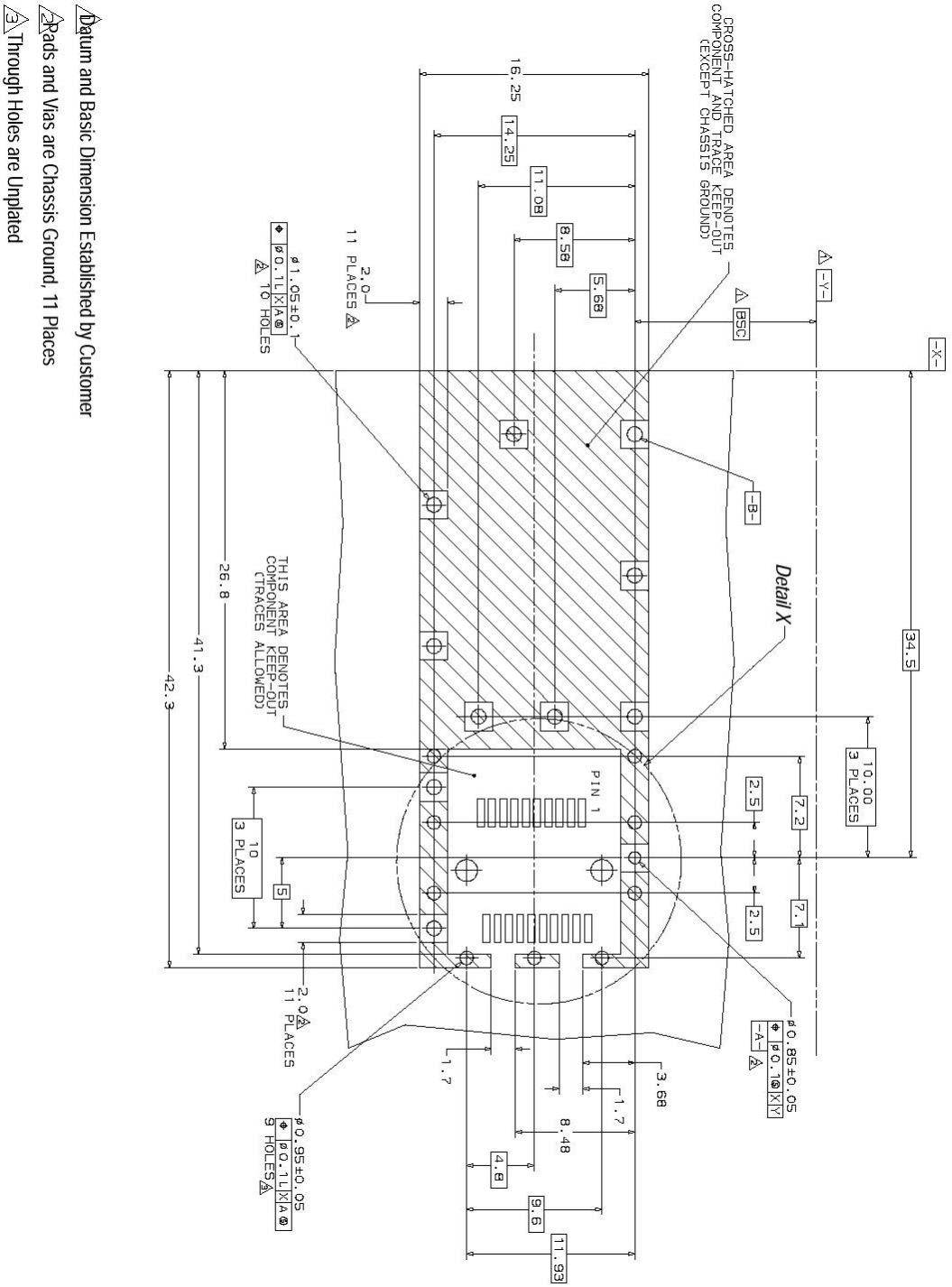
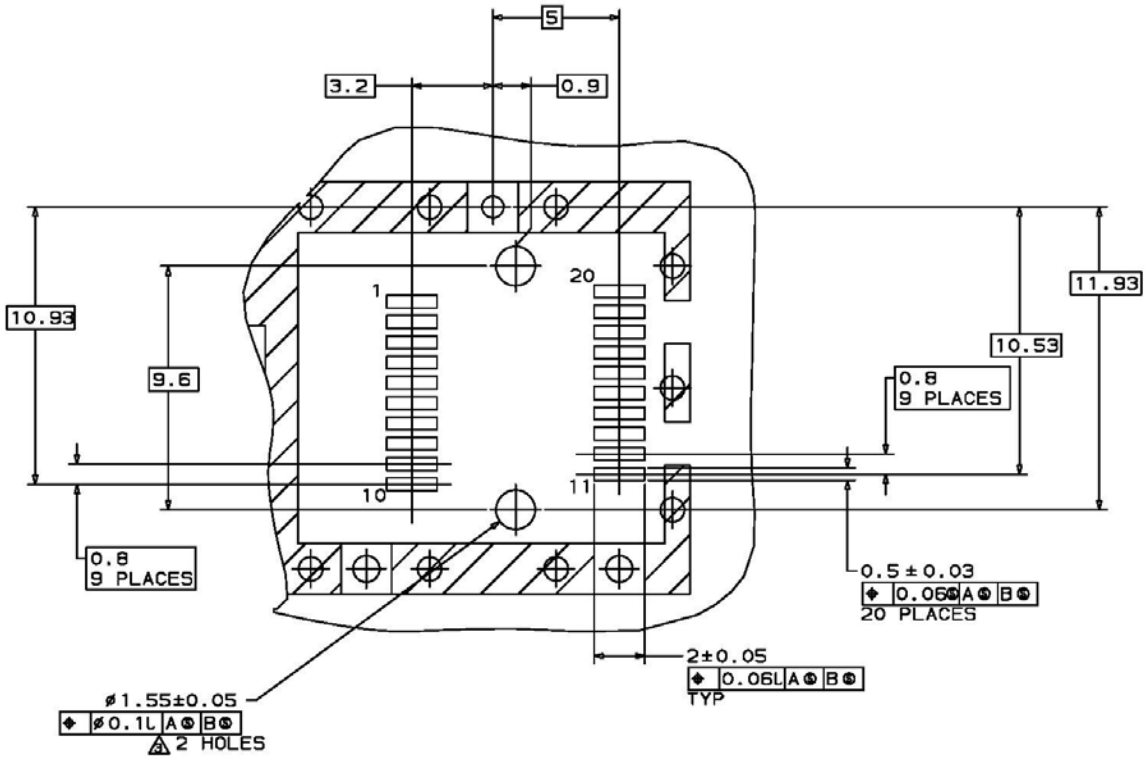
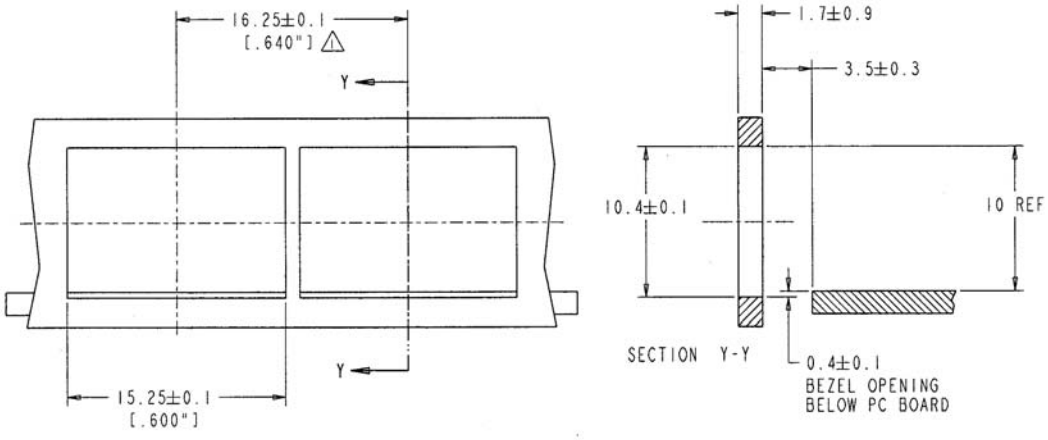


Figure 3. PCB Layout and Bezel Recommendations, as per [9]





NOTES:

1. MINIMUM PITCH ILLUSTRATED, ENGLISH DIMENSIONS ARE FOR REFERENCE ONLY
2. NOT RECOMMENDED FOR PCI EXPANSION CARD APPLICATIONS

Figure 4

XV. Host-Module Interface Diagram

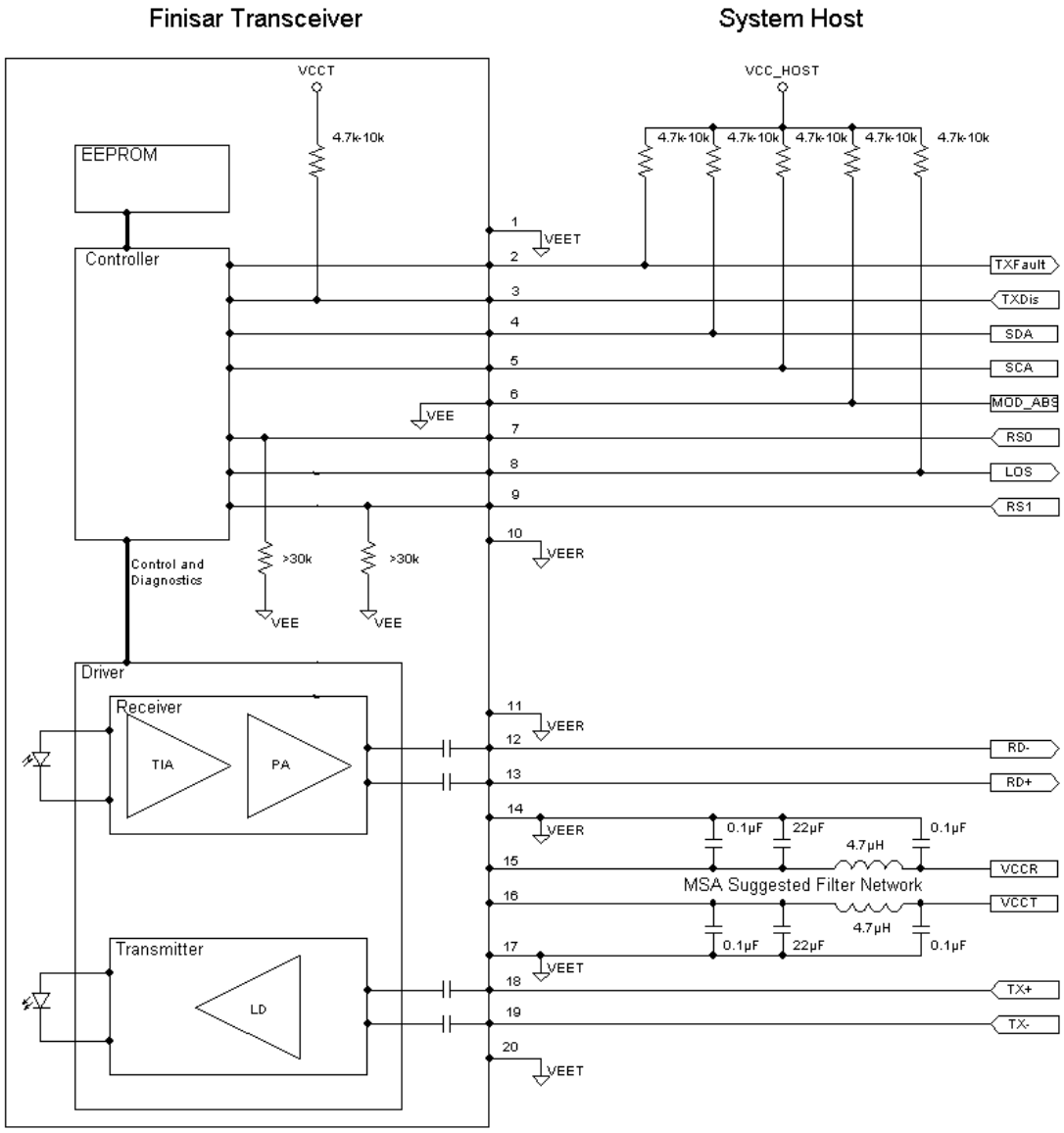


Figure 5

XVI. References

1. "Specifications for Enhanced 8.5 and 10 Gigabit Small Form Factor Pluggable Module 'SFP+ '", SFF Document Number SFF-8431, Revision 4.1, including SFF-8431 Rev 4.1 Addendum. September 15, 2013
2. "Improved Pluggable Form factor", SFF Document Number SFF-8432, Revision 4.2, April 18, 2007.
3. "Digital Diagnostics Monitoring Interface for Optical Transceivers". SFF Document Number SFF-8472, Revision 11.3, June 11, 2013.
4. Directive 2011/65/EU of the European Council Parliament and of the Council, "on the restriction of the use of certain hazardous substances in electrical and electronic equipment"
5. "Application Note AN-2038: Finisar Implementation of RoHS Compliant Transceivers"
6. Small Form-factor Pluggable (SFP) Transceiver Multi-Source Agreement (MSA)
7. "Application Note AN-2030: Digital Diagnostic Monitoring Interface for SFP Optical Transceivers"
8. "Application Note AN-2076: SFP+ Level II Power Up Sequence", Rev B

XVII. For More Information

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