

# Buck Converter - High Current, Synchronous

## NCP3235

The NCP3235 is a high current, high efficiency voltage mode synchronous buck converter which operates from 4.5 V to 23 V input and generates output voltages down to 0.6 V at up to 15 A continuous current. It has two operation modes: FCCM and automatic CCM/DCM. In automatic CCM/DCM mode, the controller can switch smoothly between CCM and DCM, where converter runs at reduced switching frequency to achieve much higher efficiency at light load. The NCP3235 is available in 6 mm x 6 mm QFN-40 pin package.

### Features

- Wide Input Voltage Range from 4.5 V to 23 V
- 0.6 V Internal Reference Voltage
- Switching Frequency Option: 550 kHz, 1.1 MHz
- External Programmable Soft-Start
- Lossless Low-side FET Current Sensing
- Output Over-voltage Protection and Under-voltage Protection
- Selective Hiccup/Latch Off Operation for All Faults
- Pre-bias Start-up
- Adjustable Output Voltage
- Power Good Output
- Internal Over-temperature Protection
- Adjustable Input UVLO
- This is a Pb-Free Device

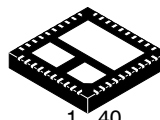
### Typical Application

- Industry PC Equipment
- ASIC, FPGA, DSP and CPU Core and I/O Supplies
- Server and Storage System
- Telecom and Network Equipment



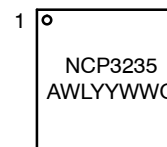
ON Semiconductor®

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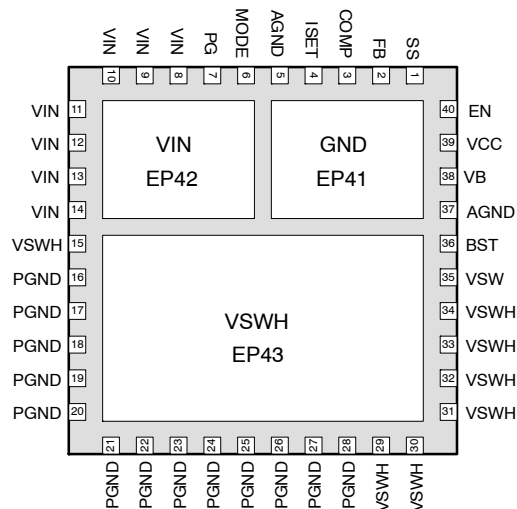
QFN40 6x6, 0.5P  
CASE 485CM

### MARKING DIAGRAM



- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

### PIN CONNECTIONS



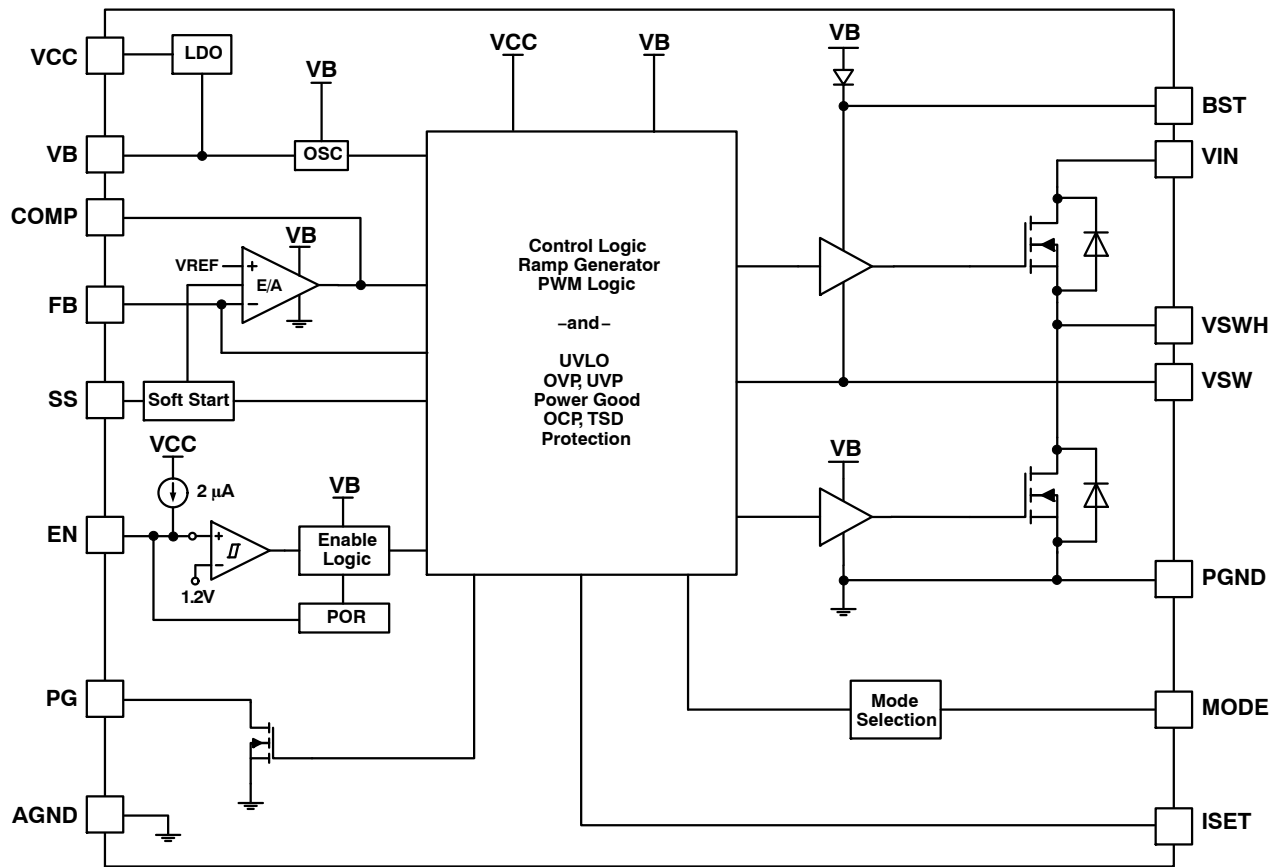
(Top View)

### ORDERING INFORMATION

| Device       | Package             | Shipping <sup>†</sup> |
|--------------|---------------------|-----------------------|
| NCP3235MNTXG | QFN-40<br>(Pb-Free) | 2500 /<br>Tape & Reel |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NCP3235

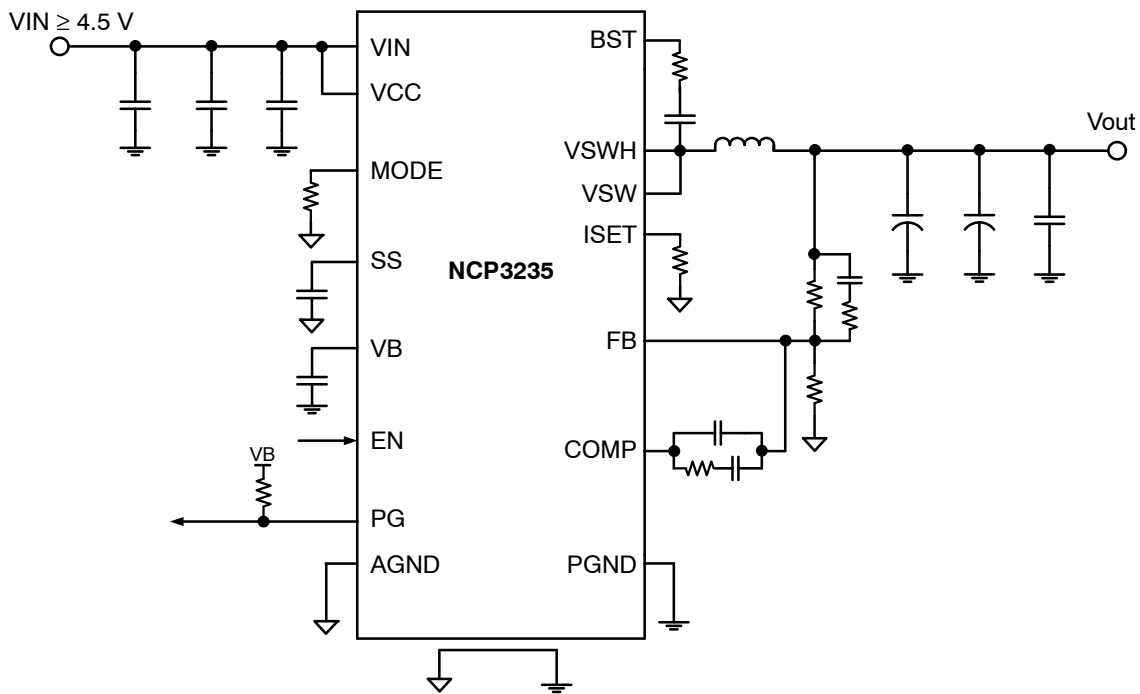


**Figure 1. NCP3235 Block Diagram**

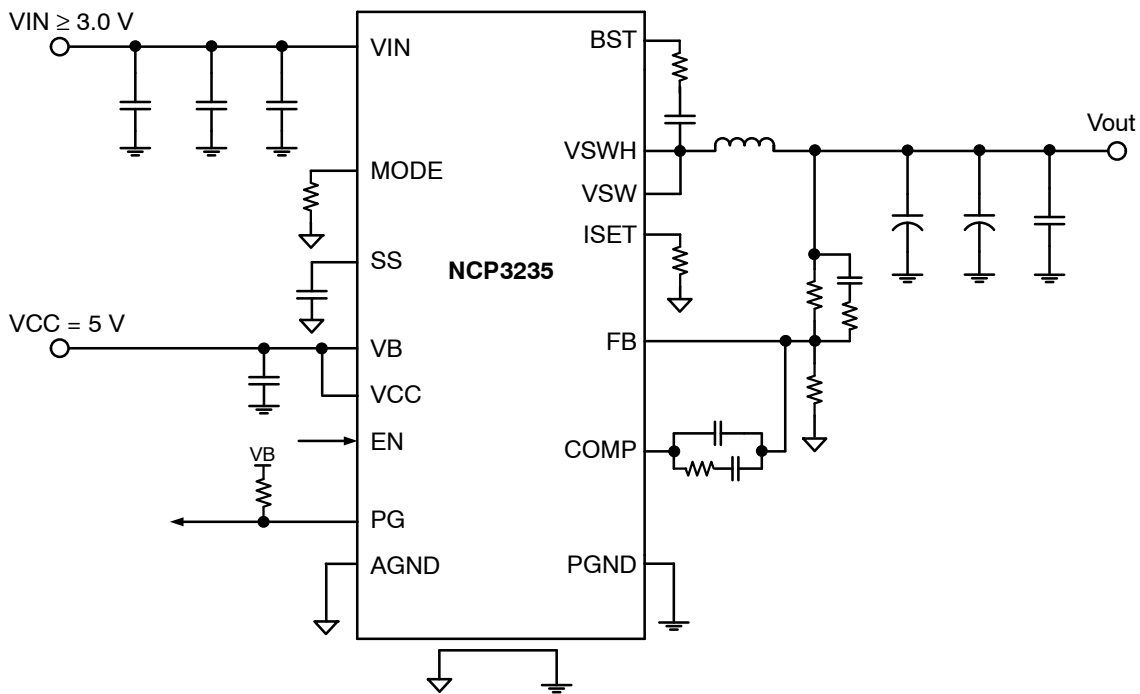
**Table 1. PIN DESCRIPTION**

| Pin No.         | Symbol | Description  |
|-----------------|--------|--|
| 1               | SS     | A capacitor from this pin to GND allows the user to adjust the soft-start ramp time.   |
| 2               | FB     | Output voltage feedback.   |
| 3               | COMP   | Output of the error amplifier.   |
| 4               | ISET   | A resistor from this pin to ground sets the over-current protection (OCP) threshold.   |
| 5, 37           | AGND   | Analog ground.   |
| 6               | MODE   | Mode selection for FCCM mode and automatic CCM/DCM mode, switching frequency and hiccup/latch protection mode. See table I in the latter page.   |
| 7               | PG     | Power good indicator of the output voltage. Open-drain output. Connect PG to VDD with an external resistor.  |
| 8-14, EP42      | VIN    | The VIN pin is connected to the internal power NMOS switch. The VIN pin has high di/dt edges and must be decoupled to ground close to the pin of the device.   |
| 15, 29-34, EP43 | VSWH   | The VSWH pin is the connection of the drain and source of the internal NMOS switches. At switch off, the inductor will drive this pin below ground as the body diode and the NMOS conducts with a high dv/dt.  |
| 16-28           | PGND   | Ground reference and high-current return path for the bottom gate driver and low-side NMOS.  |
| 35              | VSW    | IC connection to the switch node between the top MOSFET and bottom MOSFET. Return path of the high-side gate driver.   |
| 36              | BST    | Top gate driver input supply, a bootstrap capacitor connection between the switch node and this pin.   |
| 38              | VB     | The internal LDO output and supply for the NCP3235. Connect a minimum of 4.7uF ceramic capacitor from this pin to ground.  |
| 39              | VCC    | Input Supply for IC. This pin must be connected to VIN.  |
| 40              | EN     | Logic control for enabling the switcher. An internal pull-up enables the device automatically. The EN pin can also be driven high to turn on the device, or low to turn off the device. A comparator and precision reference allow the user to implement this pin as an adjustable UVLO circuit. |
| EP41            | GND    | Exposed Pad. Connect GND to a large copper plane at ground potential to improve thermal dissipation.   |

## NCP3235



**Figure 2. NCP3235 Typical Application Circuit Without External VCC**



**Figure 3. NCP3235 Typical Application Circuit With VCC = 5 V**

# NCP3235

**Table 2. ABSOLUTE MAXIMUM RATINGS** (measured vs. GND pad, unless otherwise noted)

| Rating                                      | Symbol              | Value   | Unit |
|---|---------------------|---|------|
| Power Supply to GND                         | VIN, VCC            | 23<br>-0.3  | V    |
| VSW to GND                                  | VSWH, VSW           | 30<br>-0.6 (DC)<br>35 (t < 50 ns)<br>-5 (t < 50 ns) | V    |
| BST to GND                                  | BST                 | 35 (DC)<br>-0.6 (DC)<br>40 (t < 50 ns)              | V    |
| BST to VSW                                  | VBST_VSW            | 6.5 (DC)<br>-0.3 (DC)                               | V    |
| VIN to VSW, VIN = VCC                       |                     | -0.3 to 28 (DC)<br>-4 (t < 50 ns)                   | V    |
| All other input pins                        |                     | 6.0<br>-0.3   | V    |
| Electrostatic Discharge Human body model    | HBM                 | 1.0   | kV   |
| Electrostatic Discharge Charge device model | CDM                 | 2.0   | kV   |
| Operating Ambient Temperature Range         | T <sub>A</sub>      | -40 to +125   | °C   |
| Operating Junction Temperature Range        | T <sub>J</sub>      | -40 to +125   | °C   |
| Maximum Junction Temperature                | T <sub>J(MAX)</sub> | +150  | °C   |
| Storage Temperature Range                   | T <sub>stg</sub>    | -55 to +150   | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 3. THERMAL INFORMATION**

|  |                     |     |      |
|--|---------------------|-----|------|
| HS FET Junction-to-case-bottom thermal resistance (Note 1) | R <sub>θJC-HS</sub> | 1.3 | °C/W |
| LS FET Junction-to-case-bottom thermal resistance (Note 1) | R <sub>θJC-LS</sub> | 0.6 | °C/W |
| Junction-to-ambient thermal resistance                     | R <sub>θA</sub>     | 35  | °C/W |

1. R<sub>θJC</sub> thermal resistance is obtained by simulating a cold plate test on the exposed power pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

# NCP3235

**Table 4. ELECTRICAL CHARACTERISTICS**

( $-40^{\circ}\text{C} < T_J < +125^{\circ}\text{C}$ ,  $V_{CC} = 12\text{ V}$ , for min/max values unless otherwise noted,  $T_J = +25^{\circ}\text{C}$  for typical values)

| Parameter  | Symbol            | Test Conditions  | Min          | Typ          | Max          | Units                 |
|--|-------------------|--|--------------|--------------|--------------|-----------------------|
| <b>POWER SUPPLY</b>                                  |                   |  |              |              |              |                       |
| VIN/VCC Operation Voltage                            | VIN/VCC           |  | 4.5          |              | 21           | V                     |
| VB UVLO Threshold (Rising)                           |                   |  | 4.2          | 4.3          | 4.4          | V                     |
| VB UVLO Threshold (Falling)                          |                   |  | 3.8          | 3.95         | 4.0          | V                     |
| VB Output Voltage                                    | VB                | $V_{CC} = 6\text{ V}$ , $0 \leq I_B \leq 40\text{ mA}$   | 4.86         | 5.15         | 5.45         | V                     |
| VB Dropout voltage                                   |                   | $I_B = 25\text{ mA}$ , $V_{CC} = 4.5\text{ V}$   |              | 65           | 120          | mV                    |
| VCC Quiescent Current                                |                   | EN=H, COMP=H, no switching;<br>PG open; no switching   |              | 4.7          | 6.4          | mA                    |
| Shutdown Supply Current                              |                   | EN=0; $V_{cc}=21\text{ V}$ ; PG open   |              | 100          | 140          | $\mu\text{A}$         |
|  |                   | EN=0; $V_{cc}=4.5$ ; PG open   |              | 75           | 85           | $\mu\text{A}$         |
| <b>FEEDBACK VOLTAGE</b>                              |                   |  |              |              |              |                       |
| FB input voltage                                     | VFB               | $T_J = 25^{\circ}\text{C}$ , $4.5\text{ V} \leq V_{CC} \leq 21\text{ V}$                                 | 597          | 600          | 603          | mV                    |
|  |                   | $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ ;<br>$4.5\text{ V} \leq V_{CC} \leq 21\text{ V}$ | 594          | 600          | 606          |                       |
| Feedback Input Bias Current                          | IFB               | VFB = 0.6 V  |              |              | 75           | nA                    |
| <b>ERROR AMPLIFIER</b>                               |                   |  |              |              |              |                       |
| Open Loop DC Gain (GBD)                              |                   |  | 60           | 85           |              | dB                    |
| Open Loop Unity Gain Bandwidth                       | F0dB,EA           |  |              | 24           |              | MHz                   |
| Open Loop Phase Margin                               |                   |  |              | 60           |              | deg                   |
| Slew Rate  |                   | COMP pin to GND = 10 pF  |              | 2.5          |              | V/ $\mu\text{s}$      |
| COMP Clamp Voltage, High                             |                   |  |              | 3.3          |              | V                     |
| COMP Clamp Voltage, Low                              |                   |  |              | 0.57         |              | V                     |
| Output Source Current                                |                   | VFB = 0.55 V   | 15           |              |              | mA                    |
| Output Sink Current                                  |                   | VFB = 1 V  | 20           |              |              | mA                    |
| <b>CURRENT LIMIT</b>                                 |                   |  |              |              |              |                       |
| Low-side $R_{DS(on)}/ISET$                           | $R_{DS(on)}/ISET$ | Guaranteed by characterization, $T_J = 25^{\circ}\text{C}$   |              | 108          |              | $\Omega/\text{A}$     |
| Low-side ISET Current Source Temperature Coefficient | TC_LS_ISET        |  |              | +0.33        |              | %/ $^{\circ}\text{C}$ |
| Low-side OCP switch-over threshold                   |                   | Guaranteed by design   |              | 600          |              | mV                    |
| Low-side Fixed OCP threshold                         | LS_OCPth          | Guaranteed by design   |              | 600          |              | mV                    |
| Low-side programmable OCP range                      |                   | Guaranteed by design   |              |              | <600         | mV                    |
| LS OCP Blanking time                                 | LS_Tblink         | Guaranteed by design   |              | 150          |              | ns                    |
| <b>PWM</b>   |                   |  |              |              |              |                       |
| Maximum duty cycle                                   |                   | fsw = 550 kHz,<br>$4.5\text{ V} < V_{CC} < 21\text{ V}$  |              | 87           |              | %                     |
|  |                   | fsw = 1.1 MHz,<br>$4.5\text{ V} < V_{CC} < 21\text{ V}$  |              | 76           |              |                       |
| Minimum duty cycle                                   |                   | VCOMP < PWM Ramp Offset Voltage  |              | 0            |              | %                     |
| Minimum GH on-time                                   |                   | Guaranteed by design   |              | 35           |              | ns                    |
| PWM Ramp Amplitude                                   |                   | Guaranteed by characterization   | $V_{CC}/7.9$ | $V_{CC}/6.5$ | $V_{CC}/5.6$ | V                     |
| PWM Ramp Offset                                      |                   |  |              | 0.67         |              | V                     |

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**Table 4. ELECTRICAL CHARACTERISTICS**

( $-40^{\circ}\text{C} < T_J < +125^{\circ}\text{C}$ ,  $V_{CC} = 12\text{ V}$ , for min/max values unless otherwise noted,  $T_J = +25^{\circ}\text{C}$  for typical values)

| Parameter                                | Symbol            | Test Conditions                                     | Min  | Typ     | Max  | Units |
|--|-------------------|---|------|---------|------|-------|
| <b>OSCILLATOR</b>                        |                   |   |      |         |      |       |
| Oscillator Frequency Range               | fsw               | fsw = 550 kHz<br>4.5 V < VCC < 21 V                 | 500  | 550     | 600  | kHz   |
|  |                   | fsw = 1100 kHz<br>4.5 V < VCC < 21 V                | 990  | 1100    | 1210 |       |
| Hiccup Timer                             | Thiccup           | tss < 1 ms  |      | 4       |      | ms    |
|  |                   | Tss > 1 ms  |      | 4 x tss |      |       |
| <b>ZERO CROSSING</b>                     |                   |   |      |         |      |       |
| Zero Crossing Comparator Internal Offset |                   | PGND-VSW, Automatic CCM/DCM<br>Guaranteed by design | -4.5 | -3.0    | -1.5 | mV    |
| <b>MODE</b>                              |                   |   |      |         |      |       |
| Mode pin threshold voltage               | ModeTHS           | GND   |      |         | 0.25 | V     |
|  |                   | 49.9 kΩ   | 0.43 |         | 0.65 |       |
|  |                   | 100 kΩ  | 0.86 |         | 1.15 |       |
|  |                   | 174 kΩ  | 1.48 |         | 2.0  |       |
|  |                   | Floating  | 2.4  |         |      |       |
| Mode pin source current                  | I <sub>Mode</sub> |   | 8.8  | 10      | 11.2 | μA    |
| <b>ENABLE INPUT (EN)</b>                 |                   |   |      |         |      |       |
| EN Input Operating Range                 |                   |   |      |         | 5.5  | V     |
| Enable Threshold Voltage                 | V <sub>EN</sub>   | Min VEN rising                                      | 1.11 | 1.2     | 1.29 | V     |
| Enable Threshold Voltage                 |                   | Max VEN falling                                     |      | 1.05    |      | V     |
| Deep Disable Threshold                   |                   |   | 0.7  | 0.8     | 0.9  | V     |
| Enable Pull-up Current                   |                   |   |      | 2       |      | μA    |
| <b>SOFTSTART INPUT (SS)</b>              |                   |   |      |         |      |       |
| SS Startup Delay                         | tSSD              |   |      | 1.45    |      | ms    |
| SS End Threshold                         | SSEND             |   |      | 0.6     |      | V     |
| SS Source Current                        | ISS               |   | 2.15 | 2.5     | 2.8  | μA    |
| <b>VOLTAGE MONITOR</b>                   |                   |   |      |         |      |       |
| Power Good Sink Current                  |                   | PG = 0.15 V   | 10   | 20      | 30   | mA    |
| Output Overvoltage Rising Threshold      |                   |   | 687  | 700     | 713  | mV    |
| Overvoltage Fault Blanking Time          |                   |   |      | 4.0     |      | μs    |
| Output Under-Voltage Trip Threshold      |                   |   | 475  | 500     | 525  | mV    |
| Under-voltage Protection Blanking Time   |                   |   |      | 20      |      | μs    |
| <b>POWER STAGE</b>                       |                   |   |      |         |      |       |
| High-side On Resistance                  | RDSONH            | VIN/VCC = 5 V, ID = 2 A                             |      | 6.5     | 10   | mΩ    |
| Low-side On Resistance                   | RDSONL            | VIN/VCC = 5 V, ID = 2 A                             |      | 2.9     | 5.2  | mΩ    |
| VFBOOT                                   |                   | IBOOT = 2 mA  |      | 28      |      | mV    |
| <b>THERMAL SHUTDOWN</b>                  |                   |   |      |         |      |       |
| Thermal Shutdown Threshold               |                   | Guaranteed by Characterization                      |      | 150     |      | °C    |
| Thermal Shutdown Hysteresis              |                   | Guaranteed by Characterization                      |      | 25      |      | °C    |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

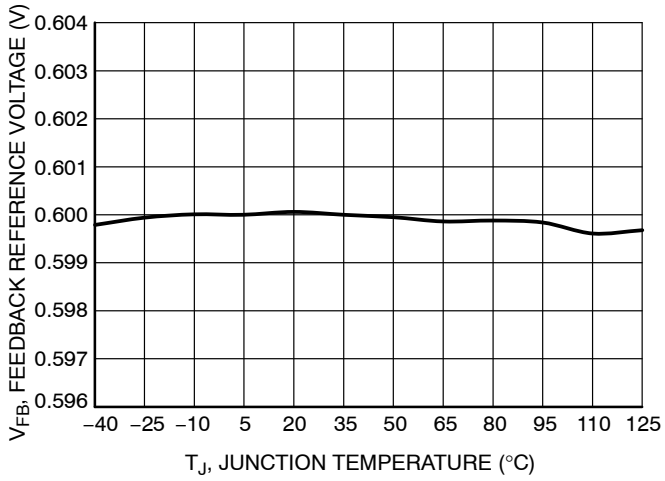


Figure 4. Reference Voltage vs. Temperature

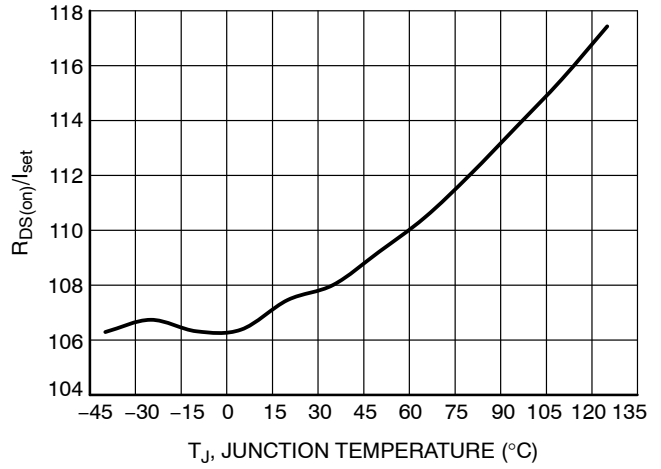


Figure 5. R<sub>DS(on)</sub>/I<sub>set</sub> vs. Temperature

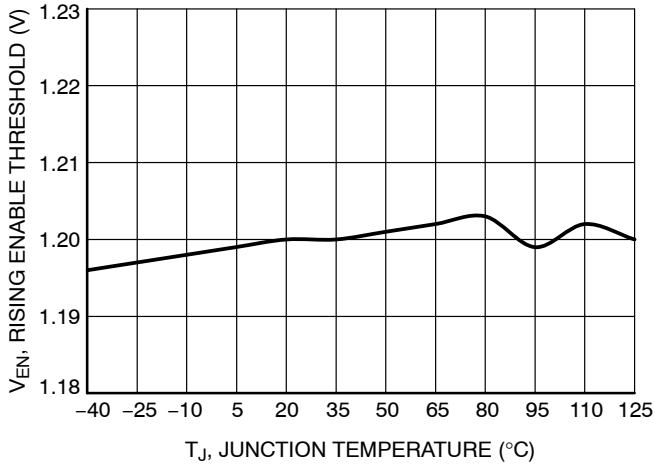


Figure 6. Rising Enable Threshold vs. Temperature

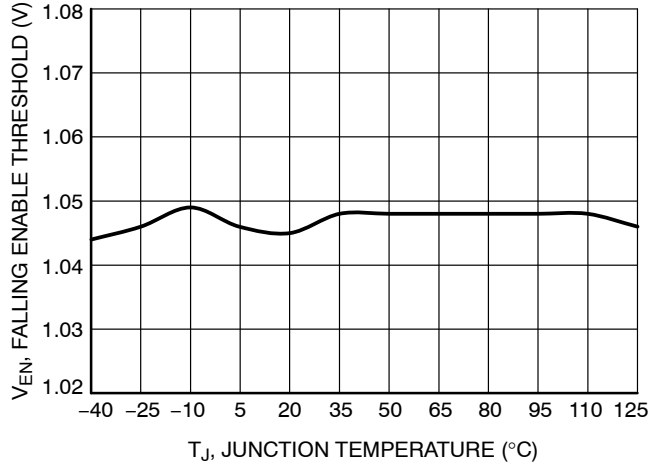


Figure 7. Falling Enable Threshold vs. Temperature

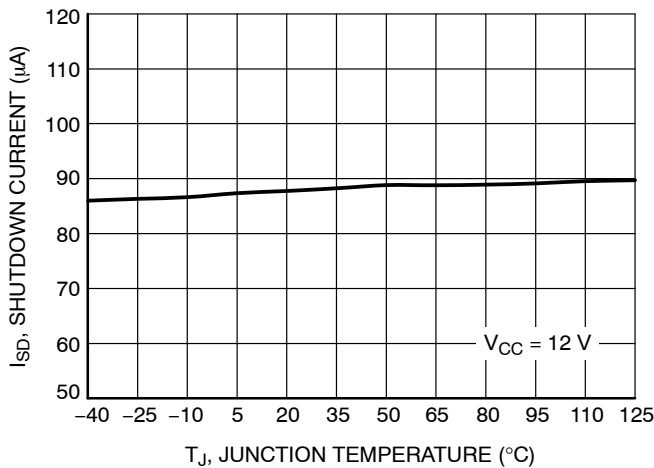


Figure 8. Shutdown Current vs. Temperature

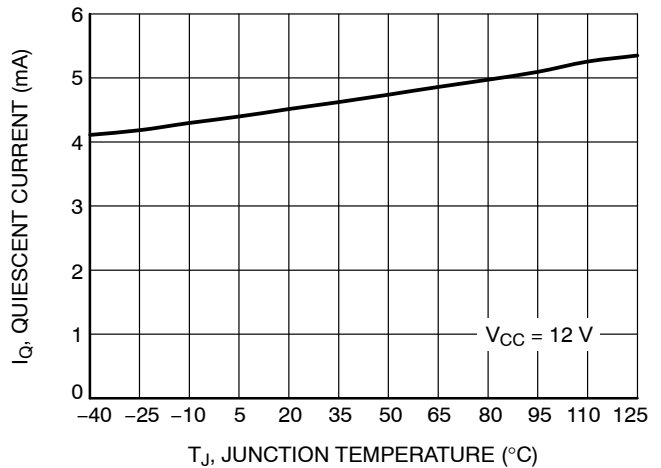


Figure 9. Quiescent Current vs. Temperature

TYPICAL CHARACTERISTICS

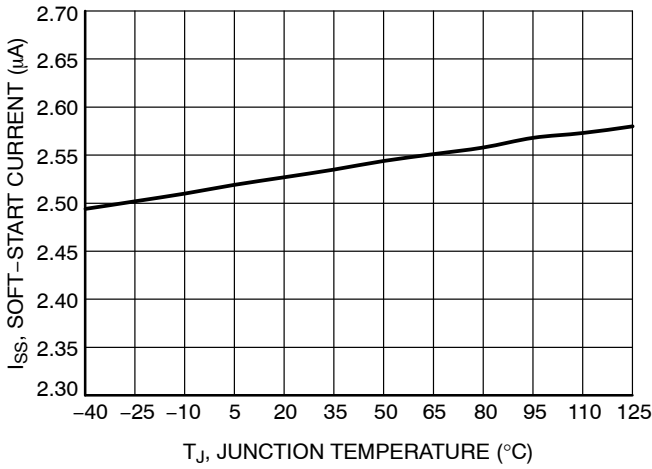


Figure 10. Soft-start Current vs. Temperature

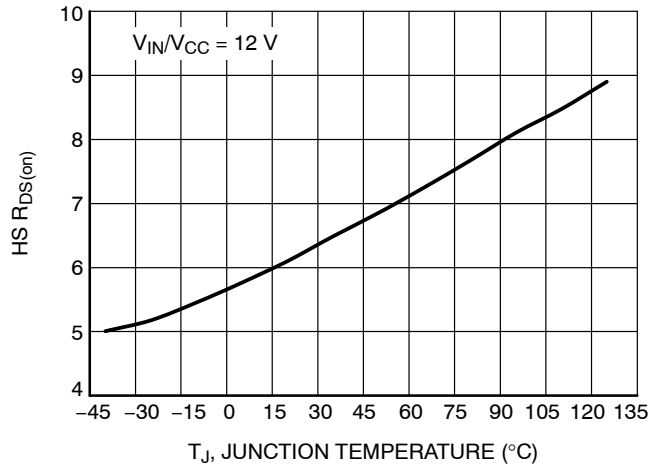


Figure 11. HS R<sub>DS(on)</sub> vs. Temperature

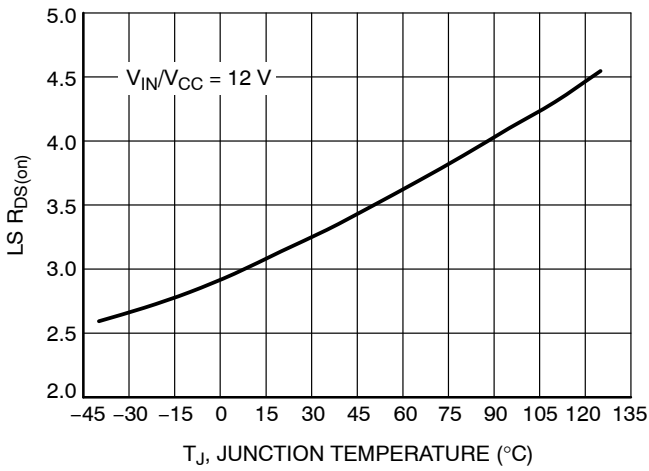


Figure 12. LS R<sub>DS(on)</sub> vs. Temperature

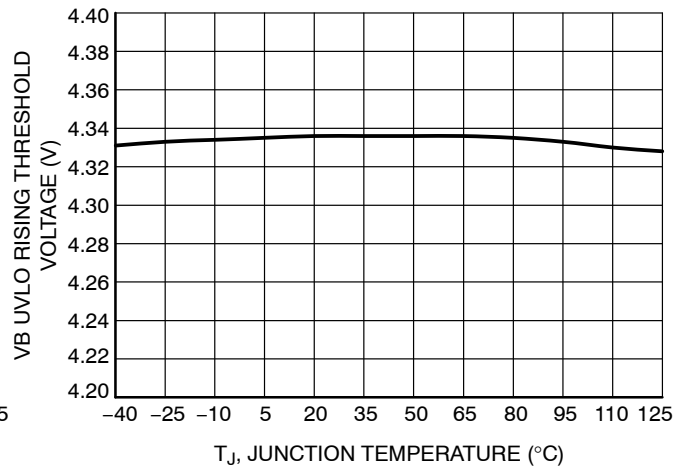


Figure 13. VB UVLO Rising Threshold vs. Junction Temperature

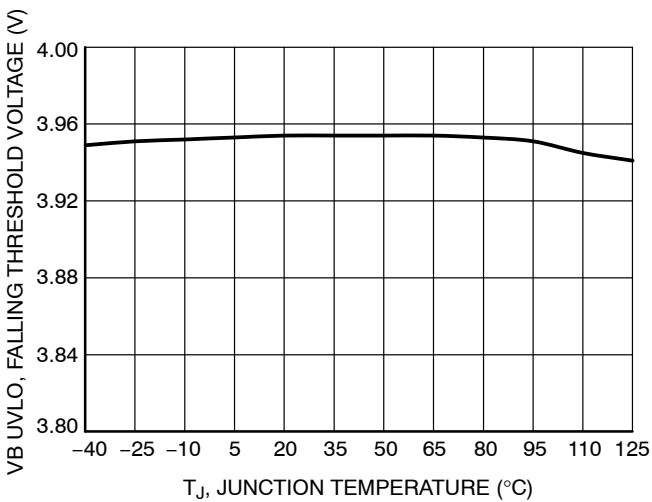


Figure 14. VB UVLO Falling Threshold vs. Junction Temperature

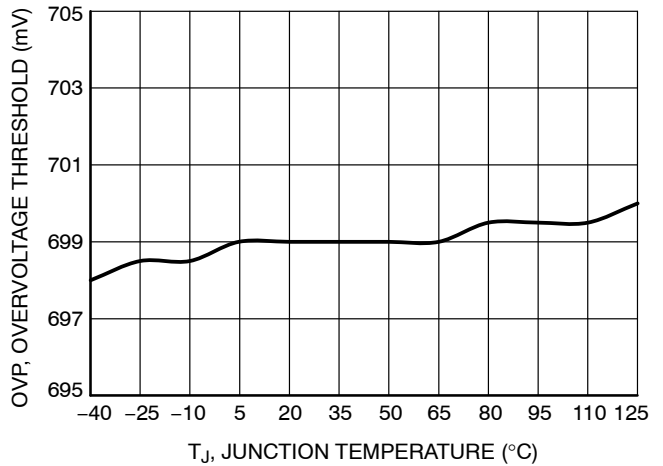


Figure 15. Output OVP vs. Junction Temperature



TYPICAL CHARACTERISTICS

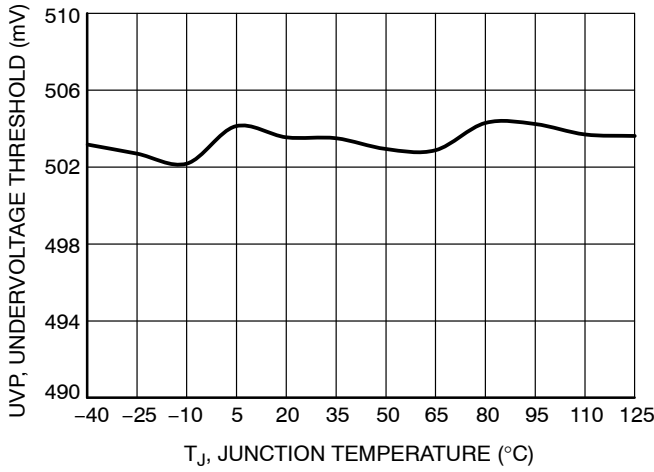


Figure 16. Output UVP vs. Junction Temperature

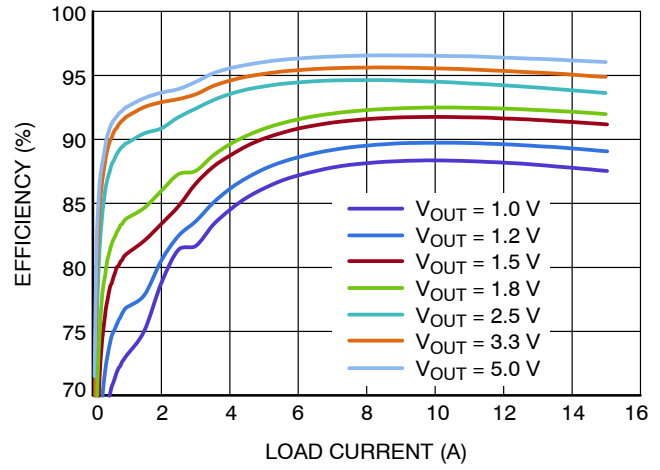


Figure 17. Efficiency ( $F_{SW} = 550 \text{ kHz}$ ,  $V_{IN} = 12 \text{ V}$ ,  $T_A = \text{Room}$ )

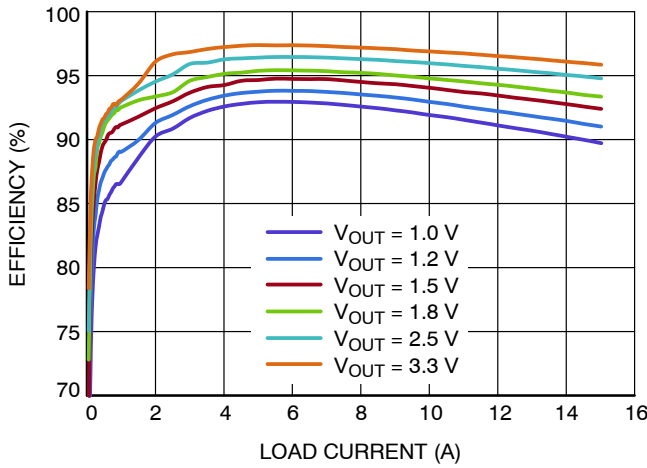


Figure 18. Efficiency ( $F_{SW} = 550 \text{ kHz}$ ,  $V_{IN} = 5 \text{ V}$ ,  $T_A = \text{Room}$ )

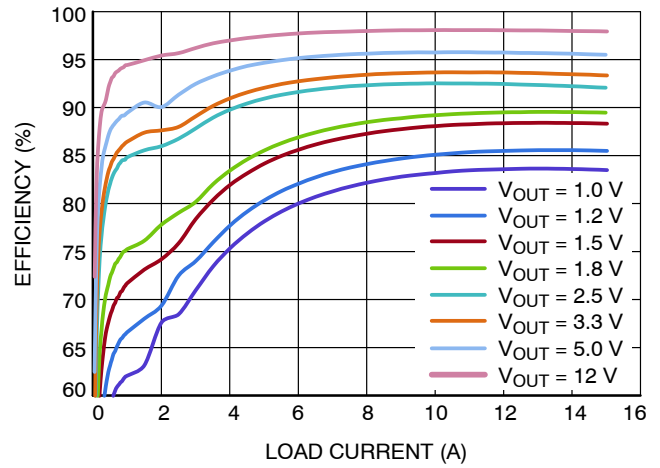


Figure 19. Efficiency ( $F_{SW} = 550 \text{ kHz}$ ,  $V_{IN} = 19 \text{ V}$ ,  $T_A = \text{Room}$ )

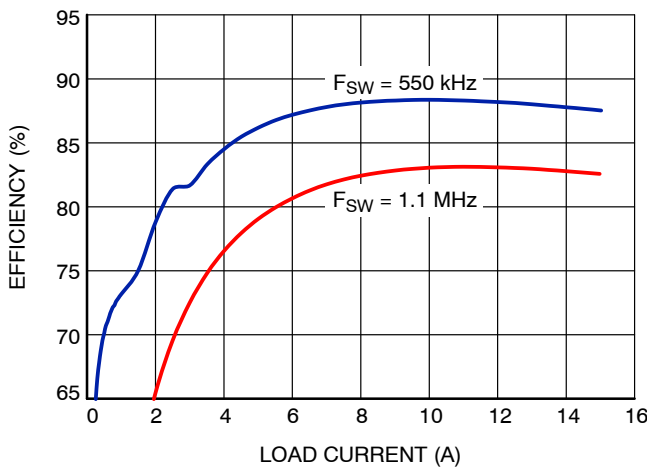


Figure 20. Efficiency ( $V_{OUT} = 1.0 \text{ V}$ ,  $V_{IN} = 12 \text{ V}$ ,  $T_A = \text{Room}$ )

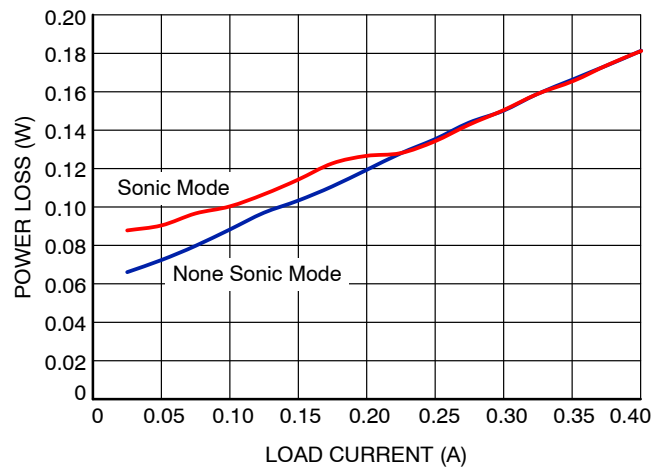
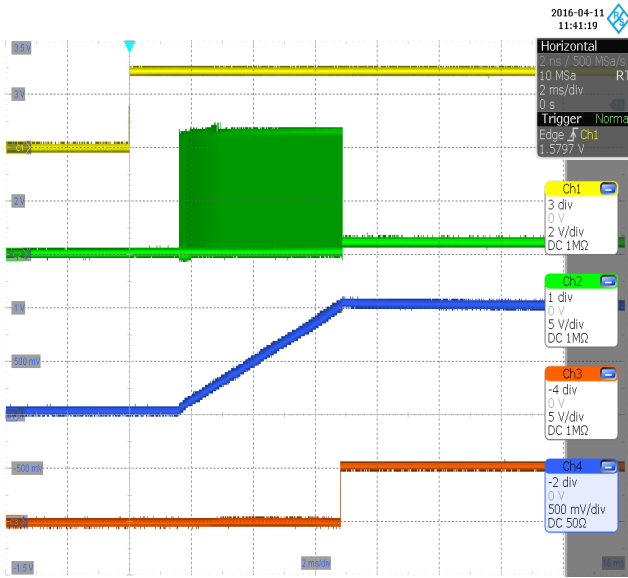


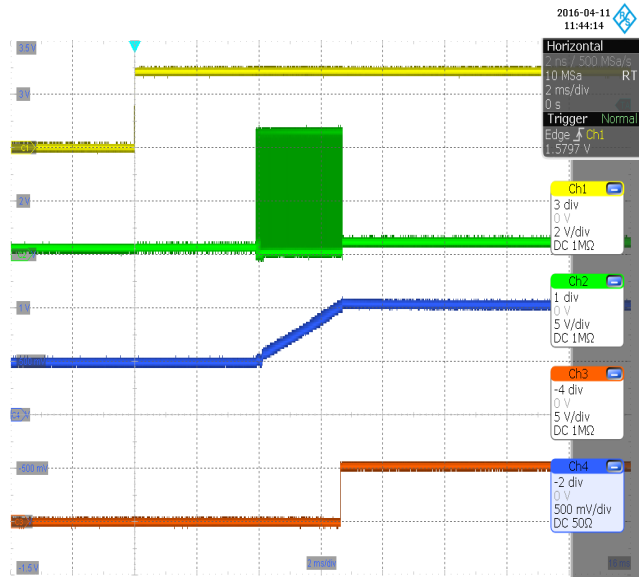
Figure 21. Power Loss Difference ( $V_{OUT} = 1.0 \text{ V}$ ,  $V_{IN} = 12 \text{ V}$ ,  $T_A = \text{Room}$ )

TYPICAL CHARACTERISTICS



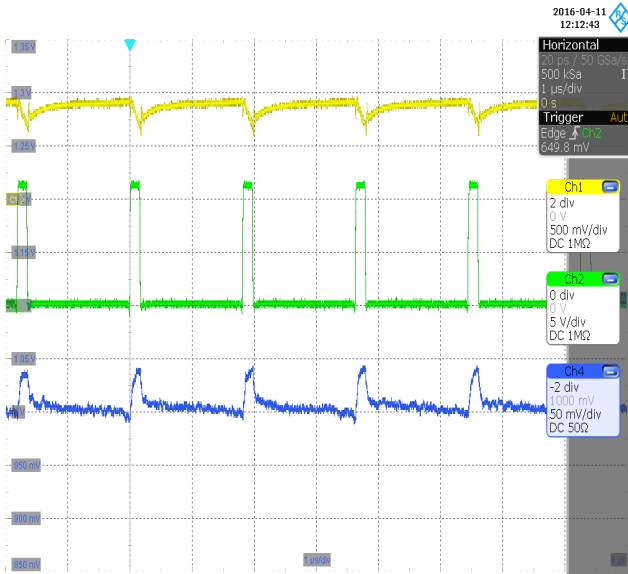
CH1 (Yellow): EN  
 CH2 (Green): VSW  
 CH3 (Orange): PG  
 CH4 (Blue): Vout

Figure 22. Soft Start Waveform (no load, sonic mode disabled)



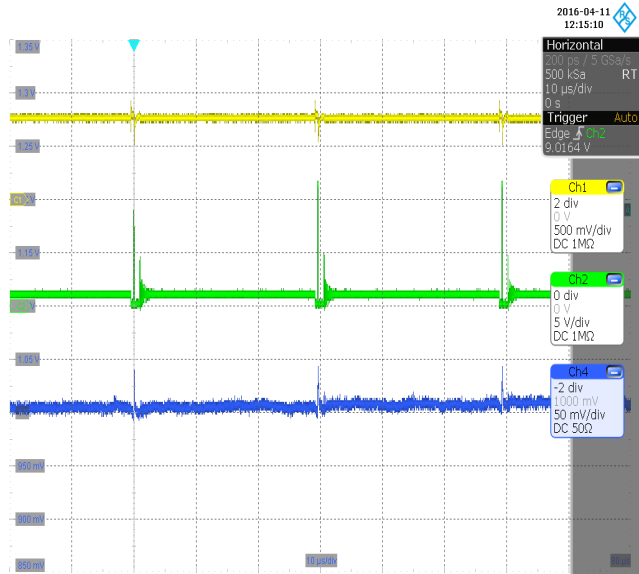
CH1 (Yellow): EN  
 CH2 (Green): VSW  
 CH3 (Orange): PG  
 CH4 (Blue): Vout

Figure 23. Pre-biased Soft Start Waveform (no load, sonic mode disabled)



CH1 (Yellow): COMP  
 CH2 (Green): VSW  
 CH3 (Blue): Vout

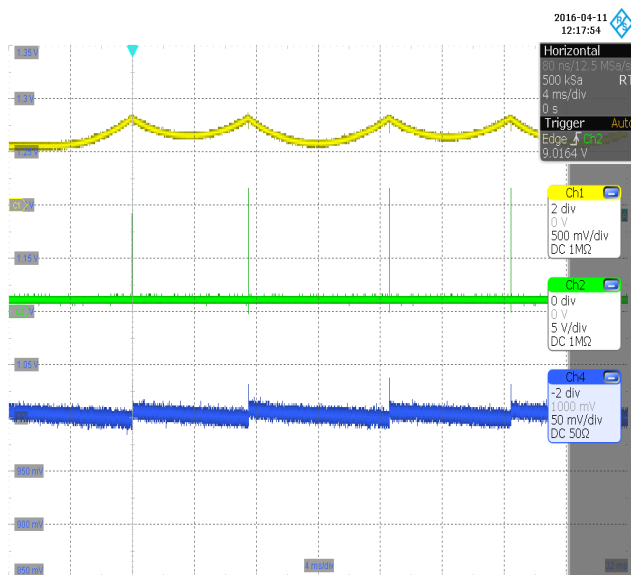
Figure 24. Steady-state CCM Operation (load = 10 A)



CH1 (Yellow): COMP  
 CH2 (Green): VSW  
 CH3 (Blue): Vout

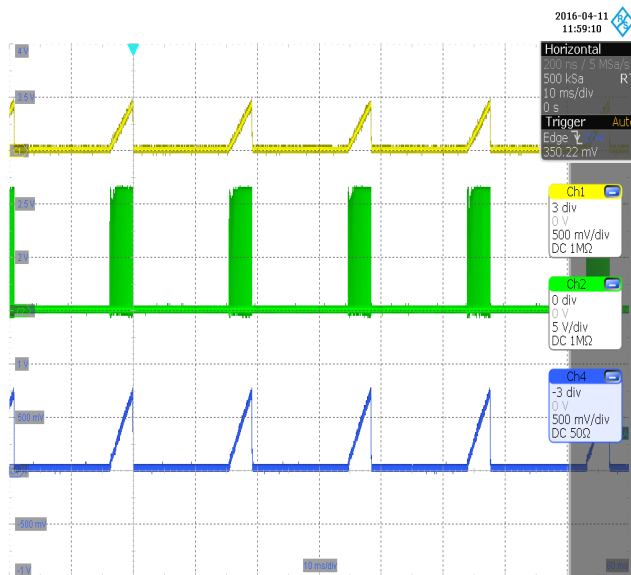
Figure 25. Steady-state DCM Operation (load = 0 A), sonic mode (enabled) limits switching frequency around 30 kHz

TYPICAL CHARACTERISTICS



CH1 (Yellow): COMP  
 CH2 (Green): VSW  
 CH3 (Blue): Vout

**Figure 26. Stead-state DCM Operation (load = 0 A), sonic mode (disabled) allows switching frequency drop to about 100 Hz**



CH1 (Yellow): SS pin  
 CH2 (Green): VSW  
 CH3 (Blue): Vout

**Figure 27. Hiccup in Over Current Protection**

## OPERATION DESCRIPTION

The NCP3235 is a high efficiency, high current PWM synchronous buck converter. It operates with a single supply voltage from 4.5 to 23 V and provides output current as high as 15 A. NCP3235 utilizes voltage mode with voltage feed-forward control to respond instantly to input voltage changes and provide for easier compensation over the supply range of the converter. The device also includes pre-bias startup capability to allow monotonic startup in the event of a pre-biased output condition.

The NCP3235 provides two operation modes to fit various application requirements. The automatic CCM/DCM mode operation provides reduced power loss and increases the efficiency at light load. The adaptive power control

architecture enables smooth transition between light load and heavy load while maintaining fast response to load transients.

Protection features include overcurrent protection (OCP), output over and under voltage protection (OVP, UVP), and power good indicator. The enable function is highly programmable to allow for adjustable startup voltages at higher input voltages. There is also an adjustable soft-start, and internal thermal shutdown.

**Operation Mode**

The NCP3235 offers five options programmed by MODE pin connections, see Table 5 below.

**Table 5. OPERATION MODE SELECTION**

| MODE pin Connection           | Switching Frequency | Operation Mode    | Overvoltage Protection | Sonic Mode  |
|-------------------------------|---------------------|-------------------|------------------------|-------------|
| GND                           | 550 kHz             | Automatic CCM/DCM | Latch off              | enabled     |
| 49.9 k $\Omega$ ( $\pm 1\%$ ) | 550 kHz             | Automatic CCM/DCM | Latch off              | disabled    |
| 100 k $\Omega$ ( $\pm 1\%$ )  | 1.1 MHz             | Automatic CCM/DCM | Latch off              | enabled     |
| 174 k $\Omega$ ( $\pm 1\%$ )  | 1.1 MHz             | FCCM              | Hiccup                 | not applied |
| Floating                      | 1.1 MHz             | Automatic CCM/DCM | Latch off              | disabled    |

In forced continuous conduction mode (FCCM), the high-side FET is ON during the on-time and the low-side FET is ON during the off-time. The switching is synchronized to an internal clock thus the switching frequency is fixed.

In Automatic CCM/DCM mode, the high-side FET is ON during the on-time and low-side FET is ON during the off-time until the inductor current reaches zero. An internal zero-crossing comparator detects the zero crossing of the inductor current from positive to negative. When the inductor current reaches zero, the comparator sends a signal to the logic circuitry and turns off the low-side FET.

When the load is increased, the inductor current is always positive and the zero-crossing comparator does not send any zero-crossing signal. The converter enters into continuous conduction mode (CCM) when no zero-crossing is detected for two consecutive PWM pulses. In CCM mode, the switching synchronizes to the internal clock and the switching frequency is fixed.

For high output voltage more than 1.8 V, recommend mode selection of either FCCM or sonic mode enabled to avoid low voltage in BST cap at no-load condition.

**Automatic Power Saving Mode**

In Automatic CCM/DCM mode when the load current decreases, the converter will enter power saving mode operation. During power saving mode, the low-side MOSFET will turn off when the inductor current reaches

zero. So the converter skips switching and operates with reduced frequency, which minimizes the quiescent current and maintains high efficiency. When sonic mode is enabled, the lowest switching frequency is limited above 30 kHz to stay out of audible noise frequency range.

**Forced Continuous Conduction Mode**

When MODE pin is connected with 175 k $\Omega$  resistor, the NCP3235 is operating in forced continuous conduction mode in both light load and heavy load conditions. In this mode, the switching frequency remains constant over the entire load range, making it suitable for applications that need tight regulation of switching frequency at a cost of lower efficiency at light load.

**Reference Voltage**

The NCP3235 incorporates an internal reference that allows output voltages as low as 0.6 V. The tolerance of the internal reference is guaranteed over the entire operating temperature range of the controller. The reference voltage is trimmed using a test configuration that accounts for error amplifier offset and bias currents.

**Oscillator Ramp**

The ramp waveform is a saw-tooth form at the PWM frequency with a peak-to-peak amplitude of  $V_{CC}/6.0$ , offset from GND by typically 0.64 V. The PWM duty cycle is limited to a maximum of 92%, allowing the bootstrap capacitors to charge during each cycle.

**Error Amplifier**

The error amplifier’s primary function is to regulate the converter’s output voltage using a resistor divider connected from the converter’s output to the FB pin of the controller, as shown in the Applications Schematic. A type III compensation network must be connected around the error amplifier to stabilize the converter. It has a bandwidth of greater than 24 MHz, with open loop gain of at least 60 dB.

**Programmable Soft-Start**

An external capacitor connected from the SS pin to ground sets up the soft start period, which can limit the start-up inrush current. The soft start period can be programmed based on the Equation 1.

$$t_{SS} = \frac{C_{SS} \cdot V_{ref}}{I_{SS}} \quad (\text{eq. 1})$$

OCP and TSD (thermal shutdown) are the only protections that are active during a soft-start.

**Adaptive Non-Overlap Gate Driver**

In a synchronous buck converter, a certain dead time is required between the low side drive signal and high side drive signal to avoid shoot through. During the dead time, the body diode of the low side FET freewheels the current. The body diode has much higher voltage drop than that of the MOSFET, which reduces the efficiency significantly. The longer the body diode conducts, the lower the efficiency. NCP3235 implements adaptive dead time control to minimize the dead time, as well as preventing shoot through.

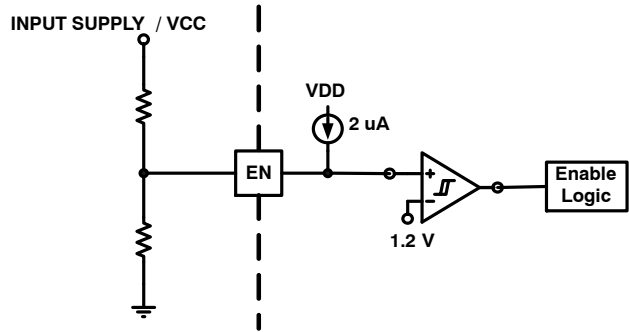
**Precision Enable (EN)**

The ENABLE block allows the output to be toggled on and off and is a precision analog input.

When the EN voltage exceeds V<sub>EN</sub>, the controller will initiate the soft-start sequence as long as the input voltage and sub-regulated voltage have exceeded their UVLO thresholds. V<sub>EN\_hyst</sub> helps to reject noise and allow the

pin to be resistively coupled to the input voltage or sequenced with other rails.

If the EN voltage is held below typically 0.8 V, the NCP3235 enters a deep disable state where the internal bias circuitry is off. As the voltage at EN continues to rise, the Enable comparator and reference are active and provide a more accurate EN threshold. The drivers are held off until the rising voltage at EN crosses V<sub>EN</sub>. An internal 2 μA pullup automatically enables the device when the EN pin is left floating.



**Figure 28. Enable Functional Block Diagram**

**Pre-bias Startup**

In some applications the controller will be required to start switching when it’s output capacitors are charged anywhere from slightly above 0 V to just below the regulation voltage. This situation occurs for a number of reasons: the converter’s output capacitors may have residual charge on them or the converter’s output may be held up by a low current standby power supply. NCP3235 supports pre-bias start up by holding off switching until the feedback voltage rises above the set regulated voltage. If the pre-bias voltage is higher than the set regulated voltage, switching does not occur until the output voltage drops back to the regulation point.

## PROTECTION FEATURES

**Hiccup Mode**

The NCP3235 uses hiccup mode for over current protection. Upon entering hiccup mode after a fault detection, the NCP3235 turns off the high side and low side FET's and PG goes low. It waits for  $t_{Hiccup}$  ms before reinitiating a soft-start.  $t_{Hiccup}$  is defined as four soft start timeouts (tss). The equation for tss is shown in Equation 1. OCP is the only active fault detection during the hiccup mode soft start.

**Over Voltage Protection (OVP)**

When the voltage at the FB pin (VFB) is above the OVP threshold for greater than 5  $\mu$ s (typical), an OVP fault is set. The high side FET (HSFET) will turn off and the low side FET (LSFET) will turn on. The open-drain PG pull down will turn on at that point as well, thus pulling PG low. Once VFB has fallen below the Undervoltage Protection Threshold (UVP), the device will enter hiccup/latch off mode. If entering latch off mode after a fault detection, the NCP3235 turns off the high side and turns on the low side FET's and PG goes low. The user has to toggle the input power supply to restart the device.

**Under Voltage Protection (UVP)**

A UVP circuit monitors the VFB voltage to detect an under voltage event. If the VFB voltage is below this threshold for more than 20  $\mu$ s, a UVP fault is set and the device will enter hiccup mode.

**Over Current Protection (OCP)**

The NCP3235 over current protection scheme senses the peak freewheeling current in the low-side FET (LSOCP) after a blanking time of 150 ns as shown in Figure 29. The low-side MOSFET drain to source voltage is compared against the voltage of an internal temperature compensated current source and a user-selected resistor RSET. The value of RSET for a given OCP level is defined by the follow equation:

$$RSET = \frac{i_{LS} \times RDSON \times 4}{i_{SET}} \quad (\text{eq. 2})$$

In this equation,  $i_{LS}$  is the inductor peak current value,  $RDSON$  is the on resistance of low-side MOSFET, and  $i_{SET}$  is an internal current source used to compensate the temperature effects of on resistance of low-side MOSFET. NCP3235 can guarantee that  $RDSON/i_{SET}$  is a constant value. By doing this, OCP accuracy won't be affected by the variation of MOSFET  $RDSON$ . In case RSET is not connected, the device switches the OCP threshold to a fixed 600 mV threshold.

After one OCP event is detected, the NCP3235 keeps the high-side MOSFET off until the low-side MOSFET falls below the trip point again and the high-side MOSFET turns on in the next clock cycle. So the low-side over current protection shows pulse skipping behavior. An internal OCP counter will count up to 3 consecutive OCP events. After the

third consecutive count, the device enters hiccup/latch mode. The scheme of LS OCP and hiccup mode protection is described in Figure 29.

**Thermal Shutdown (TSD)**

The NCP3235 protects itself from overheating with an internal thermal monitoring circuit. If the junction temperature exceeds the thermal shutdown threshold both the upper and lower MOSFETs will be shut OFF. Once the temperature drops below the falling hysteresis threshold, the voltage at the COMP pin will be pulled below the ramp valley voltage and a soft-start will be initiated.

**Power Good Monitor (PG)**

NCP3235 monitors the output voltage and signal when the output is out of regulation or during a non-regulated pre-bias condition, or fault condition. When the output voltage is within the OVP and UVP thresholds, the power good pin is a high impedance output. If the NCP3235 detects an OCP, OVP, UVP, TSD or is in soft start, it pulls PG pin low. The PG pin is an open drain 5-mA pull down output.

**Layout Guide**

When laying out a power PCB for the NCP3235 there are several key points.

General Layout Guide: these are the common techniques for high frequency high power board layout design.

Base component placement: High current path components should be placed to keep the current path as tight as possible. Placement of components on the bottom of the board such as input or output decoupling can add loop inductance.

Ground Return for Power and Signals: Solid, uninterrupted ground planes must be present and adjacent to the high current path.

Copper Shapes on Component Layers: Large copper planes on one or multiple layers with adequate vias will increase thermal transfer, reduce copper conduction losses, and minimize loop inductance. Greater than 20 A designs require 2~3 layer shapes or more, increasing the number of layers will only improvement performance.

Via Placement for Power and Ground: Place enough vias to adequately connect outer layers to inner layers for thermal transfer and to minimize added inductance in layer transition. Multiple vias should be placed near important components like input and output ceramic capacitors.

Key Signal Routes: Do not route sensitive signals, such as FB near or under noisy nets such as the switch node VSW and BST node, to reduce noise coupling effects on the sensitive lines.

To improve the Low-side OCP accuracy, users should use single ground connection instead of separate analog ground and power ground. Make sure that the inner layers (at least 2nd layer, 3rd layer and 4th layer) are dedicated for ground plane. Do not use other copper planes to break or interrupt

# NCP3235

the shape of ground plane, which may add more parasitic components to affect the sensing accuracy.

Thermal management consideration: the major heat flow path from package to the ambient is through the copper on the PCB, the area and thickness of copper plane affect the thermal performance; maximize the copper coverage on all the layers to increase the effective thermal conductivity of the board. This is important especially when there is no heat sinks attached to the PCB on the other side of the package. Add as many thermal vias as possible directly under the package ground pad to maximize the effective out-of-plane

thermal conductivity of the board; all the thermal vias must be either plated (copper) shut or plugged and capped on both sides of the board. This prevents solder seeping in to the thermal vias causing solder voids. Solder voids are detrimental to the thermal and electrical performance of the package; to ensure reliability and performance, the solder coverage should be at least 85 percent. This means the total voids on the ground pad should be less than 15 percent with no single void larger than 1 mm. Several smaller voids are always better than a few big voids.

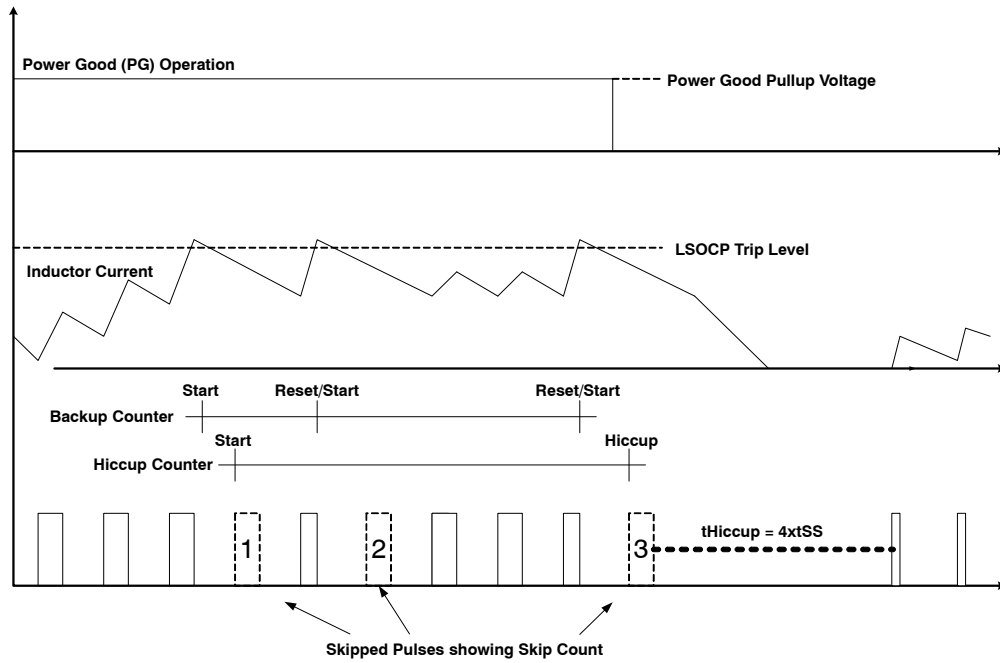
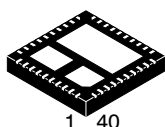


Figure 29. LSOCP Function with Counters and Power Good Shown (exaggerated for informational purposes)

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

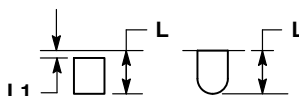
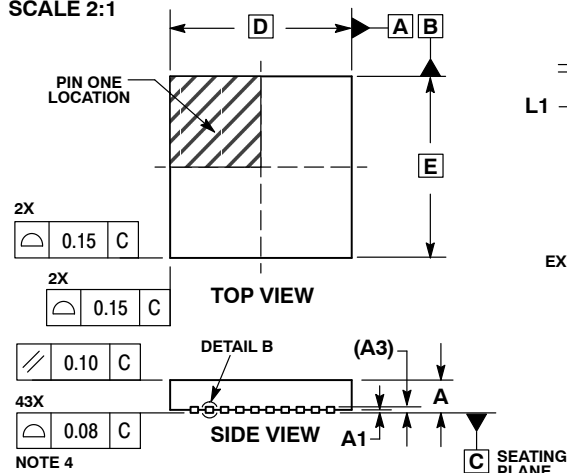
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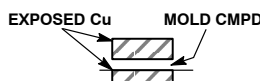
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QFN40 6x6, 0.5P  
CASE 485CM  
ISSUE O

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**DETAIL A**  
ALTERNATE  
CONSTRUCTIONS

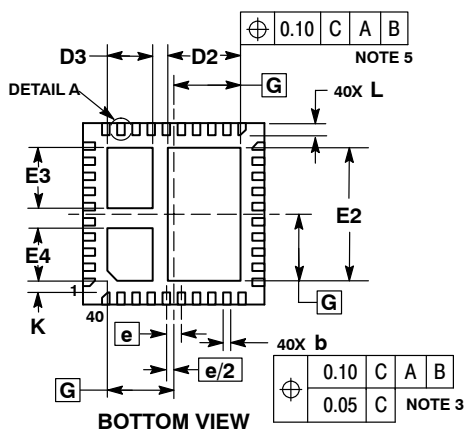


**DETAIL B**  
ALTERNATE  
CONSTRUCTION

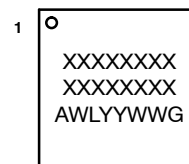
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO ALL THREE EXPOSED PADS.

| MILLIMETERS |      |      |
|-------------|------|------|
| DIM         | MIN  | MAX  |
| A           | 0.80 | 1.00 |
| A1          | ---  | 0.05 |
| A3          | 0.20 | REF  |
| b           | 0.18 | 0.30 |
| D           | 6.00 | BSC  |
| D2          | 2.30 | 2.50 |
| D3          | 1.40 | 1.60 |
| E           | 6.00 | BSC  |
| E2          | 4.30 | 4.50 |
| E3          | 1.90 | 2.10 |
| E4          | 1.64 | 1.84 |
| e           | 0.50 | BSC  |
| G           | 2.20 | BSC  |
| K           | 0.20 | ---  |
| L           | 0.30 | 0.50 |
| L1          | ---  | 0.15 |

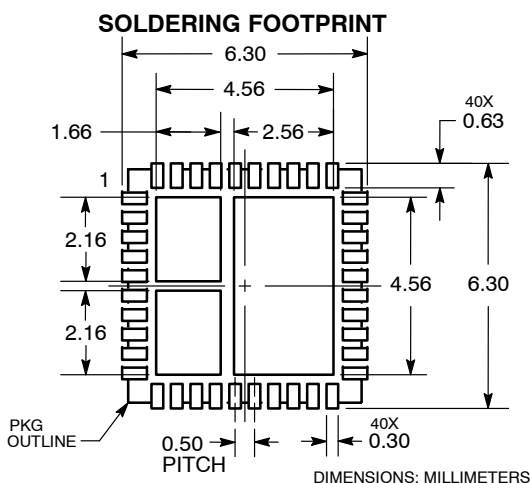


**GENERIC MARKING DIAGRAM\***



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "▪", may or may not be present.



|                         |                        |   |
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