National Semiconductor

February 2001

CLC446
400MHz, 50mW Current-Feedback Op Amp

General Description

The National CLC446 is a very high speed unity-gain-stable current-feedback op amp that is designed to deliver the highest levels of performance from a mere 50mW quiescent power. It provides a very wide 400MHz bandwidth, a 2000V/µs slew rate and 900ps rise/fall times. The CLC446 achieves its superior speed-vs-power using an advanced complementary bipolar IC process and National's current-feedback architecture.

The CLC446 is designed to drive video loads with very low differential gain and phase errors (0.02%, 0.03˚). Combined with its very low power (50mW), the CLC446 makes an excellent choice for NTSC/PAL video switchers and routers. With its very quick edge rates (900ps) and high slew rate (2000V/µs), the CLC446 also makes an excellent choice for high speed, high resolution component RGB video systems.

The CLC446 makes an excellent low power, high resolution A/D converter driver with its very fast 9ns settling time (to 0.1%) and low harmonic distortion.

The combination of high performance and low power make the CLC446 useful in many high speed general purpose applications. Its current-feedback architecture maintains consistent performance over a wide gain range and signal levels. DC gain and bandwidth can be set independently. Also, either maximally flat AC response or linear phase response can be emphasized.

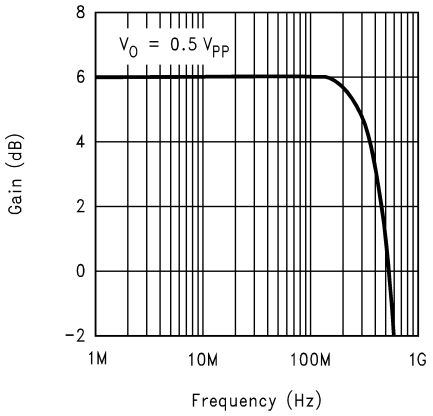
Features

- 400MHz bandwidth (A_V = +2)
- 5mA supply current
- 0.02%, 0.03˚ differential gain, phase
- 2000V/µs slew rate
- 9ns settling to 0.1%
- 0.05dB gain flatness to 100MHz
- −65/−78dBc HD2/HD3

Applications

- High resolution video
- A/D driver
- Medical imaging
- Video switchers & routers
- RF/IF amplifier
- Communications
- Instrumentation

Non-Inverting Frequency Response (A_V = +2)



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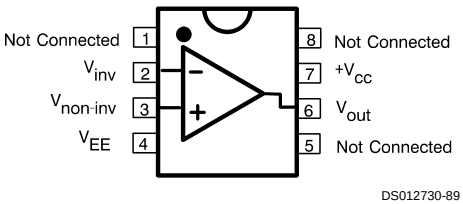
Connection Diagram



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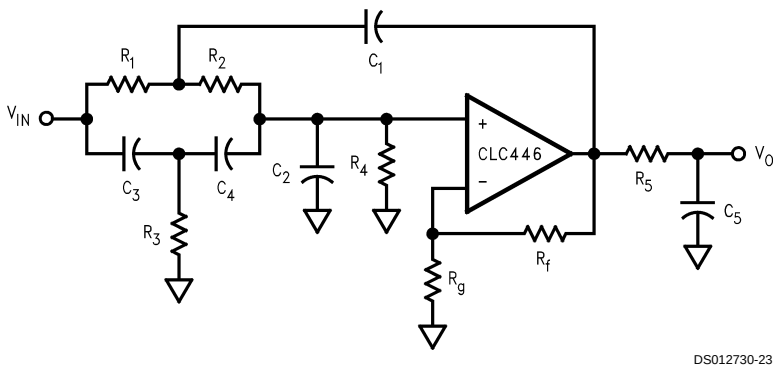
Pinout
DIP & SOIC

Typical Application



Elliptic-Function Low Pass Filter

Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
8-pin plastic DIP	−40˚C to +85˚C	CLC446AJP	CLC446AJP	N08E
8-pin plastic SOIC	−40˚C to +85˚C	CLC446AJE	CLC446AJE	M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±6V
Output Current	±48mA
Common Mode Input Voltage	$\pm V_{CC}$
Maximum Junction Temperature	+150˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Solder Duration (+300˚C)	10 sec
ESD Rating (human body model)	1000V

Operating Ratings

Thermal Resistance		
Package	(θ_{JC})	(θ_{JA})
MDIP	70˚C/W	125˚C/W
SOIC	60˚C/W	140˚C/W

Electrical Characteristics

A_V = +2, V_{CC} = ±5V, R_L = 100Ω, R_f = 249Ω; unless specified

Symbol	Parameter	Conditions	Typ	Min/Max (Note 2)			Units
Ambient Temperature		CLC446AJ	+25˚C	+25˚C	o to 70˚C	−40 to 85˚C	
Frequency Domain Response							
	-3dB Bandwidth	V_O <0.2V_{PP}	400	340	300	300	MHz
		V_O<2.0V_{PP}	280	210	190	190	MHz
	Gain Flatness V_O< 2.0V_{PP}	<100MHz	±0.05	±0.2	±0.2	±0.2	dB
	Linear Phase Dev. V_O< 2.0V_{PP}	<100MHz	0.2	0.5	0.8	0.8	deg
	Differential Gain	NTSC, R_L = 150Ω	0.02	0.04	0.04	0.04	%
	Differential Phase	NTSC, R_L = 150Ω	0.03	0.05	0.05	0.05	deg
Time Domain Response							
	Rise and Fall Time	2V Step	0.9	1.4	1.5	1.6	ns
	Settling Time to ±0.1%	2V Step	9	13	15	15	ns
	Overshoot	2V Step	6	15	18	18	%
	Slew Rate	2V Step, ±0.5V Crossing	2000	1400	1300	1200	V/µs
Distortion And Noise Response							
	2nd Harmonic Distortion	2V_{PP},5MHz	−65	−59	−58	−58	dBc
		2V_{PP},20MHz	−55	−48	−48	−48	dBc
		2V_{PP},50MHz	−54	−43	−42	−42	dBc
	3rd Harmonic Distortion	2V_{PP}, 5MHz	−78	−70	−68	−68	dBc
		2V_{PP},20MHz	−70	−62	−60	−60	dBc
		2V_{PP},50MHz	−50	−45	−42	−42	dBc
	Equivalent Input Noise						
	Voltage (e_{ni})	>1MHz	3.8	4.8	5.0	5.1	nV/$\sqrt{Hz}$
	Non-Inverting Current (i_{bn})	>1MHz	2.0	2.6	2.8	3.3	pA/$\sqrt{Hz}$
	Inverting Current (i_{bi})	>1MHz	16	19	20	21	pA/$\sqrt{Hz}$
Static, DC Performance							
	Input Offset Voltage (Note 3)		2	7	10	11	mV
	Average Drift		17	-	25	35	µV/C˚
	Input Bias Current (Note 3)	Non-Inverting	3	12	25	25	µA
	Average Drift		30	-	90	130	nA/C˚
	Input Bias Current (Note 3)	Inverting	10	22	30	35	µA
	Average Drift		26	-	75	85	nA/C˚
	Power Supply Rejection Ratio	DC	52	45	43	43	dB
	Common Mode Rejection Ratio	DC	48	44	42	42	dB
	Supply Current (Note 3)	R_L = ∞	4.8	5.8	6.2	6.2	mA

Electrical Characteristics (Continued)

A_V = +2, V_{CC} = ±5V, R_L = 100Ω, R_f = 249Ω; unless specified

Symbol	Parameter	Conditions	Typ	Min/Max (Note 2)			Units
Miscellaneous Performance							
	Input Resistance	Non-Inverting	1.5	1.0	0.85	0.70	MΩ
	Input Capacitance	Non-Inverting	1	2	2	2	pF
	Input Range	Common-Mode	±2.8	±2.6	±2.4	±2.3	V
	Output Voltage Range	R_L 100Ω	±3.1	±2.8	±2.8	±2.6	V
		R_L = ∞	±3.2	±3.0	±2.9	2.8	V
	Output Current		48	48	48	48	mA
	Output Resistance, Closed Loop	DC	0.04	0.1	0.1	0.1	Ω

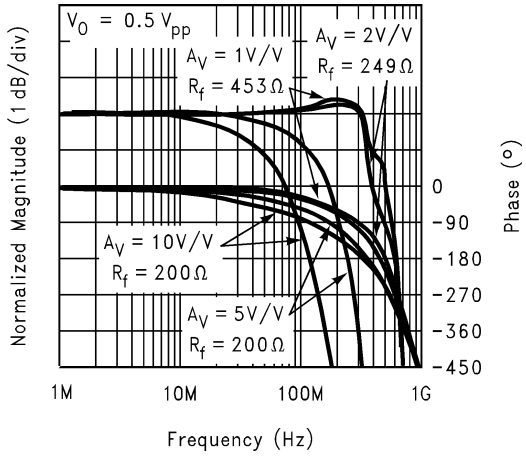
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Note 3: AJ-level: spec. is 100% tested at +25°C.

Typical Performance Characteristics (V_{CC} = ±5, A_V = +2, R_f =249Ω, R_L =100Ω; unless specified)

Non-Inverting Frequency Response



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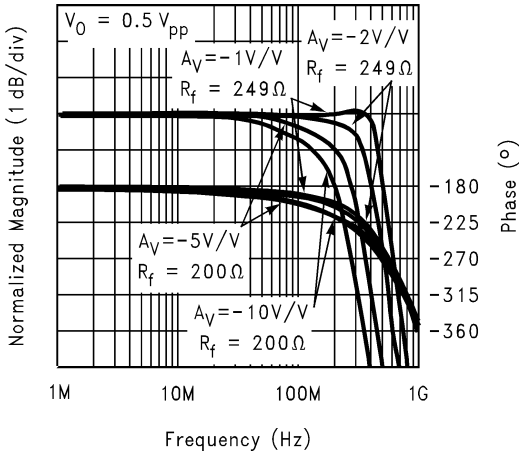
Inverting Frequency Response



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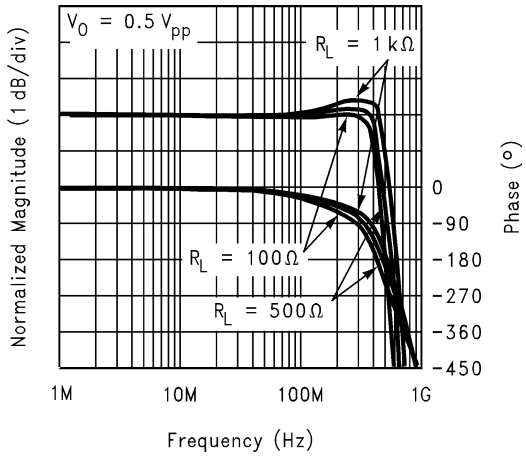
Frequency Response vs. R_L



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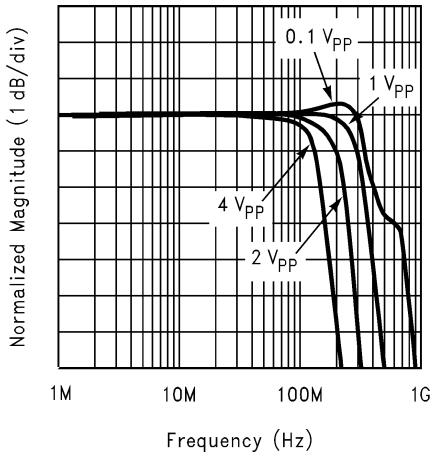
Frequency Response vs. R_O



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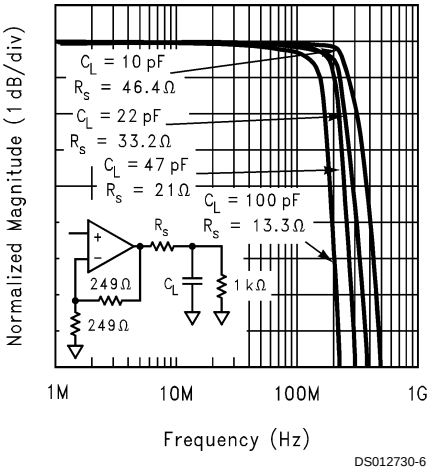
Typical Performance Characteristics (V_{CC} = ±5, A_V = +2, R_f =249Ω, R_L =100Ω; unless specified)) (Continued)

Frequency Response vs. C_L



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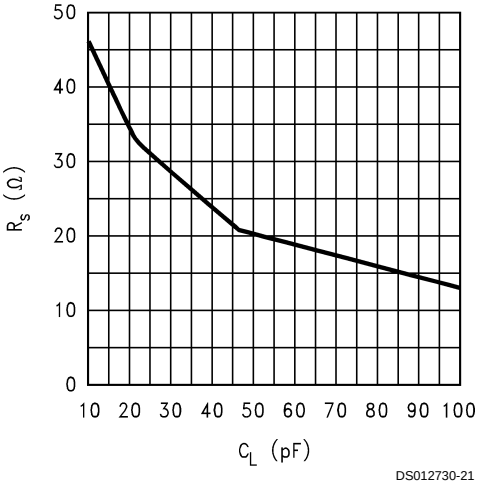
Recommended R_S vs. C_L



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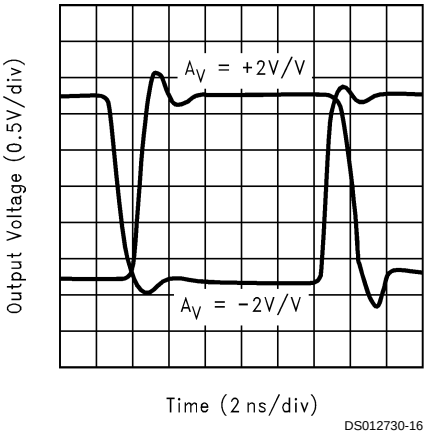
Small Signal Pulse Response



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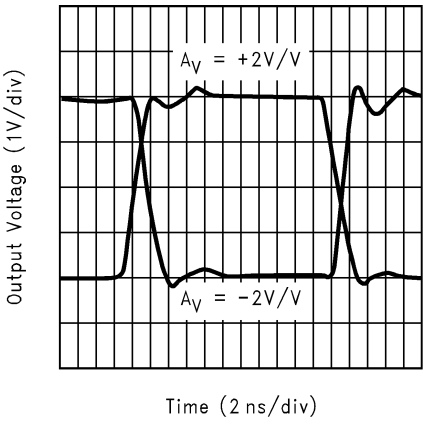
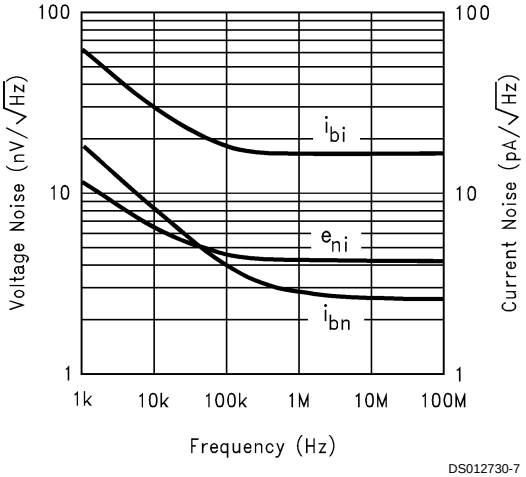
Large Signal Pulse Response



DS012730-17

Equivalent Input Noise



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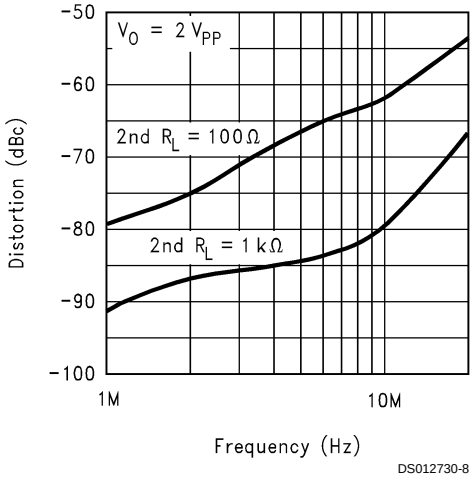
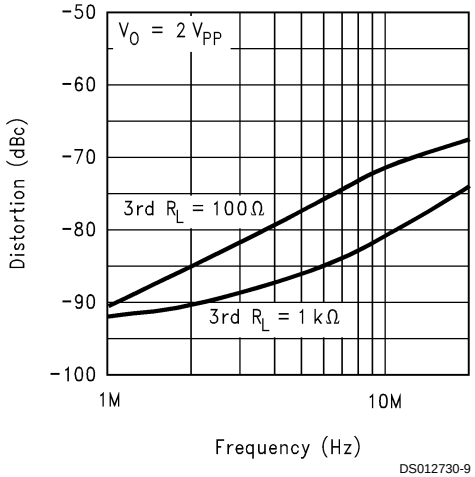
2nd Harmonic Distortion



DS012730-8

Typical Performance Characteristics (V_{CC} = ±5, A_V = +2, R_f =249Ω, R_L =100Ω; unless specified)) (Continued)

3rd Harmonic Distortion



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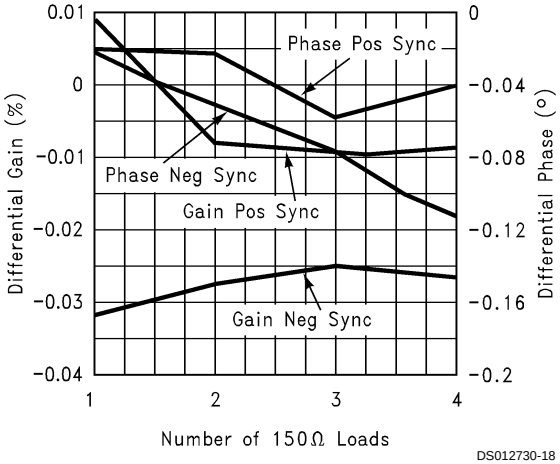
Differential Gain and Phase (3.58MHz)



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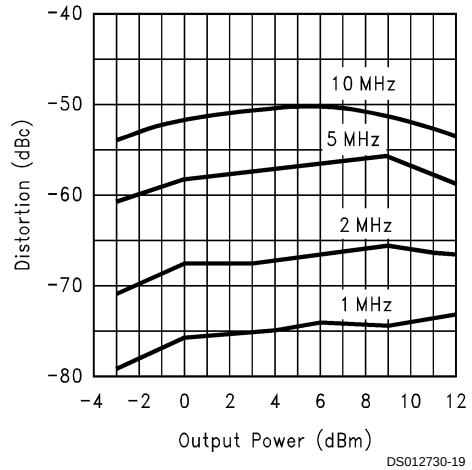
2nd Harmonic Distortion vs. P_{OUT}



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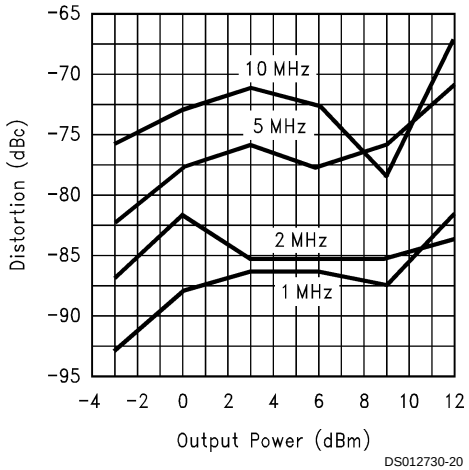
3rd Harmonic Distortion vs. P_{OUT}



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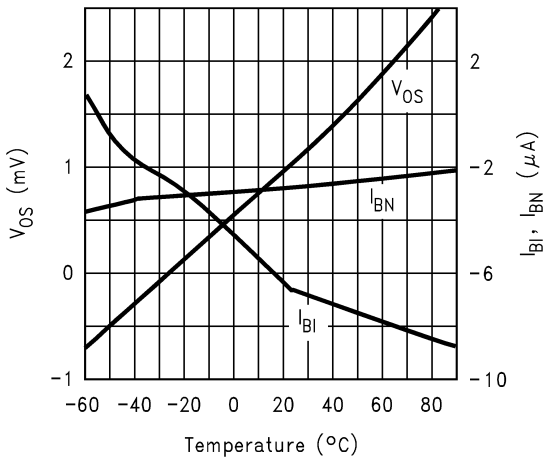
V_{OS}, I_{BN}, and I_{BI} vs. Temperature



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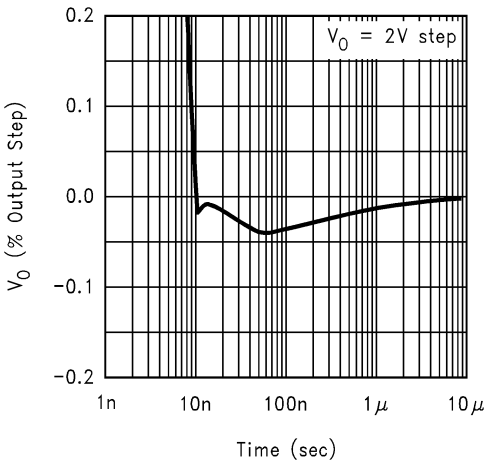
Short Term Settling Time



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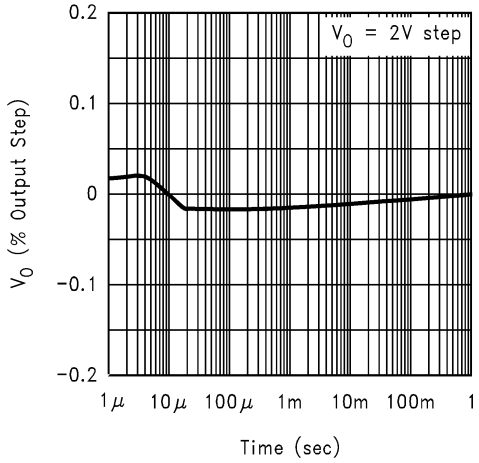
Typical Performance Characteristics (V_{CC} = ±5, A_V = +2, R_f =249Ω, R_L =100Ω; unless specified)) (Continued)

Long Term Settling Time



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Application Division

CLC446 Operation

The CLC446 has a current-feedback architecture built in an advanced complementary bipolar process. The key features of current-feedback are:

- AC bandwidth is independent of voltage gain
- Unity-gain stability
- Frequency response may be adjusted with R_f
- High slew rate
- Low variation in performance for a wide range of gains, signal levels and loads
- Fast settling

Current-feedback operation can be explained with a simple model. The voltage gain for the circuits in *Figure 1* and *Figure 2* is approximately:

$$\frac{V_o}{V_{in}} = \frac{A_V}{1+\frac{R_f}{Z(j\omega)}}$$

where:

- A_V is the DC voltage gain
- R_f is the feedback resistor
- Z(jω) is the CLC446's open-loop transimpedance gain
- $\frac{Z(j\omega)}{R_f}$ is the loop-gain

The denominator of the equation above is approximately 1 at low frequencies. Near the −3dB corner frequency, the interaction between R_f and Z(jω) dominates the circuit performance. Increasing R_f does the following:

- Decreases loop-gain
- Decreases bandwidth
- Lowers pulse response overshoot
- Reduces gain peaking
- Affects frequency response phase linearity

CLC446 Design Information

The following topics will supply you with:

- Design parameters, formulas and techniques
- Interfaces
- Application circuits
- Layout techniques
- SPICE model information

DC Gain (non-inverting)

The non-inverting DC voltage gain for the configuration shown in *Figure 1* is

$$A_V = 1+\frac{R_f}{R_g}$$

The normalized gain plots in the **Typical Performance Characteristics** section show different feedback resistors (R_f) for different gains. These values of R_f are recommended for obtaining the highest bandwidth with minimal peaking. The resistor R_t provides DC bias for the non-inverting input.

For A_V <5, use linear interpolation on the nearest A_V values to calculate the recommended value of R_f. For A_V ≥5, the minimum recommended R_f is 200Ω.

Select R_g to set the DC gain:

$$R_g = \frac{R_f}{A_V - 1}$$

Application Division (Continued)

DC gain accuracy is usually limited by the tolerance of R_f and R_g.

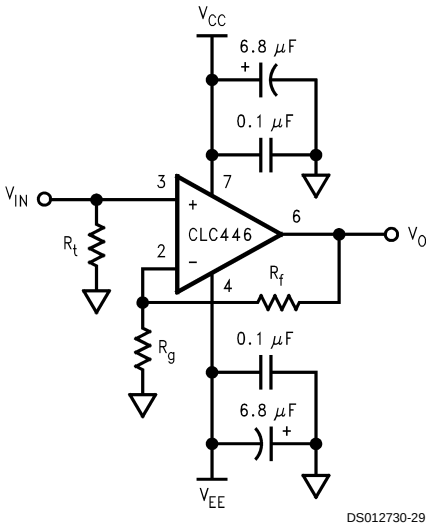


FIGURE 1. Non-Inverting Gain

DC Gain (unity gain buffer)

The recommended R_f for unity gain buffers is 453Ω. R_g is left open. Parasitic capacitance at the inverting node may require a slight increase of R_f to maintain a flat frequency response.

DC Gain (inverting)

The inverting DC voltage gain for the configuration shown in *Figure 2* is $A_V = -R_f/R_g$

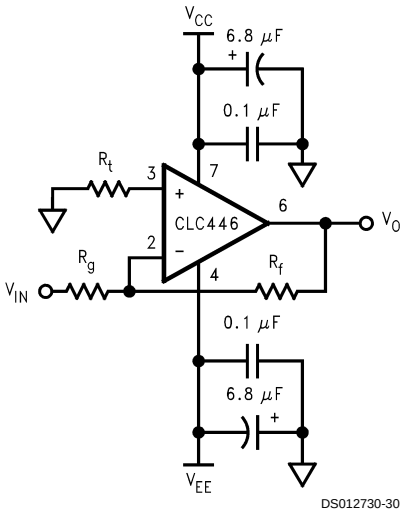


FIGURE 2. Inverting Gain

The normalized gain plots in the **Typical Performance Characteristics** section show different feedback resistors (R_f) for different gains. These values of R_f are recommended for obtaining the highest bandwidth with minimal peaking. The resistor R_t provides DC bias for the non-inverting input.

For $|A_V| < 5$, use linear interpolation on the nearest A_V values to calculate the recommended value of R_f. For $|A_V| \geq 5$, the minimum recommended R_f is 200Ω.

Select R_g to set the DC gain:

$$R_g = \frac{R_f}{|A_V|}$$

At large gains, R_g becomes small and will load the previous stage. This can be solved by driving R_g with a low impedance buffer like the CLC111, or increasing R_f and R_g. See the **AC Design (small signal bandwidth)** sub-section for the tradeoffs.

DC gain accuracy is usually limited by the tolerance of R_f and R_g.

DC Gain (transimpedance)

Figure 3 shows a transimpedance circuit where the current I_{in} is injected at the inverting node. The current source's output resistance is much greater than R_f.

The DC transimpedance gain is:

$$A_R = \frac{V_o}{I_{in}} = -R_f$$

The recommended R_f is 453Ω. Parasitic capacitance at the inverting node may require a slight increase of R_f to maintain a flat frequency response.

DC gain accuracy is usually limited by the tolerance of R_f.

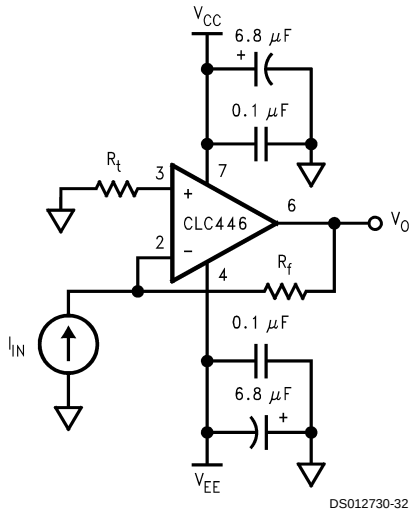


FIGURE 3. Transimpedance Gain

Application Division (Continued)

DC Design (level shifting)

Figure 4 shows a DC level shifting circuit for inverting gain configurations. V_{ref} produces a DC output level shift of

$$-V_{ref} \times \frac{R_f}{R_{ref}}$$

which is independent of the DC output produced by V_{IN}.

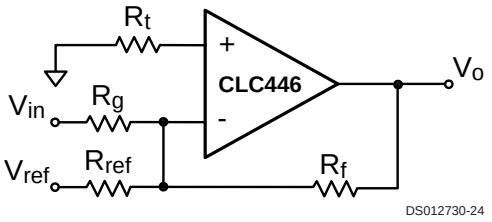


FIGURE 4. Level Shifting Circuit

DC Design (single supply)

Figure 5 is a typical single supply circuit. R_1 and R_2 from a voltage divider that sets the non-inverting input DC voltage. This circuit has a DC gain of 1. A low frequency zero is set by R_g and C_2. The coupling capacitor C_1 isolates its DC bias point from the previous stage. Both capacitors make high pass response; high frequency gain is determined by R_f and R_g.

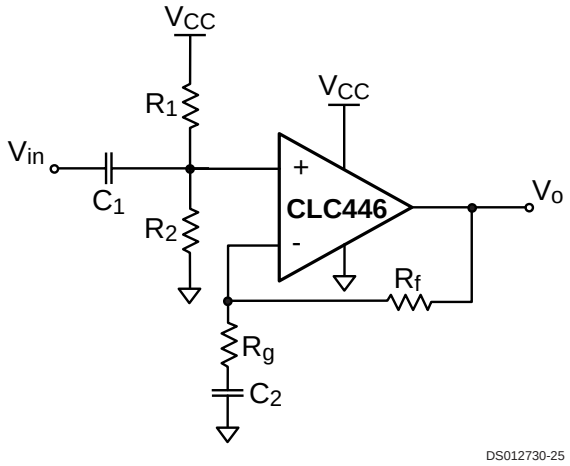


FIGURE 5. Single Supply Circuit

The complete gain equation for the circuit in *Figure 5* is:

$$\frac{V_o}{V_{in}} = \frac{s\tau_1}{1 + s\tau_1} \cdot \frac{1 + s\tau_2 \cdot \left[1 + \frac{R_f}{R_g}\right]}{1 + s\tau_2}$$

where

$s = j\omega$

$\tau_1 = (R1_1 \| R_1) \times C1$

$\tau_2 = R_g \times C_2$

DC Design (DC offsets)

The DC offset model shown in *Figure 6* is used to calculate the output offset voltage. The equation for output offset voltage is:

$$V_O = -(V_{os} + I_{BN} \cdot R_{eq1}) \cdot \left[1 + \frac{R_f}{R_{eq2}}\right] + (I_{BI} \cdot R_f)$$

The current offset terms, I_{BN} and I_{BI}, do not track each other. The specifications are stated in terms of magnitude only. Therefore, the terms V_{os},I_{BN}, and I_{BI} can have either polarity. Matching the equivalent resistance seen at both input pins does not reduce the output offset voltage.

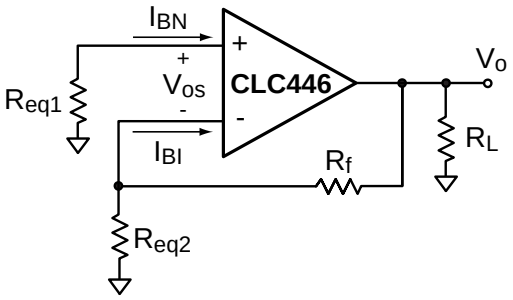


FIGURE 6. DC Offset Model

DC Design (output loading)

R_L, R_f, and R_g load the op amp output. The equivalent load seen by the output in *Figure 6* is:

$R_{L(eq)} = R_L \| (R_f + R_{eq2})$, non-inverting gain

$R_{L(eq)} = R_L \| R_f$, inverting gain

$R_{L(eq)}$ needs to be large enough so that the minimum output current can produce the required output voltage swing.

AC Design (small signal bandwidth)

The CLC446 current-feedback amplifier bandwidth is a function of the feedback resistor (R_f), not of the DC voltage gain (A_V). The bandwidth is approximately proportional to

$$\frac{1}{R_f}$$

As a rule, if R_f doubles, the bandwidth is cut in half. Other AC specifications will also be degraded. Decreasing R_f from the recommended value increases peaking, and for very small values of R_f oscillation will occur.

AC Design (minimum slew rate)

Slew rate influences the bandwidth of large signal sinusoids. To determine an approximate value of slew rate necessary to support a large sinusoid, use the following equation:

$SR \cong 5 \times f \times V_{peak}$

where V_{peak} is the peak output sinusoidal voltage.

The slew rate of the CLC446 in inverting gains is always higher than in non-inverting gains.

AC Design (linear phase/constant group delay)

The recommended value of R_f produces minimal peaking and a reasonably linear phase response. To improve phase linearity when $|A_v| < 5$, increases R_f approximately 50% over its recommended value. Some adjustment of R_f may be needed to achieve phase linearity for your application. See the **AC Design (small signal bandwidth)** a sub-section for other effects of changing R_f.

Application Division (Continued)

Propagation delay is approximately equal to group delay. Group delay is related to phase by this equation:

$$\tau_{gd} = (f) = -\frac{1}{360°} \cdot \frac{d\phi(f)}{df} \approx -\frac{\Delta\phi(f)}{\Delta f}$$

where θ(f) is the phase in degrees. Linear phase implies constant group delay. The technique for achieving linear phase also produces a constant group delay.

AC Design (peaking)

Peaking is sometimes observed with the recommended R_f. If a small increase in R_f does not solve the problem, then investigate the possible causes and remedies listed below.

■Capacitance across R_f

–Do not place a capacitor across R_f

–Use a resistor with low parasitic capacitance for R_f

■A capacitive load

–Use a series resistor between the output and a capacitive load (see the **Recommended R_s vs. C_L** plot)

■Long traces and/or lead lengths between R_f and the CLC446

–Keep these traces as short as possible

For non-inverting and transimpedance gain configurations:

■Extra capacitance between the inverting pin and gound (C_g)

–See the **Printed Circuit Board Layout** sub-section below for suggestions on reducing C_g

–Increase R_f if peaking is still observed after reducing C_g

For inverting gain configurations:

■Inadequate ground plane at the non-inverting pin and/or long traces between non-inverting pin and grouns

–Place a 50 to 100Ω resistor between the non-inverting pin and ground (see R_t in *Figure 2*)

Capacitive Loads

Capacitive loads, such as found in A/D converters, require a series resistor (R_s) in the output to improve settling performance. The **Recommended R_s vs. C_L** plot in the **Typical Performance Characteristics** section provides the information for selecting this resistor.

Using a resistor in series with a reactive load will also reduce the load's effect on amplifier loop dynamics. For instance, driving coaxial cables without an output series resistor may cause peaking or oscillation.

Transmission Line Matching

One method for matching the characteristic impedance of a transmission line is to place the appropriate resistor at the input or output of the amplifier. *Figure 7* shows the typical circuit configurations for matching transmission lines.

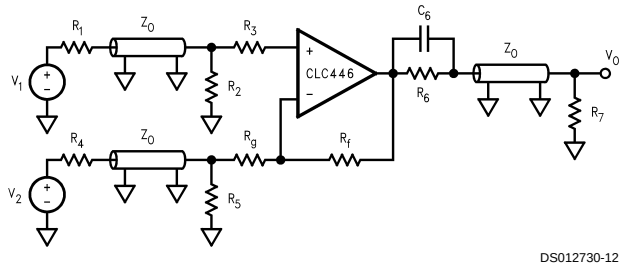


FIGURE 7. Transmission Line Matching

In non-inverting gain applications, R_g is connected directly to ground. The resistors R_1, R_2, R_6, and R_7 are equal to the characteristic impedance, Z_0 of the transmission line or cable. Use R_3 to isolate the amplifier from reactive loading caused by the transmission line, or by parasitics.

In inverting gain applications, R_3 is connected directly to ground. The resistor R_4, R_6, and R_7 are equal to Z_0. The parallel combination of R_5 and R_g is also equal to Z_0.

The input and output matching resistors attenuate the signal by a factor of 2, therefore additional gain is needed. Use C_6 to match the output transmission line over a greater frequency range. It compensates for the increase of the op amp's output impedance with frequency.

Thermal Design

To calculate the power dissipation for the CLC446, follow these steps:

1. Calculate the no-load op amp power:

   $P_{amp} = I_{CC} (V_{CC}-V_{EE})$

2. Calculate the output stage's RMS power:

   $P_o = (V_{CC} - V_{load})\ I_{load}$, where V_{load} and I_{load} are the RMS voltage and current across the external load.

3. Calculate the total op amp RMS power:

   $P_t = P_{amp} + P_o$

To calculate the maximum allowable ambient temperature, solve the following equation: $T_{amb} = 150 - P_t\ \theta_{JA}$ where θ_{JA} is the thermal resistance from junction to ambient in ˚C/W, and T_{amb} is in ˚C. The **Package Thermal Resistance** section contains the thermal resistance for various packages.

Dynamic Range (input/output protection)

ESD diodes are present on all connected pins for protection from static voltage damage. For a signal that may exceed the supply voltages, we recommend using diode clamps at the amplifier's input to limit the signals to less than the supply voltages.

Dynamic Range (input/output levels) The **Electrical Characteristics** section specifies the Common-Mode Input Range and Output Voltage Range; these voltage ranges scale with the supplies. Output Current also specified in the **Electrical Characteristics** section.

Unity gain applications are limited by the Common-Mode Input Range. At greater non-inverting gains, the Output Voltage Range becomes the limiting factor. Inverting gain applications are limited by the Output Voltage Range. For transimpedance gain applications, the sum of the input currents injected at the inverting input pin of the op amp needs to be:

$$|I_{in}| \leq \frac{V_{max}}{R_f}$$

where V_{max} is the Output Voltage Range (see the **DC Gain (transimpedance)** sub-section for details.

The equivalent output load needs to be large enough so that the minimum output current can produce the required output voltage swing. See the **DC Design (output loading)** sub-section for details.

Dynamic Range (noise)

In RF applications, noise is frequently specified as Noise Figure (NF). This allows the calculation of signal to noise ratio into a defined load. *Figure 8* plots the NF for a CLC446 at a gain of 10, and with a feedback resistor R_f of 100Ω. The minimum NF (3.9dB) occurs when the source impedance equals 1600Ω.

Application Division (Continued)

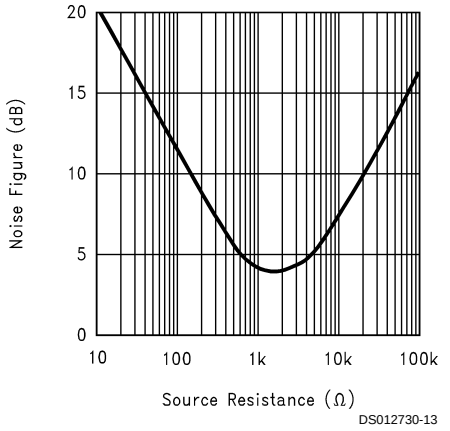


FIGURE 8. Noise Figure vs. Source Resistance

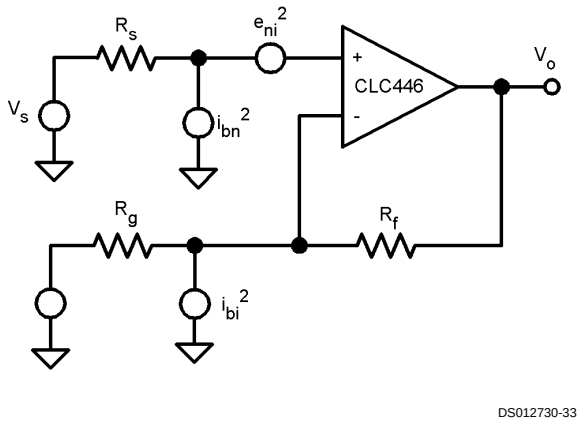


FIGURE 9. Noise Model

The CLC446 noise model in *Figure 9* is used to develop this equation for NF:

$$NF = 10\log\left(\frac{\theta_{ni}^2 + (i_{on}R_s)^2 + 4\kappa TR_s + (i_{bi} \cdot R_f \,||\, R_g)^2 + 4\kappa T \cdot R_f \,||\, R_g}{4\kappa TR_s}\right)$$

where:

- R_s is the source resistance at the non-inverting input
- There is no matching resistor from the input to ground
- e_{ni}, i_{bn}, and i_{bi} are the voltage and current noise density terms (see the **Electrical Characteristics** section)
-

$$4kT = (16.0 \times 10^{-21}\text{J}) \cdot \left[\frac{T}{290°K}\right], \text{ T is in °K}$$

- R_f is the feedback resistor, and R_g is the gain-setting resistor

To achieve a low Noise Figure while matching the source, use a matching transformer or the **Low Noise Composite Amp With Input Matching** circuit found in the **CLC446 Applications** section.

Dynamic Range (distortion)

The distortion plots in the Typical Performance Characteristics section show distortion as a function of load resistance, frequency, and output amplitude. Distortion places an upper limit on the CLC446's dynamic range.

Realized output distortion is highly dependent upon the external circuit. Some of the common external circuit choices that can improve distortion are:

- Short and equal return paths from the load to the supplies
- De-coupling capacitors of the correct value
- Higher load resistance
- A lower ratio of the output voltage swing to power supply voltage

Printed Circuit Board Layout

High Frequency op amp performance is strongly dependent on proper layout, proper resistive termination and adequate power supply decoupling. The most important layout points to follow are:

- Use a ground plane
- Bypass power supply pins with:
- ceramic capacitors of about 0.1µF placed less than 0.1" (3mm) from the pin
- tantalum capacitors of about 6.8µF for large signal current swings or improved power supply noise rejection; we recommend a minimum of 2.2 µF for any circuit
- Minimize trace and lead lengths for components between the inverting and output pins
- Remove ground plane underneath the amplifier package and 0.1" (3mm) from all input/output pads
- For prototyping, use flush-mount printed circuit board pins; never use high profile DIP sockets

Evaluation Board

Separate evaluation boards are available for prototyping and measurements. Additional information is available in the evaluation board literature.

Low Noise Composite Amp With Input Matching

The composite amp shown in *Figure 10* eliminates the need for a matching resistor to ground at the input. By connecting two amplifiers in series, the first non-inverting and the second inverting, an overall inverting gain is realized. The feedback resistor (R_f) closes the loop, and generates a set input resistance (R_{in}) that can be matched to R_s. R_f generates less noise than a matching resistor to ground at the input.

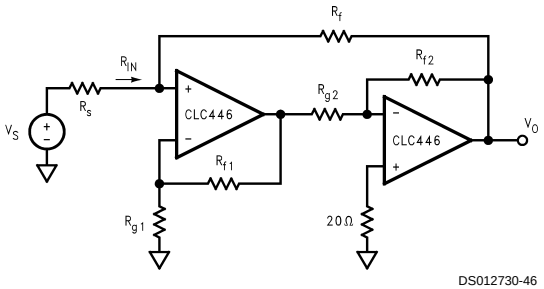


FIGURE 10. Composite Amplifier

The input resistance and DC voltage gain of the amplifier are:

Application Division (Continued)

$$R_{in} = \frac{R_f}{1+G}, \text{ where } G = \left[1 + \frac{R_{f1}}{R_{g1}}\right] \cdot \left[\frac{R_{f2}}{R_{g2}}\right]$$

$$\frac{V_o}{V_s} = -G \cdot \left[\frac{R_{in}}{R_{in} + R_s}\right]$$

Match the source resistance by setting: $R_{in}R = {}_s$.

The voltage noise produced by R_f, referred to the source V_s is:

$$e_{Rf}^2 = 4kTR_s \cdot \left[\frac{R_s}{R_{in} \cdot (1+G)}\right]$$

The noise of a simple input matching resistor connected to ground can be calculated by setting G to 0 in this equation. Thus, this circuit reduces the thermal noise power produced by the matching resistor by a factor of (1+G).

Rectifier Circuit

Wide bandwidth rectifier circuits have many applications. *Figure 11* shows a 200MHz wideband full-wave rectifier circuit using a CLC446 and a CLC522 amplifier. Schottky or PIN diodes are used for D_1 and D_2. They produce an active half-wave rectifier whose signals are taken at the feedback diode connection. The CLC522 takes the difference of the two half-wave rectified signals, producing a full-wave rectifier. The CLC522 is used at a gain of 5 to achieve high differential bandwidth. For best high frequency performance, maintain low parasitic capacitance from the diodes D_1 and D_2 to ground, and from the input of the CLC522 to ground.

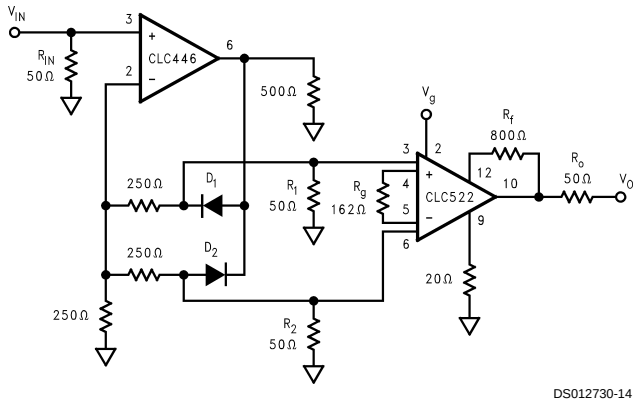


FIGURE 11. Full-Wave Rectifier

Elliptic Low-pass, Anti-aliasing Filter

Elliptic filters are often used in anti-aliasing applications. If there is noise or undesired signals at frequencies above 1/2 the sampling rate of an A/D converter, then these signals are aliased down into the operating frequency range, degrading the signal of interest. To filter out these undesired signal components, place a low pass filter in front of the A/D converter.

The **Typical Application** depicted on the front page is a 10MHz, third-order elliptic filter. It has a voltage-controlled, voltage source (VCVS) topology using a CLC446. To calculate the component values for this filter, do the following:

1. Select the filter approximation function for your application (see References). For this design we choose:

Filter type = Elliptic

Filter order (n) = 3

Passband ripple = 0.18dB

Minimum stopband attenuation (A_{min})= 37.44dB

Cutoff frequency = 10MHz (at 0.18dB attenuation)

These choices produce the following results:

-3dB frequency = 12.7MHz

Stopband corner frequency = 29.3MHz

2. Find the pole and zero locations. Reference gave the following for our filter:

Pole 1: $\alpha = 0.38621$

Pole 2: $\alpha_o = 0.88668$

Zero 1: $\beta = 1.13897$

Zero 2: $\omega_\infty = 3.3505$

3. Denormalize the frequency by multiplying by the cutoff frequency (ω_o) in radians/second. For our filter we have:

Cutoff frequency: $\omega_o = 2\pi(10\text{MHz}) = 62.832 \times 10^6$rad/s

Pole 1: $\alpha' = \omega_o\alpha = 24.266 \times 10^6$rad/s

Pole 2: $\alpha_o' = \omega_o\alpha_o = 55.712 \times 10^6$rad/s

Zero 1: $\beta' = \omega_o\beta = 21.052 \times 10^6$rad/s

Zero 2: $\omega_\infty' = \omega_o\omega_\infty = 71.564 \times 10^6$rad/s

4. Calculate these intermediate coefficients used in Reference [2].

$$c = \sqrt{(\alpha')^2 + (\beta')^2} \qquad a = \frac{2\alpha'}{c} \qquad b = \frac{\omega'_\infty}{c}$$

For this design, a = 0.64226, b = 7.7612 and c = 75.556 x 10^6.

5. Set the following resistance and capacitance scaling factors:

R = an arbitrary value

C = an arbitrary value

We chose C = 47pF and R = 1.00kΩ

6. Calculate the capacitor, resistor and gain (K) values using these equations:

$$C_1 = C$$

$$C_3 = C_4 = \frac{C}{2}$$

$$C_2 \geq \frac{C(b-1)}{4}$$

$$R_3 = \frac{1}{cC\sqrt{b}}$$

$$R_1 = R_2 = \frac{R_3}{2}$$

$$R_4 = \frac{4\sqrt{b}}{cC(1-b) + 4cC_2}$$

$$R_5 = R$$

$$C_5 = \frac{1}{R\alpha'_o}$$

$$K = 2 + \frac{2C_2}{C} - \frac{a}{2\sqrt{b}} + \frac{2}{C\sqrt{b}} \bullet \left(\frac{1}{cR_4} - aC_2\right)$$

Application Division (Continued)

For this design, the calculated values are:

C_1 = 47pF, C_2 = 91pF, C_3 = C_4 = 23.5pF,

C_5 = 17.95pF, R_1 = R_2 = 202.1Ω, R_3 = 101.1Ω,

R_4 = 3190Ω, R_5 = 1000Ω and K = 4.928.

7. Select the feedback resistor (R_f) and gain setting resistor (R_g values to obtain a non-inverting voltage gain of A_V = K. See the **DC Gain (non-inverting)** sub-section for details on selecting these values.

Figure 12 shows the ideal response of this filter. Some methods to bring actual performance closer to this ideal are:

- Compensate for op amp delay effects (pre-distortion)
- Adjust for parasitic capacitances in the layout
- Use components with small tolerances
- Add trim capacitors

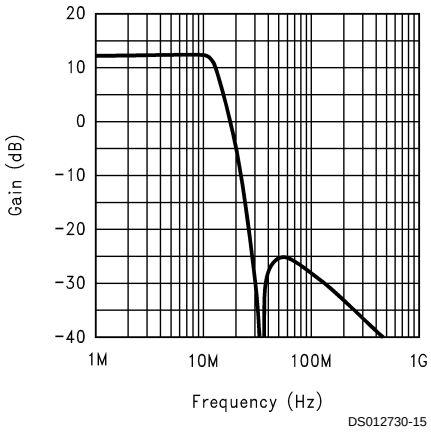


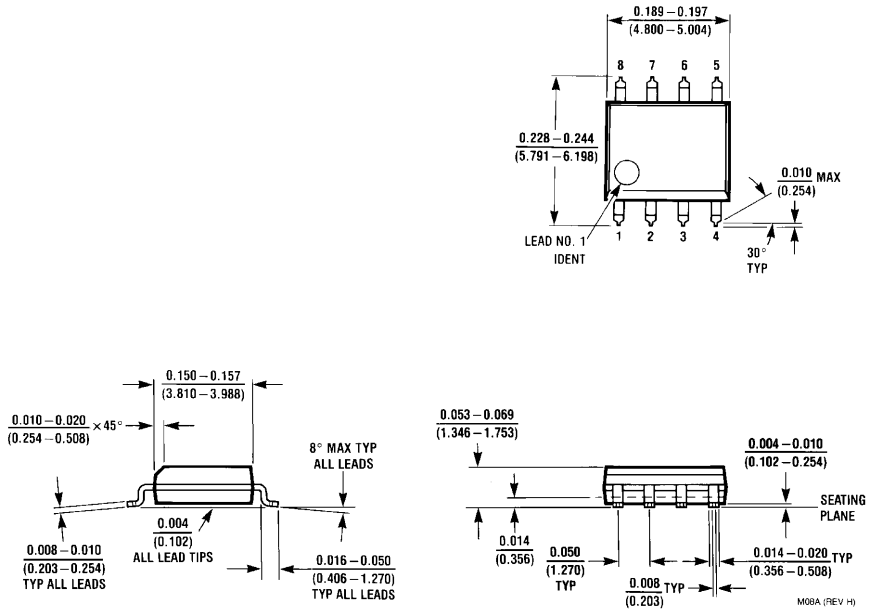
FIGURE 12. Ideal Elliptic Filter Frequency Response

References

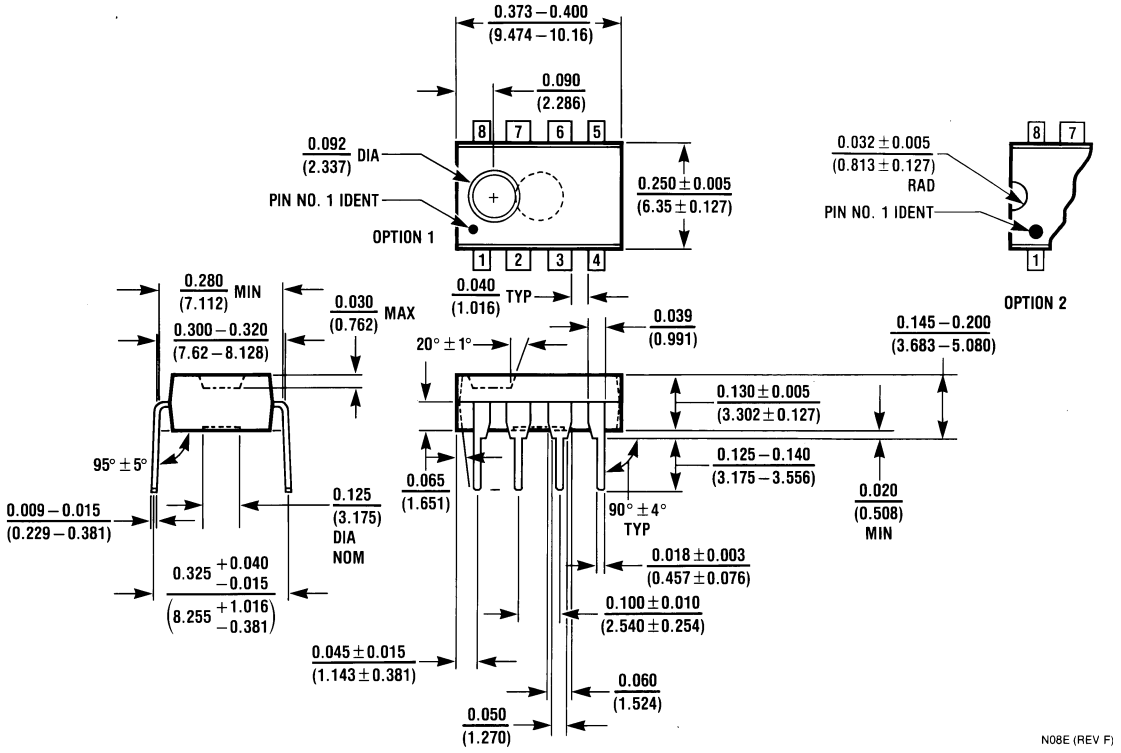
[1] Anatol I. Zverev, **Handbook of FILTER SYNTHESIS**, John Wiley & Sons 1967, p. 177

[2] Arthur B. Williams and Fred J. Taylor, **Electronic Filter Design Handbook**, McGraw Hill, 1995, pp. 3-29 to 3-31.

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin SOIC
NS Package Number M08A



8-Pin MDIP
NS Package Number N08E

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