53A, 100V, 0.028 Ohm, N-Channel UltraFET Power MOSFETs

These N-Channel power MOSFETs are manufactured using the innovative UltraFET™ process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA75639.

Ordering Information

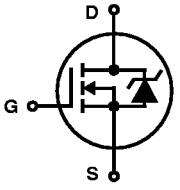
PART NUMBER	PACKAGE	BRAND
HUF75639G3	TO-247	75639G
HUF75639P3	TO-220AB	75639P
HUF75639S3	TO-262AA	75639S
HUF75639S3S	TO-263AB	75639S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUF75639S3ST.

Features

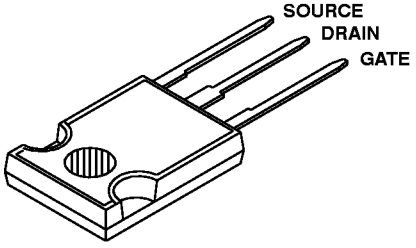
- 53A, 100V
- *Ultra Low On-Resistance*, $r_{DS(ON)} = 0.028\Omega$
- Diode Exhibits Both High Speed and Soft Recovery
- *Temperature Compensating* PSPICE Model
- *Thermal Impedance* SPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

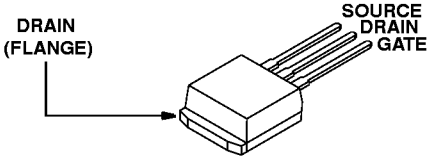


Packaging

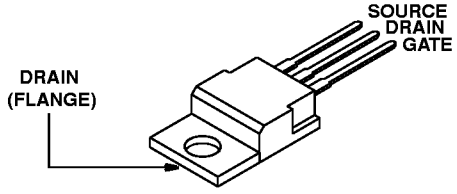
JEDEC STYLE TO-247



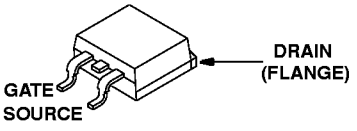
JEDEC TO-262AA



JEDEC TO-220AB



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

Drain to Source Voltage (Note1)	V_{DSS}	100	V
Drain to Gate Voltage (R_{GS} = 20KΩ) (Note 1)	V_{DGR}	100	V
Gate to Source Voltage	V_{GS}	20	V
Drain Current			
Continuous (Figure 2)	I_D	53	A
Pulsed Drain Current	I_{DM}	Figure 5	
Pulsed Avalanche Rating	E_{AS}	Figures 6, 14, 15	
Power Dissipation	P_D	200	W
Derate Above 25^oC		1.33	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure11)		100	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA (Figure10)		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 90V, V_{GS} = 0V		-	-	1	μA
		V_{DS} = 80V, V_{GS} = 0V, $T_C = 150^oC$		-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = 20V		-	-	±100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 53A, V_{GS} = 10V (Figure 9)		-	0.023	0.028	Ω
Turn-On Time	t_{ON}	V_{DD} = 50V, $I_D \cong 53$, R_L = 0 .943Ω, V_{GS} = 10V, R_{GS} = 5.1Ω		-	-	110	ns
Turn-On Delay Time	$t_{d(ON)}$			-	15	-	ns
Rise Time	t_r			-	60	-	ns
Turn-Off Delay Time	$t_{d(off)}$			-	20	-	ns
Fall Time	t_f			-	25	-	ns
Turn-Off Time	t_{OFF}			-	-	70	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 20V	V_{DD} = 50V, $I_D \cong 53A$, R_L =0 .943Ω $I_{g(REF)}$ = 1.0mA (Figures 13, 16, 17)	-	110	130	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V		-	57	75	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 2V		-	3.7	4.5	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure12)		-	2000	-	pF
Output Capacitance	C_{OSS}			-	500	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	65	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	0.75	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-247		-	-	30	$^oC/W$
		TO-220, TO-262, and TO-263		-	-	62	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 53A	-	-	1.25	V
Reverse Recovery Time	t_{rr}	I_{SD} = 53A, dI_{SD}/dt = 100A/μs	-	-	110	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 53A, dI_{SD}/dt = 100A/μs	-	-	320	nC

Typical Performance Curves

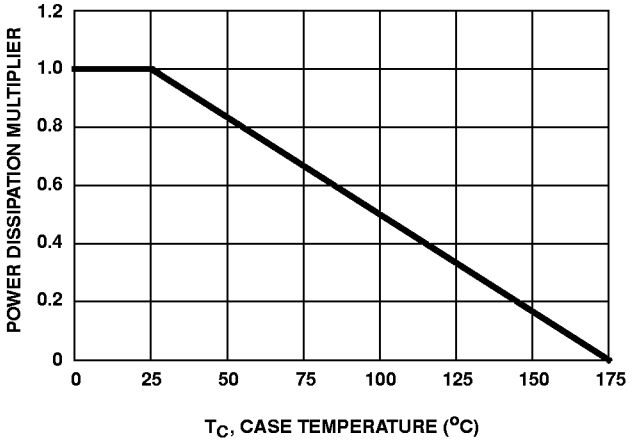


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

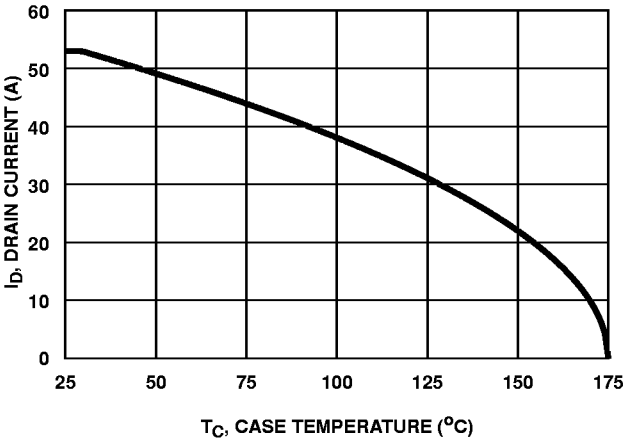


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

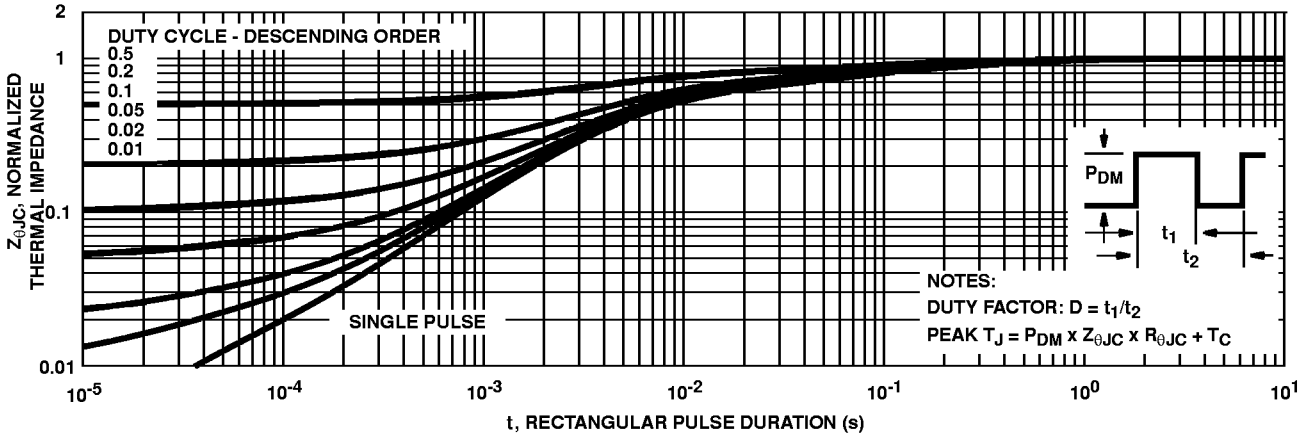


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

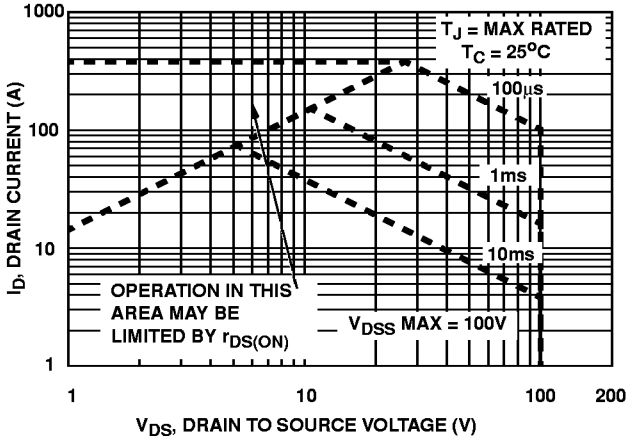


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

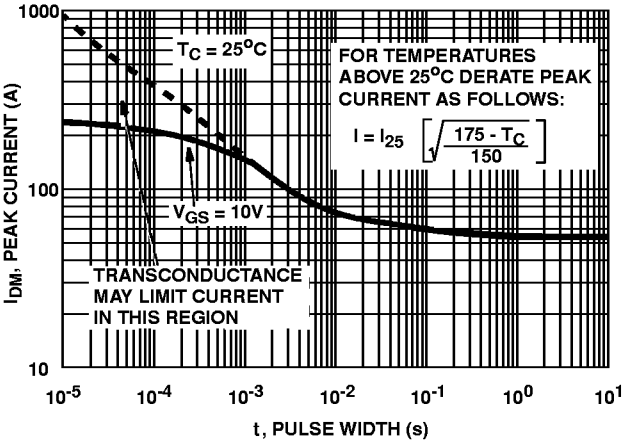
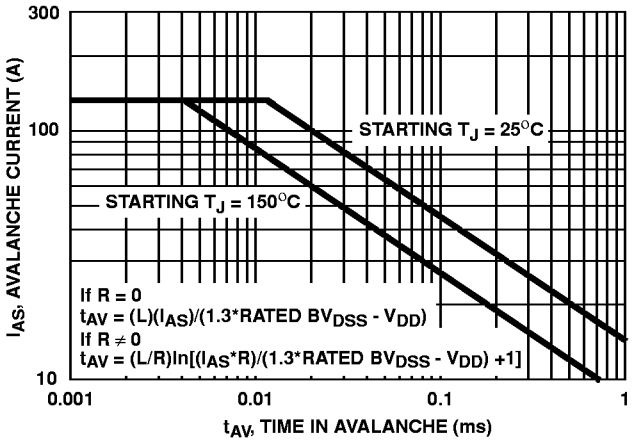


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)



NOTE: Refer to Harris Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

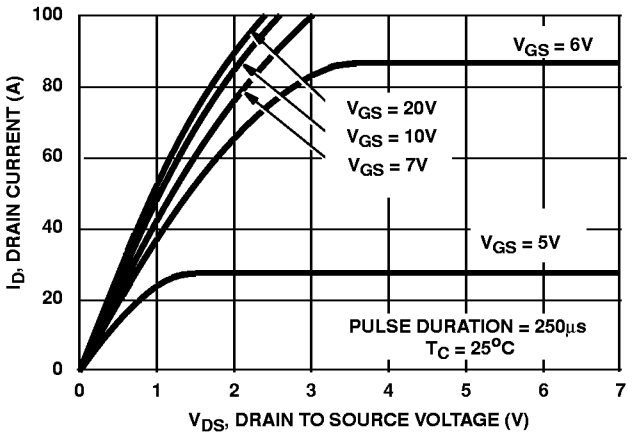


FIGURE 7. SATURATION CHARACTERISTICS

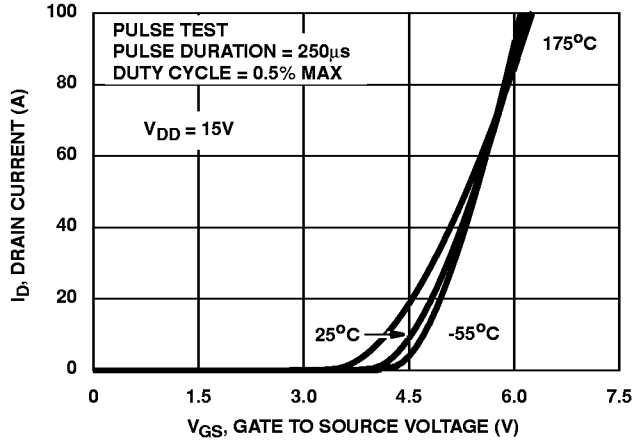


FIGURE 8. TRANSFER CHARACTERISTICS

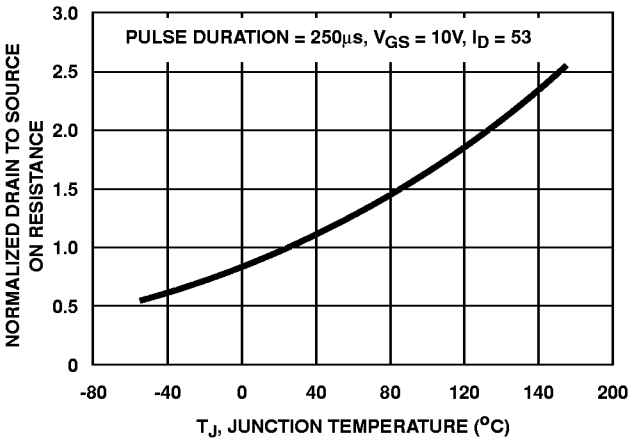


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

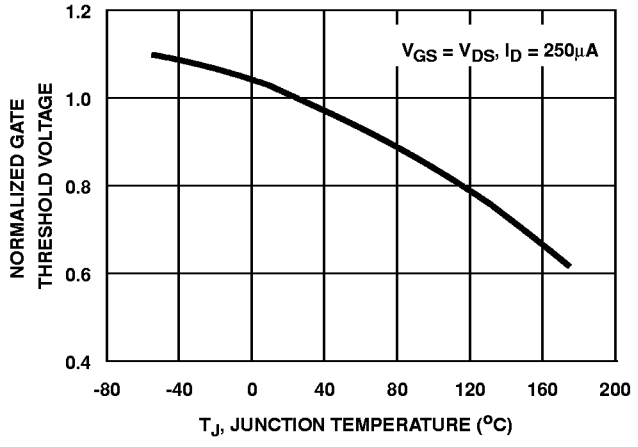


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

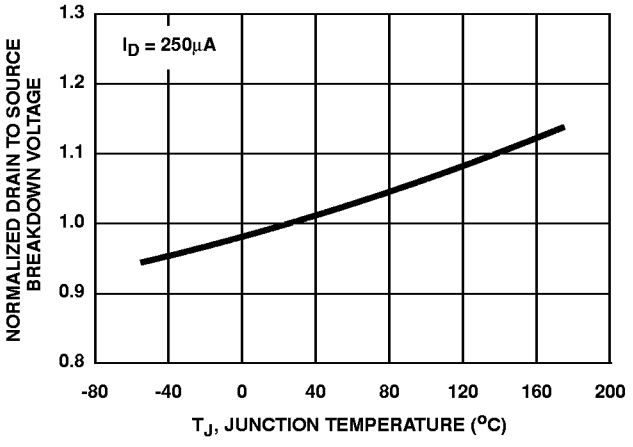


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

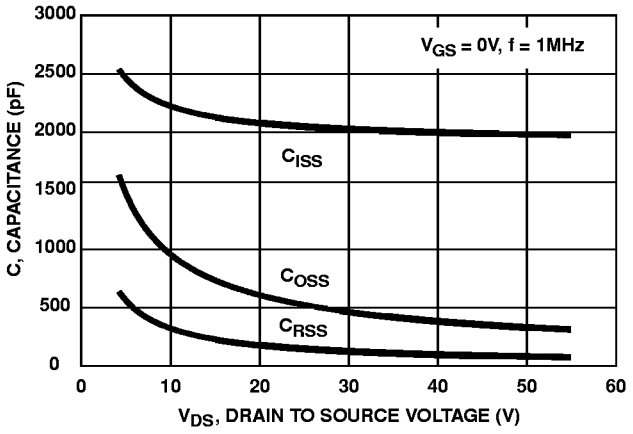
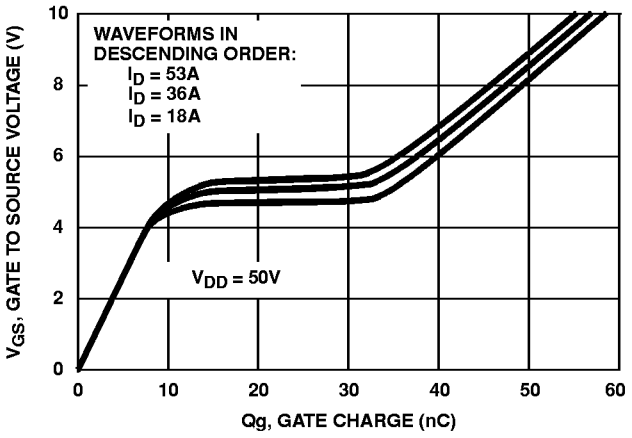


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

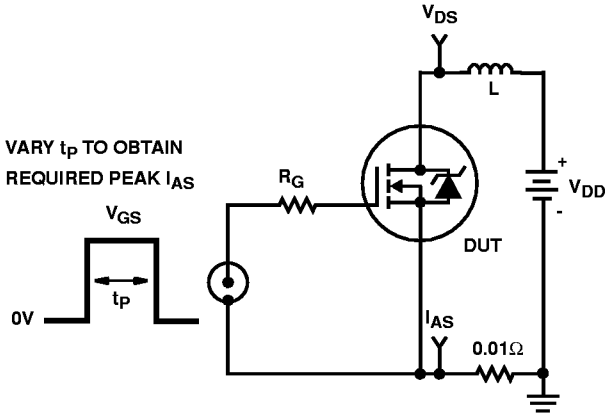


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

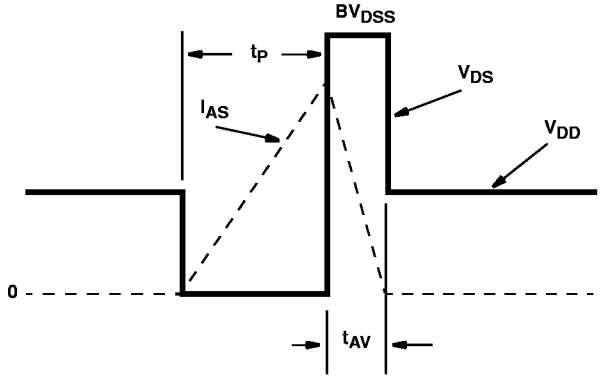


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

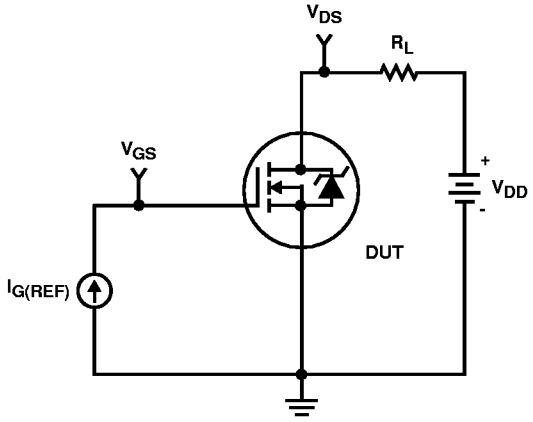


FIGURE 16. GATE CHARGE TEST CIRCUIT

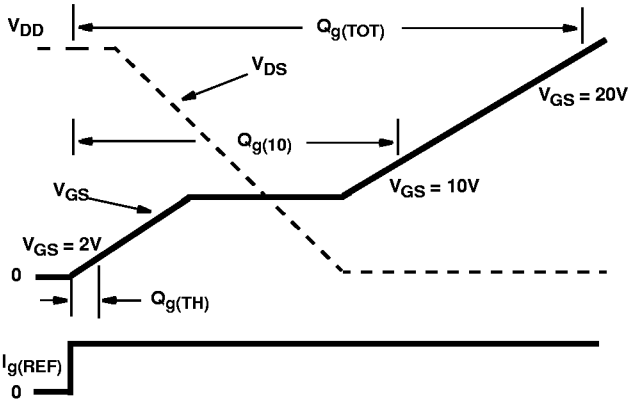


FIGURE 17. GATE CHARGE WAVEFORMS

Test Circuits and Waveforms (Continued)

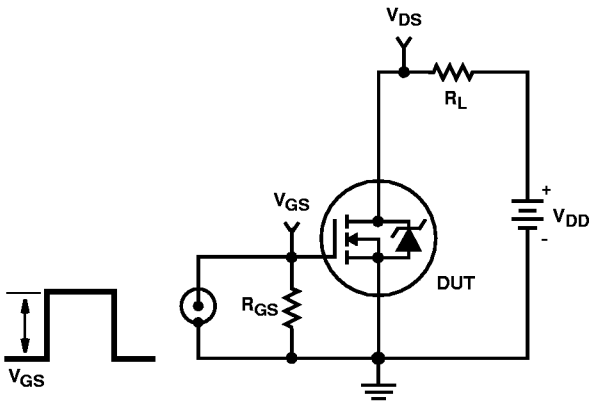


FIGURE 18. SWITCHING TIME TEST CIRCUIT

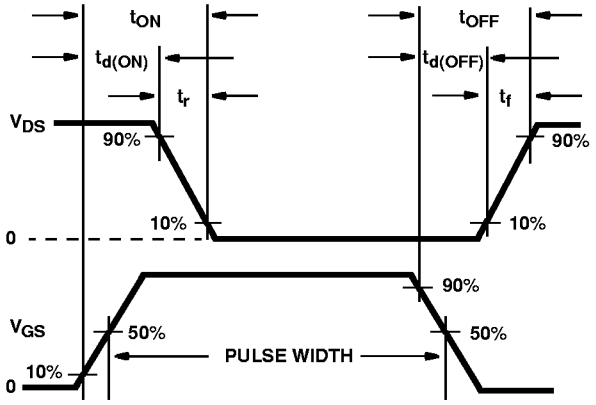
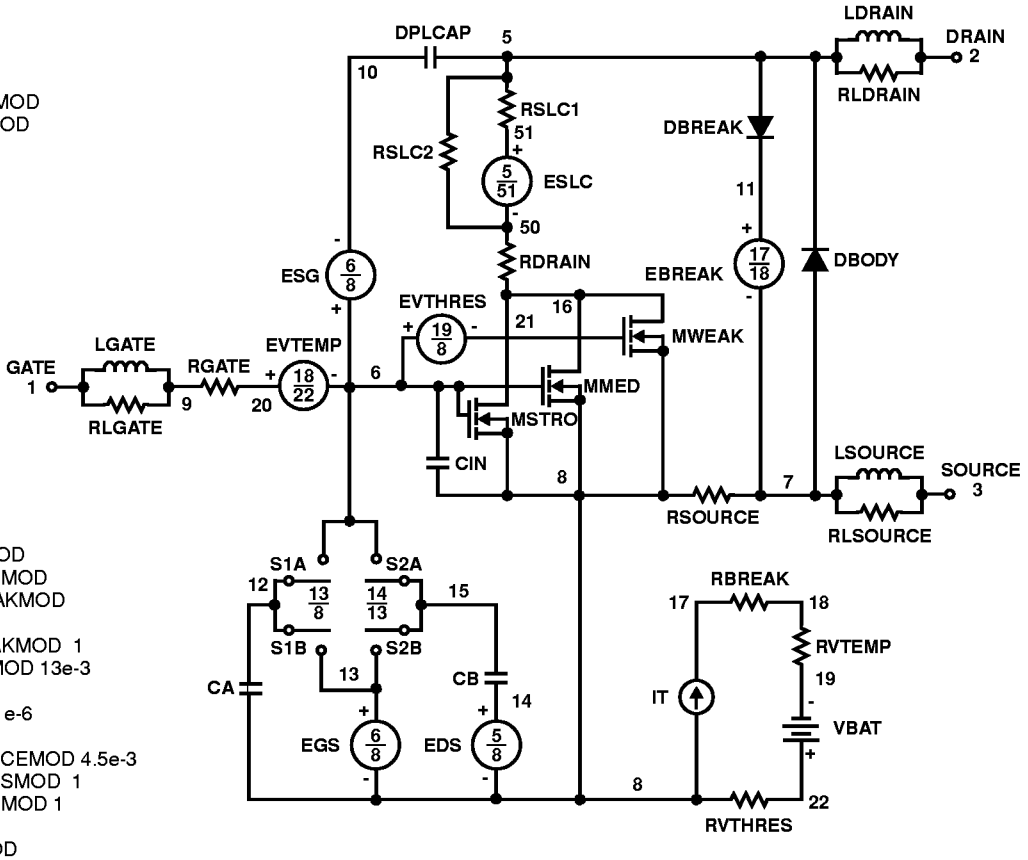


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

PSPICE Electrical Model

```
SUBCKT HUF75639 2 1 3 ;       rev OCT98
CA  12  8 28.5e-10
CB  15  14 26.5e-10
CIN  6  8 19e-10

DBODY 7 5 DBODYMOD
DBREAK 5 11  DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17  18 110
EDS  14  8  5  8 1
EGS  13  8  6  8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8  1
EVTEMP 20 6 18 22 1

IT  8  17  1

LDRAIN 2 5 2e-9
LGATE 1  9 1e-9
LSOURCE  3  7 4.69e-10

RLGATE 1 9 10
RLDRAIN 2 5 20
RLSOURCE 3 7 4.69

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK  17  18  RBREAKMOD  1
RDRAIN 50 16 RDRAINMOD 13e-3
RGATE  9  20 .7
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE  8  7  RSOURCEMOD 4.5e-3
RVTHRES 22 8 RVTHRESMOD  1
RVTEMP 18 19 RVTEMPMOD 1

S1A  6  12  13  8  S1AMOD
S1B  13  12  13  8  S1BMOD
S2A  6  15  14  13  S2AMOD
S2B  13  15  14  13  S2BMOD

VBAT 22 19  DC  1

ESLC 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*115),4))}

.MODEL DBODYMOD D (IS = 1.4e-12  RS = 3.3e-3 XTI=4.7  TRS1 = 2e-3  TRS2 = .1e-5  CJO = 27e-10  TT = 6.1e-8 M = 0.6 )
.MODEL DBREAKMOD D (RS = 3.5e-1  TRS1 = 1e-3  TRS2 = 1e-6)
.MODEL DPLCAPMOD D (CJO = 28.5e-10  IS = 1e-30  N = 10 M = .95 vj=1.0)
.MODEL MMEDMOD NMOS (VTO = 3.5 KP = 4.8 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u Rg=.7)
.MODEL MSTROMOD NMOS (VTO = 3.97 KP = 56.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO =3.11 KP = 0.085 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG=7 RS=.1)
.MODEL RBREAKMOD RES (TC1 = .8e-3  TC2 = 1e-6)
.MODEL RDRAINMOD RES (TC1 = 1e-2  TC2 = 1.75e-5)
.MODEL RSLCMOD RES (TC1 = 2.8e-3 TC2 = 14e-6)
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RVTHRESMOD RES (TC = -2.e-3 TC2 = -1.75e-5)
.MODEL RVTEMPMOD RES (TC1 = -2.75e-3  TC2 = .05e-9)

.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -6.0  VOFF = -3.5)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -3.5  VOFF = -6.0)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -2.5  VOFF = 4.95)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 4.95  VOFF = -2.5)

.ENDS
```



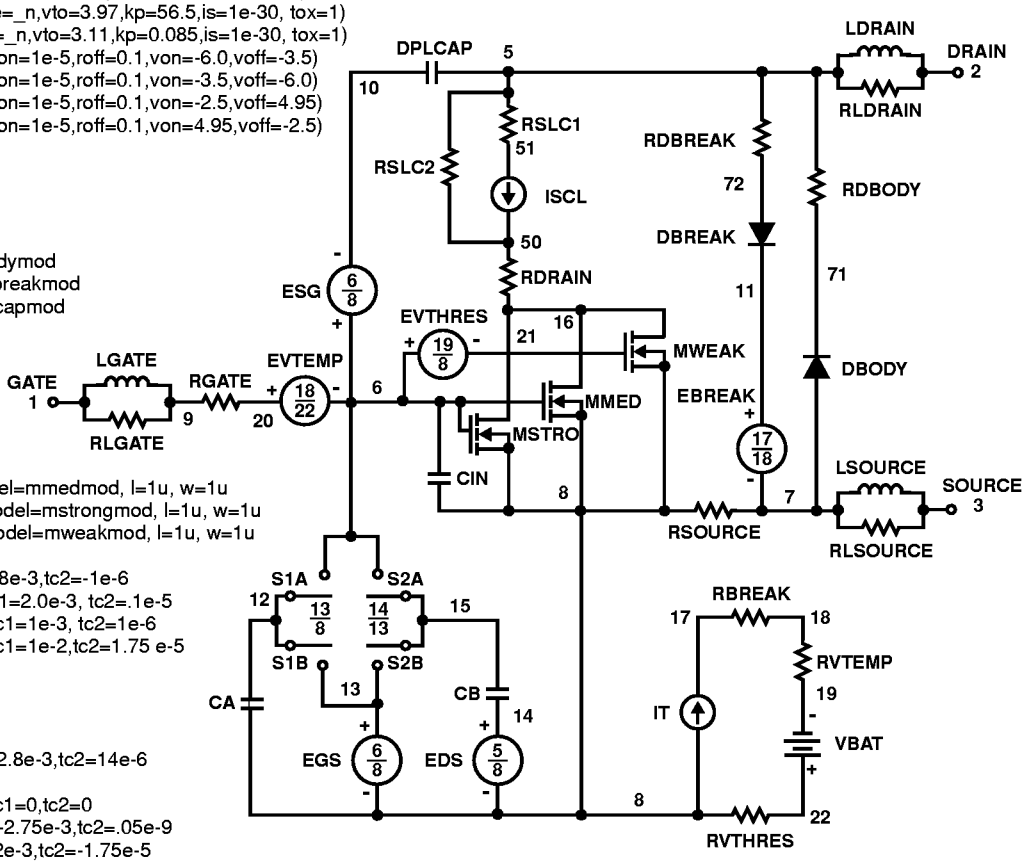
NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

nom temp=25 deg c 100v Ultrafet

REV Oct 1998

```
template huf75639 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
d..model dbodymod = (is=1.4e-12, xti=4.7, cjo=27e-10,tt=6.1e-8, m=0.6)
d..model dbreakmod = ()
d..model dplcapmod = (cjo=28.5e-10,is=1e-30,n=10,m=0.95, vj=1.0)
m..model mmedmod = (type=_n,vto=3.5,kp=4.8,is=1e-30, tox=1)
m..model mstrongmod = (type=_n,vto=3.97,kp=56.5,is=1e-30, tox=1)
m..model mweakmod = (type=_n,vto=3.11,kp=0.085,is=1e-30, tox=1)
sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-6.0,voff=-3.5)
sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-3.5,voff=-6.0)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-2.5,voff=4.95)
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=4.95,voff=-2.5)

c.ca n12 n8 = 28.5e-10
c.cb n15 n14 = 26.5e-10
c.cin n6 n8 = 19e-10

d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 2.0e-9
l.lgate n1 n9 = 1e-9
l.lsource n3 n7 = 4.69e-10

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1=.8e-3,tc2=-1e-6
res.rdbody n71 n5 =3.3e-3, tc1=2.0e-3, tc2=.1e-5
res.rdbreak n72 n5 =3.5e-1, tc1=1e-3, tc2=1e-6
res.rdrain n50 n16 = 13e-3, tc1=1e-2,tc2=1.75 e-5
res.rgate n9 n20 = .7
res.rldrain n2 n5 = 20
res.rlgate n1 n9 = 10
res.rlsource n3 n7 = 4.69
res.rslc1 n5 n51 = 1e-6, tc1=2.8e-3,tc2=14e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 4.5e-3, tc1=0,tc2=0
res.rvtemp n18 n19 = 1, tc1=-2.75e-3,tc2=.05e-9
res.rvthres n22 n8 = 1, tc1=-2e-3,tc2=-1.75e-5

spe.ebreak n11 n7 n17 n18 = 110
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/115))** 4))
}
}
```



SPICE Thermal Model

REV APRIL 1998

HUF75639

CTHERM1 TH 6 6 5.0
CTHERM2 6 5 3.0e-2
CTHERM3 5 4 1.0e-2
CTHERM4 4 3 3.0e-2
CTHERM5 3 2 3.5e-2
CTHERM6 2 TL 1.0

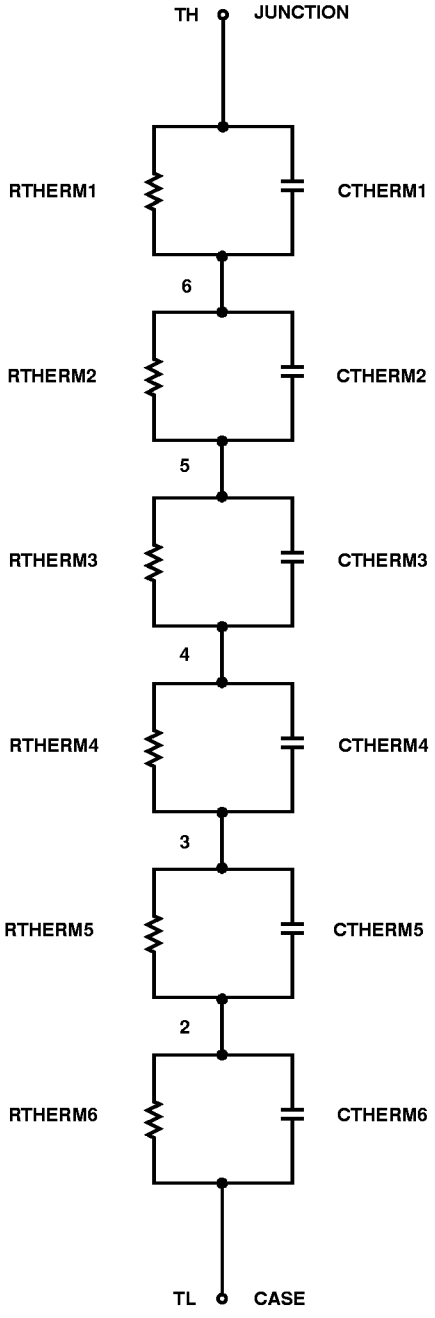
RTHERM1 TH 6 2.5e-4
RTHERM2 6 5 5.0e-4
RTHERM3 5 4 2.8e-3
RTHERM4 4 3 8.8e-2
RTHERM5 3 2 1.8e-1
RTHERM6 2 TL 5.0e-2

SABER Thermal Model

SABER thermal model HUF75639

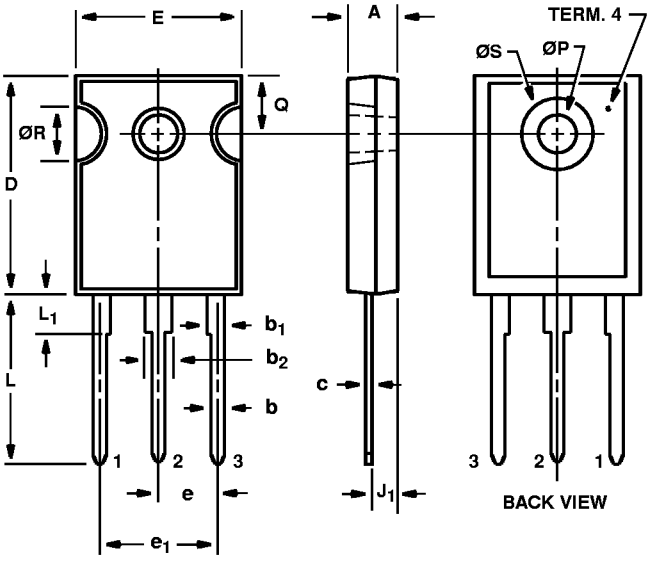
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 = 500e-2
ctherm.ctherm2 6 5 = 3.0e-2
ctherm.ctherm3 5 4 = 1.0e-2
ctherm.ctherm4 4 3 = 3.0e-2
ctherm.ctherm5 3 2 = .35e-1
ctherm.ctherm6 2 tl = 1.0

rtherm.rtherm1 th 6 = 2.5e-4
rtherm.rtherm2 6 5 = 5.0e-4
rtherm.rtherm3 5 4 = 2.8e-3
rtherm.rtherm4 4 3 = 88e-3
rtherm.rtherm5 3 2 = 18.0e-2
rtherm.rtherm6 2 tl = .5e-1
}



TO-247

3 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE



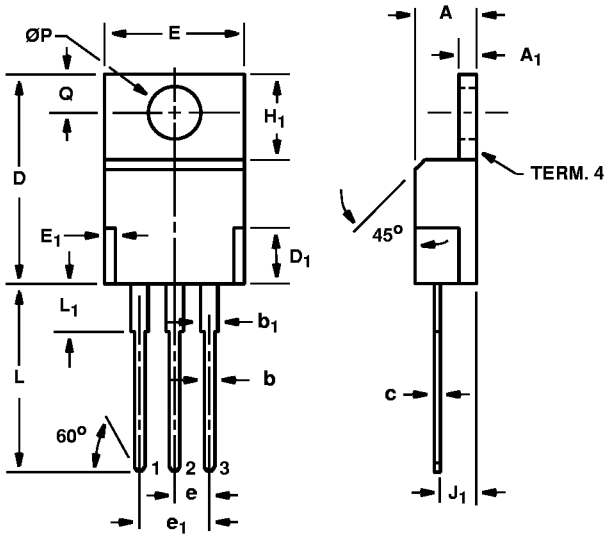
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b_1	0.060	0.070	1.53	1.77	1, 2
b_2	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.219 TYP		5.56 TYP		4
e_1	0.438 BSC		11.12 BSC		4
J_1	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L_1	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L_1.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

TO-220AB

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE

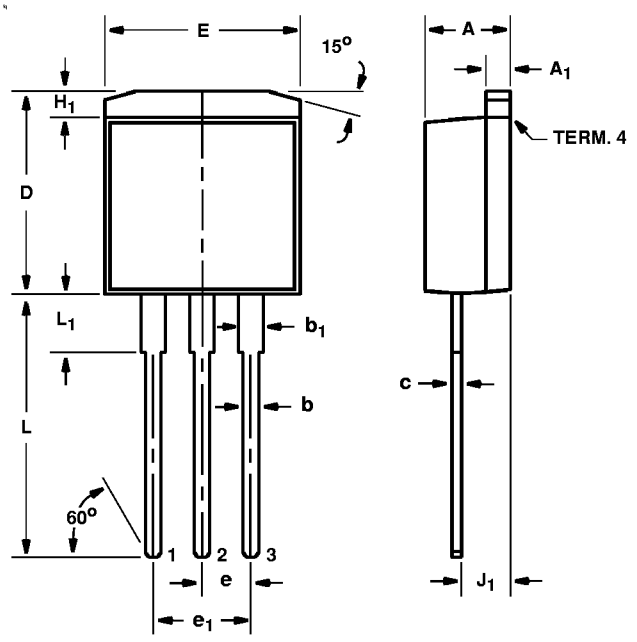


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D_1	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E_1	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L_1	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L_1.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 7-97.

TO-262AA 3 LEAD JEDEC TO-262AA PLASTIC PACKAGE

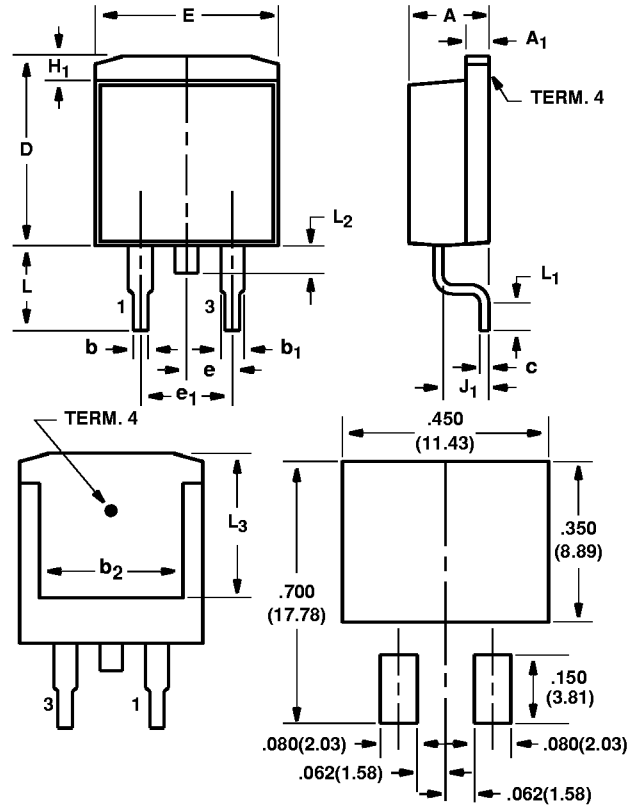


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	3, 4
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.045	0.055	1.15	1.39	-
J_1	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L_1	0.110	0.130	2.80	3.30	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC TO-262AA outline dated 6-90.
2. Solder finish uncontrolled in this area.
3. Dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 5 dated 7-97.

TO-263AB SURFACE MOUNT JEDEC TO-263AB PLASTIC PACKAGE



MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

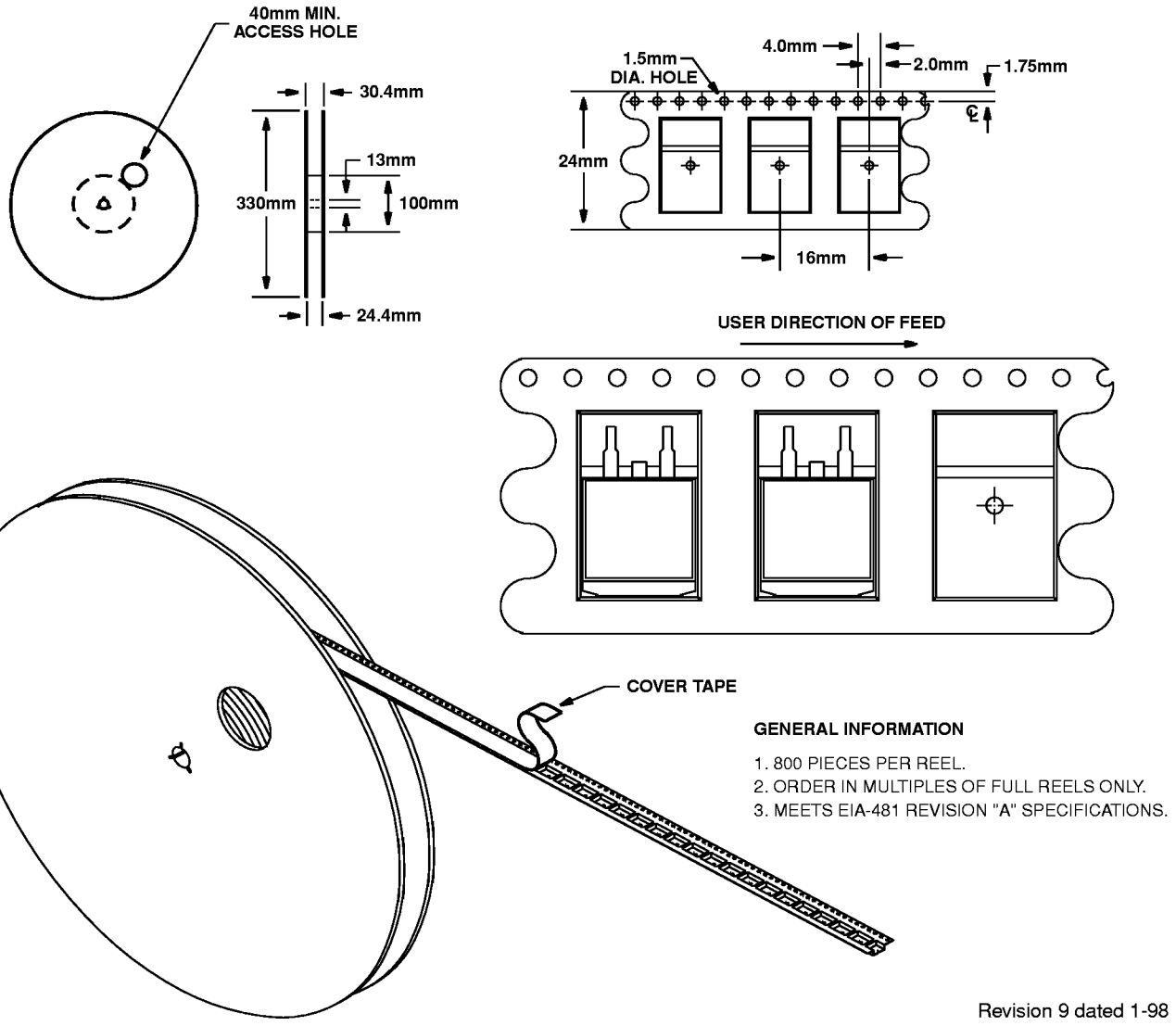
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	4, 5
b	0.030	0.034	0.77	0.86	4, 5
b_1	0.045	0.055	1.15	1.39	4, 5
b_2	0.310	-	7.88	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		7
e_1	0.200 BSC		5.08 BSC		7
H_1	0.045	0.055	1.15	1.39	-
J_1	0.095	0.105	2.42	2.66	-
L	0.175	0.195	4.45	4.95	-
L_1	0.090	0.110	2.29	2.79	4, 6
L_2	0.050	0.070	1.27	1.77	3
L_3	0.315	-	8.01	-	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
2. L_3 and b_2 dimensions established a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L_1 is the terminal length for soldering.
7. Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 9 dated 1-98.

TO-263AB

24mm TAPE AND REEL



GENERAL INFORMATION

1. 800 PIECES PER REEL.
2. ORDER IN MULTIPLES OF FULL REELS ONLY.
3. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revision 9 dated 1-98

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