19-1116; Rev 1; 11/96

MAXIM

Microprocessor-Compatible, 14-Bit DACs

General Description

The MX7534/MX7535 are high-performance, CMOS, monolithic, 14-bit digital-to-analog converters (DACs). Wafer-level, laser-trimmed, thin-film resistors and temperature-compensated NMOS switches assure operation over the full operating temperature range with exceptional linear and gain stability.

The MX7534 accepts right-justified data in two bytes from an 8-bit bus, while the MX7535 operates with a 14-bit data bus with separate MS-byte and LS-byte select controls. In addition, all digital inputs are compatible with both TTL and 5V CMOS-logic levels. The MX7534/MX7535 are intended for unipolar operation, but may be operated as bipolar DACs with additional external components. Both devices are protected against CMOS latchup, and neither requires the use of external Schottky protection diodes.

The MX7534 is available in 20-pin narrow (0.3") DIP, wide SO, or PLCC packages. The MX7535 is available in 28-pin, 600 mil wide DIP, wide SO, or PLCC packages.

Applications

Machine and Motion Control Systems
Automatic Test Equipment
Digital Audio
µP-Controlled Calibration Circuitry
Programmable-Gain Amplifiers
Digitally Controlled Filters
Programmable Power Supplies

Features

- ♦ **14-Bit Monotonic Over Full Temperature Range**
- ♦ **Full 4-Quadrant Multiplication**
- ♦ **µP-Compatible, Double-Buffered Inputs**
- ♦ **Exceptionally Low Gain Tempco (2.5ppm/°C)**
- ♦ **Low Output Leakage (<20nA) Over Temp.**
- ♦ **Low Power Consumption**
- ♦ **TTL and CMOS Compatible**

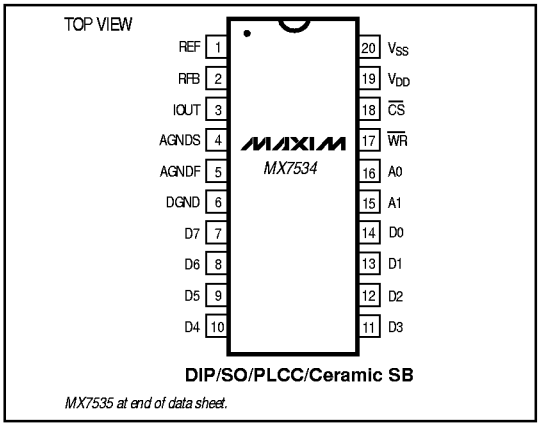
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MX7534KN	0°C to +70°C	20 Plastic DIP	±1
MX7534JN	0°C to +70°C	20 Plastic DIP	±2
MX7534KCWP	0°C to +70°C	20 SO	±1
MX7534JCWP	0°C to +70°C	20 SO	±2
MX7534KP	0°C to +70°C	20 PLCC	±1
MX7534JP	0°C to +70°C	20 PLCC	±2
MX7534J/D	0°C to +70°C	Dice*	±2
MX7534BQ	-25°C to +85°C	20 CERDIP	±1
MX7534AQ	-25°C to +85°C	20 CERDIP	±2
MX7534BD	-25°C to +85°C	20 Ceramic SB	±1
MX7534AD	-25°C to +85°C	20 Ceramic SB	±2
MX7534KEWP	-40°C to +85°C	20 SO	±1
MX7534JEWP	-40°C to +85°C	20 SO	±2
MX7534TQ	-55°C to +125°C	20 CERDIP	±1
MX7534SQ	-55°C to +125°C	20 CERDIP	±2
MX7534TD	-55°C to +125°C	20 Ceramic SB	±1
MX7534SD	-55°C to +125°C	20 Ceramic SB	±2

Ordering Information continued at end of data sheet.

**Dice are tested at +25°C, DC parameters only.*

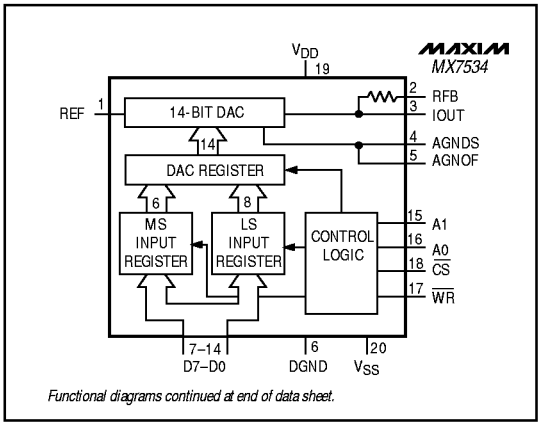
Pin Configurations



DIP/SO/PLCC/Ceramic SB

MX7535 at end of data sheet.

Functional Diagrams



Functional diagrams continued at end of data sheet.

Microprocessor-Compatible, 14-Bit DACs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND .....-0.3V, +17V
V_{SS} to AGND .....-15V, +0.3V
REF to AGND (MX7534) .....±25V
REFS to AGND (MX7535) .....±25V
REFF to AGND (MX7535) .....±25V
RFB to AGND.....±25V
Digital Input Voltage to DGND.....-0.3V, V_{DD} + 0.3V
IOUT to DGND.....-0.3V, V_{DD} + 0.3V
AGND to DGND.....-0.3V, V_{DD} + 0.3V
Continuous Power Dissipation (T_A = +70°C)
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C)....889mW
28-Pin Plastic DIP (derate 14.29mW/°C above +70°C).....1.14W
20-Pin SO (derate 10.00mW/°C above +70°C).....800mW
28-Pin SO (derate 12.50mW/°C above +70°C).....1W
20-Pin PLCC (derate 10.00mW/°C above +70°C) 800mW
28-Pin PLCC (derate 10.53mW/°C above +70°C) 842mW
20-Pin CERDIP (derate 11.11mW/°C above +70°C).....889mW
28-Pin CERDIP (derate 16.67mW/°C above +70°C).....1.33W
20-Pin Ceramic SB
(derate 11.76mW/°C above +70°C) 941mW
28-Pin Ceramic SB
(derate 20.00mW/°C above +70°C).....1.6W
Operating Temperature Ranges
MX753_J/K.....0°C to +70°C
MX753_A/B .....-25°C to +85°C
MX753_EW_.....-40°C to +85°C
MX753_S/T.....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +11.4V to +15.75V (Note 1), V_{REF} = 10V, V_{IOUT} = V_{AGNDS} = V_{SS} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
DC ACCURACY								
Resolution					14			Bits
Relative Accuracy	INL	MX753_K/B/T					±1	LSB
		MX753_J/A/S					±2	
Differential Nonlinearity		Guaranteed Monotonic					±1	LSB
Full-Scale Error		Measured with internal R_{FB}, includes effects of leakage current and gain TC		MX753_K/B/T			±4	LSB
				MX753_J/A/S			±8	
Gain Temperature Coefficient (Note 2)		MX753_K/B/T				±0.5	±2.5	ppm/°C
		MX753_J/A/S				±0.5	±5	
Output Leakage Current	I_{OUT}	All digital inputs at 0V	T_A = +25°C				±5	nA
		All digital inputs at 0V, V_{SS} = 0V	T_A = T_{MIN} to T_{MAX}	MX753_J/K/A/B			±25	
				MX753_S/T			±150	
REFERENCE INPUT								
Reference Voltage Input Resistance (Note 3)	R_{REF}				3.5	6	10	kΩ
DIGITAL INPUTS								
Input High Voltage	V_{INH}				2.4			V
Input Low Voltage	V_{INL}						0.8	V
Input Leakage Current		Digital inputs at 0V or V_{DD}	T_A = +25°C				±1	µA
			T_A = T_{MIN} to T_{MAX}				±10	
Input Capacitance (Note 2)	C_{IN}						7	pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +11.4V to +15.75V (Note 1), V_{REF} = 10V, V_{IOUT} = V_{AGNDS} = V_{SS} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Positive Supply-Voltage Range	V_{DD}	For specific performance		11.4		15.75	V
Negative Supply-Voltage Range	V_{SS}	For specific performance		-200		-500	mV
Positive Supply Current	I_{DD}	Digital inputs at V_{INH} or V_{INL}	MX7534			3	mA
			MX7535			4	
Negative Supply Current	I_{SS}	Digital inputs at 0V or V_{DD}				500	µA

Note 1: Specifications are guaranteed for V_{DD} of +11.4V to +15.75V. At V_{DD} = +5V, device is still functional with degraded specifications.
Note 2: Guaranteed by design, not tested.
Note 3: Resistors have a typical -300ppm/°C tempco.

AC PERFORMANCE CHARACTERISTICS (Note 4)

(V_{DD} = +11.4V to +15.75V, V_{REF} = 10V, V_{IOUT} = V_{AGND} (V_{AGNDS} for MX7535) = V_{SS} = 0V, output amplifier is AD544*, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Current Setting Time		T_A = +25°C, to 0.003% of full-scale range, IOUT load = 100Ω || 13pF, DAC register alternately loaded with all 1s and all 0s			0.8	1.5	µs
Digital-to-Analog Glitch Impulse		Measured with V_{REF} = 0V, IOUT loads = 100Ω || 13pF, DAC register alternately loaded with all 1s and all 0s			50		nV-sec
Multiplying Feedthrough Error (Note 5)		V_{REF} = ±10V, 10kHz sine wave, DAC register loaded with all 0s	T_A = +25°C		3		mVp-p
			T_A = T_{MIN} to T_{MAX}		5		
Power-Supply Rejection		ΔV_{DD} = ±5%	T_A = +25°C			±0.01	%/%
			T_A = T_{MIN} to T_{MAX}			±0.02	
Output Capacitance (IOUT Pin)	C_{OUT}	DAC register loaded with all 1s				260	pF
		DAC register loaded with all 0s				130	
Output Noise Voltage Density (10Hz–100kHz)		Measured between R_{FB} and I_{OUT}			15		nV/Hz

Note 4: These characteristics are included for design guidance only, and are not subject to test.
Note 5: Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

* AD544 is an Analog Devices part.

TIMING CHARACTERISTICS (MX7534)

(V_{DD} = +11.4V to +15.75V, V_{REF} = 10V, V_{IOUT} = V_{AGND} = V_{SS} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. See Figure 1a for timing diagram.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Address Valid to Write Setup Time	t_1		0			ns
Address Valid to Write Hold Time	t_2		0			ns
Data Setup Time	t_3	T_A = +25°C	60			ns
		T_A = -25°C to +85°C	70			
		T_A = -55°C to +125°C	80			
Data Hold Time	t_4	T_A = +25°C	20			ns
		T_A = -25°C to +85°C	20			
		T_A = -55°C to +125°C	30			
Chip-Select to Write-Setup Time	t_5		0			ns
Chip-Select to Write-Hold Time	t_6		0			ns
Write Pulse Width	t_7	T_A = +25°C	170			ns
		T_A = -25°C to +85°C	200			
		T_A = -55°C to +125°C	240			

TIMING CHARACTERISTICS (MX7535)

(V_{DD} = +11.4V to +15.75V, V_{REF} = 10V, V_{IOUT} = V_{AGNDS} = V_{SS} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. See Figure 1b for timing diagram.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup Time	t_1		0			ns
$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold Time	t_2		0			ns
$\overline{LDAC}$ Pulse Width	t_3	T_A = +25°C	170			ns
		T_A = -25°C to +85°C	200			
		T_A = -55°C to +125°C	240			
Write Pulse Width	t_4	T_A = +25°C	170			ns
		T_A = -25°C to +85°C	200			
		T_A = -55°C to +125°C	240			
Data-Setup Time	t_5	T_A = +25°C	140			ns
		T_A = -25°C to +85°C	160			
		T_A = -55°C to +125°C	180			
Data-Hold Time	t_6	T_A = +25°C	20			ns
		T_A = -25°C to +85°C	20			
		T_A = -55°C to +125°C	30			

Pin Description (MX7534)

PIN	NAME	FUNCTION
1	REF	Reference Input to DAC
2	RFB	Feedback Resistor. Used to close the loop around an external op amp.
3	IOUT	Current Output
4	AGNDS	Analog Ground Sense. Reference point for external circuitry. AGNDS should carry minimum current.
5	AGNDF	Analog Ground Force. Carries current from internal analog ground connections. AGNDS and AGNDF are tied together internally.
6	DGND	Digital Ground
7	D7	Data Bit 7
8	D6	Data Bit 6
9	D5	Data Bit 5 or Data Bit 13 (MSB)
10	D4	Data Bit 4 or Data Bit 12
11	D3	Data Bit 3 or Data Bit 11
12	D2	Data Bit 2 or Data Bit 10
13	D1	Data Bit 1 or Data Bit 9
14	D0	Data Bit 0 (LSB) or Data Bit 8
15	A1	Address Input 1
16	A0	Address Input 0
17	$\overline{WR}$	Write Input. Active low.
18	$\overline{CS}$	Chip-Select Input. Active low.
19	V_{DD}	+12V to +15V Supply-Voltage Input
20	V_{SS}	Bias pin for high-temperature, low-leakage configuration

Pin Description (MX7535)

PIN	NAME	FUNCTION
1	REFS	Reference Voltage Sense
2	REFF	Reference Voltage Force
3	RFB	Feedback Resistor. Used to close the loop around an external op amp.
4	IOUT	Current Output
5	AGNDS	Analog Ground Sense. Reference point for external circuitry. This pin should carry minimum current.
6	AGNDF	Analog Ground Force. Carries current from internal analog ground connections. AGNDS and AGNDF are tied together internally.
7	DGND	Digital Ground
8	D13	Data Bit 13 (MSB)
9	D12	Data Bit 12
10	D11	Data Bit 11
11	D10	Data Bit 10
12	D9	Data Bit 9
13	D8	Data Bit 8
14	D7	Data Bit 7
15	D6	Data Bit 6
16	D5	Data Bit 5
17	D4	Data Bit 4
18	D3	Data Bit 3
19	D2	Data Bit 2
20	D1	Data Bit 1
21	D0	Data Bit 0 (LSB)
22	$\overline{CSMSB}$	Chip-Select Most Significant Byte. Active low.
23	$\overline{LDAC}$	Asynchronous Load DAC Input. Active low.
24	$\overline{CSLSB}$	Chip-Select Least Significant Byte. Active low.
25	$\overline{WR}$	Write Input. Active low.
26	V_{DD}	+12V to +15V Supply-Voltage Input
27	V_{SS}	Bias pin for high-temperature, low-leakage configuration
28	N.C.	No Connection. Not internally connected.

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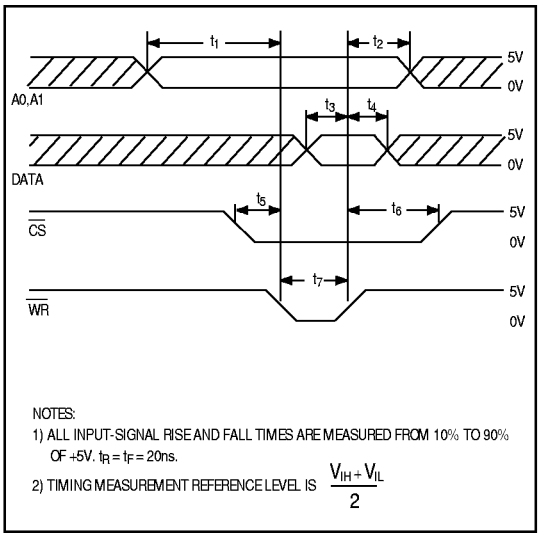

Figure 1a. MX7534 Timing Diagram

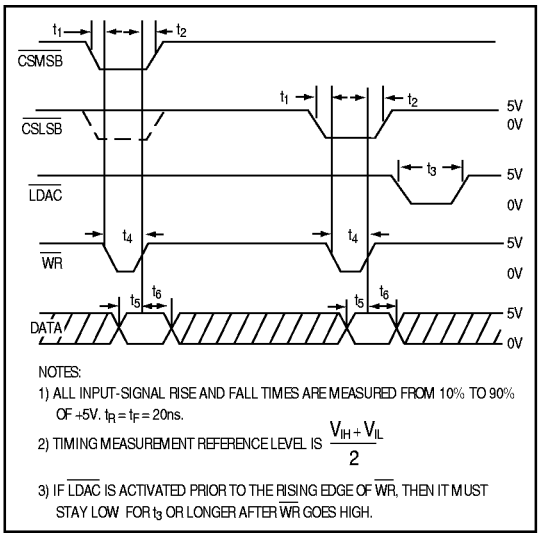

Figure 1b. MX7535 Timing Diagram

Detailed Description

Digital-to-Analog Section

The basic MX7534/MX7535 digital-to-analog converter (DAC) circuit consists of a laser-trimmed, thin-film, 11-bit R-2R resistor array, a 3-bit segmented resistor array, and NMOS current switches, as shown in Figure 2. The three MSBs are decoded to drive switches A–G of the segmented array, and the remaining bits drive switches S0–S10 of the R-2R array.

Binary weighted currents are switched to either AGNDF or I_{OUT}, depending on the status of each input bit. The R-2R ladder current is one-eighth of the total reference input current. The remaining seven-eighths of the current flows in the segmented resistors, dividing equally among these seven resistors. The input resistance at REF is constant; therefore, it can be driven by a voltage or current source of positive or negative polarity.

The MX7534/MX7535 are optimized for unipolar output operation (analog output from 0V to $-V_{REF}$), although bipolar operation (analog output from $+V_{REF}$ to $-V_{REF}$) is possible with some added external components.

Figure 3 shows the equivalent circuit for the two DACs. C_{OUT} varies from about 90pF to 180pF, depending on the digital code. R_0 denotes the DAC'S equivalent output resistance, which varies with the input code. g(V_{REF},N) is the Thevenin equivalent voltage generator due to the reference input voltage, V_{REF}, and the transfer function of the R-2R ladder, N.

Digital Section

All digital inputs are both TTL and 5V CMOS logic compatible. The digital inputs are protected from electrostatic discharge (ESD) with typical input currents of less than 1nA. To minimize power-supply currents, keep digital input voltages as close to 0V and 5V logic levels as possible.

Applications Information

Unipolar Operation (2-Quadrant Multiplication)

Figures 4a and 4b show the circuit diagram for unipolar binary operation. With an AC input, the circuit performs 2-quadrant multiplication. The code table for Figure 4 is given in Table 2.

Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when high-speed op amps are used. Note that the output polarity is the inverse of the reference input.

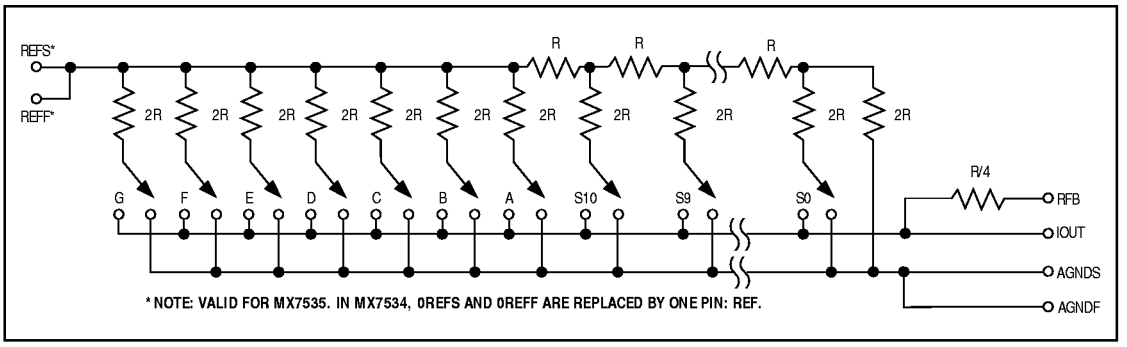

Figure 2. Simplified Circuit Diagram

Zero-Offset Adjustment (Figures 4a and 4b)

1) Load the DAC register with all 0s.
2) Adjust the offset of amplifier A1 so that V_0 (see figure) is at a minimum (i.e., ≤ 30µV).

Gain Adjustment (Figures 4a and 4b)

1) Load the DAC register with all 1s.
2) Trim potentiometer R1 so that $V_{OUT} = -V_{IN}\left(\frac{16383}{16384}\right)$

In fixed-reference applications, adjust full scale by omitting R1 and R2 and trimming the reference voltage magnitude. In many applications, the excellent Gain Tempco and Gain Error specifications eliminate the need for gain adjustment. However, if trims are required and the DAC is to operate over a wide temperature range, use low-tempco (>300ppm/°C) resistors.

Bipolar Operation (4-Quadrant Multiplication)

Bipolar or 4-quadrant operation is shown in Figures 5a and 5b. This configuration provides for offset binary coding. Table 4 shows DAC codes and the corresponding analog outputs for Figures 5a and 5b. With the DAC loaded to 10 0000 0000 0000, either adjust R1 for V_{OUT} = 0V, or omit R1 and R2 and adjust the ratio of R5 and R6 for V_{OUT} = 0V. Adjust the amplitude of V_{IN} or vary the value of R7 for full-scale trimming.

Resistors R5, R6, and R7 must be matched to 0.003%. Mismatch of R5 and R6 causes both offset and full-scale errors. For wide temperature range operation, use resistors of the same material so that their temperature coefficients match and track.

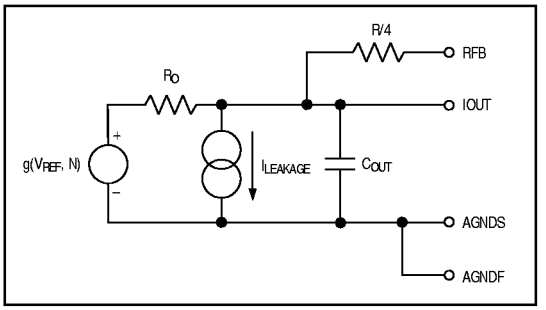

Figure 3. Equivalent Analog Output Circuit

Table 1. MX7534 Logic States

$\overline{WR}$	$\overline{CS}$	A1	A2	FUNCTION
X	1	X	X	Device not selected (Note 1)
1	X	X	X	No data transfer
0	0	0	0	DAC loaded directly from Data Bus (Note 2)
0	0	0	1	MS Input Register loaded from Data Bus
0	0	1	0	LS Input Register loaded from Data Bus
0	0	1	1	DAC Register loaded from Input Registers

Note 1: X = Don't Care.
Note 2: When A1 = 0 and A0 = 0, all DAC registers are transparent. By placing all 0s or all 1s on the data inputs, the user can load the DAC to zero or full-scale output in one write operation. This simplifies system calibration.

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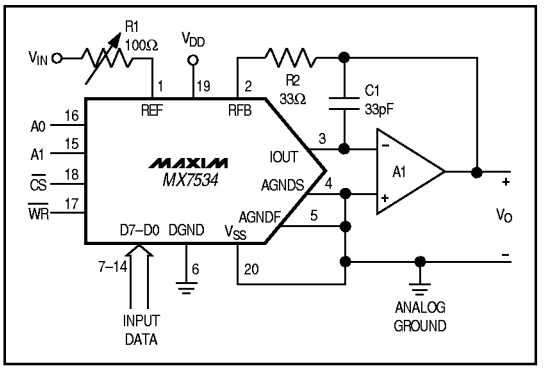


Figure 4a. Unipolar Binary Operation

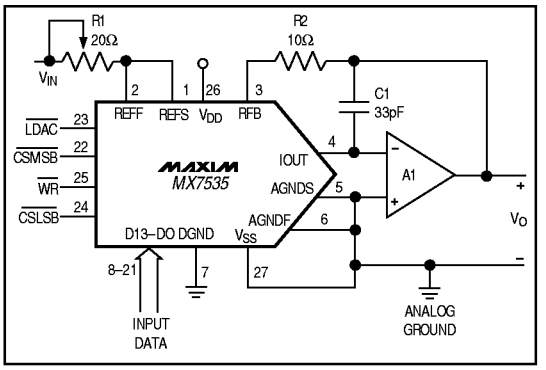


Figure 4b. Unipolar Binary Operation

Grounding Considerations

Since IOUT and the output amplifier noninverting input are sensitive to offset voltages, connect nodes that must be grounded directly to a single-point ground through a separate, very-low-resistance path. Note that the output currents at IOUT and AGNDF vary with input code and create code-dependent error if these terminals are connected to ground (or a virtual ground) through a resistive path.

To obtain high accuracy, it is important to use a proper grounding technique. The two AGND pins (AGNDF, AGNDS) provide flexibility in this respect. In Figures 4a and 4b, AGNDS and AGNDF are shorted together externally and an extra op amp, A2, is not used. Voltage-drops due to bond-wire resistance are not compensated for in this circuit; this could create a linearity error of approximately 0.1LSB due to bond-wire resistance alone. This can be eliminated by using the circuits shown in Figures 6a and 6b, where A2 maintains AGNDS at signal ground potential. By using force/sense techniques, all switch contacts on the DAC are kept at exactly the same potential, and any error caused by bond-wire resistance is eliminated.

Figure 7 shows a remote voltage reference driving the MX7535. Op amps A2 and A3 compensate for voltage drops along the reference input line and analog ground line.

Figure 8 shows a printed circuit board (PCB) layout with a single output amplifier for the MX7534. The input to REF (Pin 1) is shielded to reduce AC feedthrough, while the digital inputs are shielded to minimize digital feedthrough. The traces connecting IOUT and AGNDS to the inverting and noninverting op amp inputs are kept as short as possible. Gain trim components, R3 and R4, are omitted.

Table 2. Unipolar Binary Code Table

BINARY NUMBER IN DAC REGISTER				ANALOG OUTPUT (V_{OUT})
MSB 11	1111	1111	LSB 1111	$-V_{IN}\left(\frac{16383}{16384}\right)$
10	0000	0000	0000	$-V_{IN}\left(\frac{8192}{16384}\right) = -\frac{1}{2} V_{IN}$
00	0000	0000	0001	$-V_{IN}\left(\frac{1}{16384}\right)$
00	0000	0000	0000	0V

Zero-Offset Adjustment (Figures 6a and 6b)

1) Load DAC register with all 0s.
2) Adjust offset of amplifier A2 for minimum potential at AGNDS. This potential should be ≤30µV with respect to signal ground.
3) Adjust A1's offset so that V_{OUT} is at a minimum (i.e., ≤30µV).

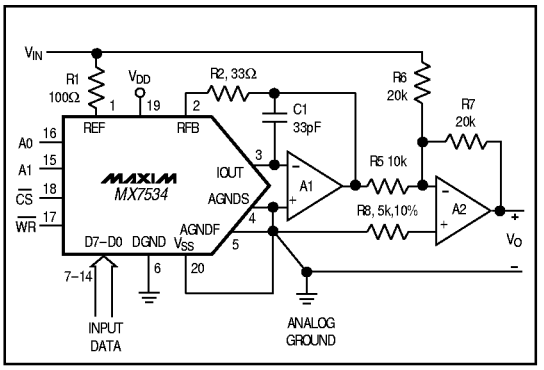


Figure 5a. Bipolar Operation

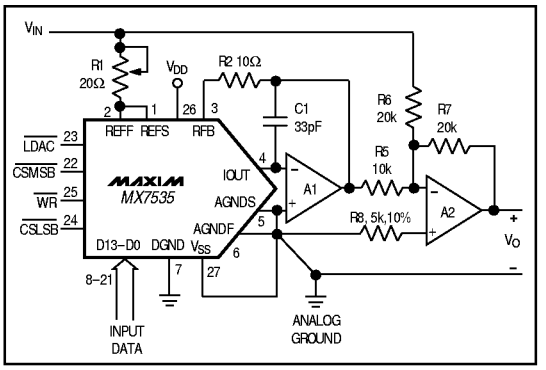


Figure 5b. Bipolar Operation

Gain Adjustment (Figures 6a and 6b)

1) Load DAC register with all 1s.

2) Trim potentiometer R3 so that $V_{OUT} = -\left(\frac{16383}{16384}\right)V_{IN}$

Low-Leakage Configuration

Leakage current in the DAC flowing into the I_{OUT} line can cause gain, linearity, and offset errors. Leakage is worse at high temperatures.

Negatively bias V_{SS} for a high-temperature, low-leakage configuration.

Dynamic Considerations

In static or DC applications, the output amplifier's AC characteristics are not critical. In higher-speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the output op amp's AC parameters must be considered.

Another error source in dynamic applications is the parasitic signal coupling from the REF terminal to I_{OUT}. This is normally a function of board layout and lead-to-lead package capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough depends on circuit-board layout and on-chip capacitive coupling. Minimize layout-induced feedthrough with guard traces between digital inputs, REF, and DAC outputs.

Table 3. MX7535 Logic States

$\overline{CSMSB}$	$\overline{CSLSB}$	$\overline{LDAC}$	$\overline{WR}$	FUNCTION
0	1	1	0	Load MS Input Register
1	0	1	0	Load LS Input Register
0	0	1	0	Load LS and MS Input Registers
1	1	0	X	Load DAC Register from Input Register
0	0	0	0	All registers are transparent.
1	1	1	X	No operation
X	X	1	1	No operation

Note: X = Don't Care.

Table 4. Offset Binary Bipolar Code Table

BINARY NUMBER IN DAC REGISTER				Analog Output (V_{OUT})
MSB			LSB	
11	1111	1111	1111	$+V_{IN}\left(\frac{8191}{8192}\right)$
10	0000	0000	0001	$+V_{IN}\left(\frac{1}{8192}\right)$
10	0000	0000	0000	0
01	1111	1111	1111	$-V_{IN}\left(\frac{1}{8192}\right)$
00	0000	0000	0000	$-V_{IN}\left(\frac{8192}{8192}\right) = -V_{IN}$

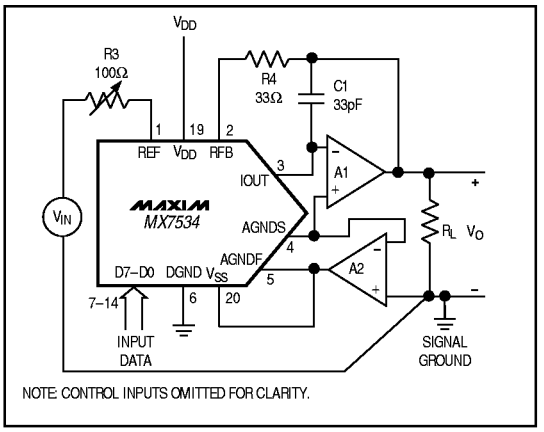


Figure 6a. Unipolar Binary Operation with Forced Ground

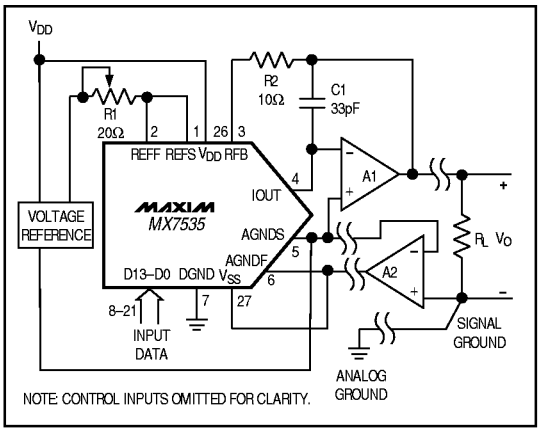


Figure 6b. Unipolar Binary Operation with Forced Ground for Remote Load

Table 5. Amplifier Performance Comparisons

OP AMP	INPUT OFFSET VOLTAGE (V_{OS})	INPUT BIAS CURRENT (I_B)	OFFSET VOLTAGE DRIFT (TC V_{OS})	SETTLING TO 0.003% FS
MAX400	10µV	2nA	0.3µV/°C	50µs
Maxim OP07	25µV	2nA	0.6µV/°C	50µs
AD554L*	500µV	25pA	5µV/°C	5µs
HA2620*	4mV	35nA	20µV/°C	0.8µs

* AD544L is an Analog Devices part; HA2620 is a Harris Semiconductor part.

Compensation

A compensation capacitor, C1, may be needed when the DAC is used with a high-speed output amplifier. The capacitor cancels the pole formed by the DAC's output capacitance and internal feedback resistance. Its value depends on the type of op amp used, but typical values range from 10pF to 33pF. Too small a value causes output ringing, while excess capacitance overdamps the output. Minimize C1's size and improve output settling performance by keeping the PC board trace as short as possible and stray capacitance at I_{OUT} as small as possible.

Bypassing

Place a 1µF bypass capacitor, in parallel with a 0.01µF ceramic capacitor, as close to the DAC's V_{DD} and GND pins as possible. Use a 1µF tantalum bypass capacitor to optimize high-frequency noise rejection. Place a 4.7µF decoupling capacitor at V_{SS} to minimize the DAC output leakage current.

The MX7534/MX7535 have high-impedance digital inputs. To minimize noise pickup, connect them to either V_{DD} or GND terminals when not in use. Connect active inputs to V_{DD} or GND through high-value resistors (1MΩ) to prevent static charge accumulation if these pins are left floating, as might be the case when a circuit card is left unconnected.

Op-Amp Selection

Input offset voltage (V_{OS}), input bias current (I_B), and offset voltage drift (TC V_{OS}) are three key parameters in determining the choice of a suitable amplifier. To maintain specified accuracy with V_{REF} of 10V, V_{OS} should be less than 30µV and I_B should be less than 2nA. Open-loop gain should be greater than 340,000. Maxim's MAX400 has low V_{OS} (10µV max), low I_B (2nA), and low TC V_{OS} (0.3µV/°C max). This op amp can be used without requiring any adjustments. For

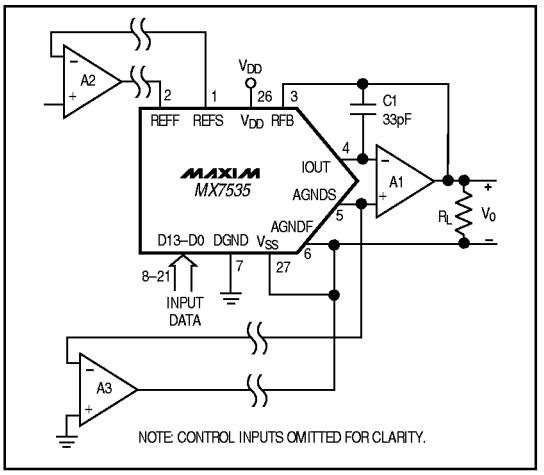


Figure 7. Driving the MX7535 with a Remote Voltage Reference

medium-frequency applications, the OP27 is recommended. For higher-frequency applications, the HA-2620 is recommended. However, these op amps require external offset adjustment (Table 5).

Microprocessor Interfacing

8086 with MX7535

The MX7534/MX7535 interface to both 8-bit and 16-bit processors. Figure 9a shows the 8086 16-bit processor interfacing to a single MX7535. In this setup, the double-buffering feature of the DAC is not used. AD0–AD13 of the 16-bit data bus are connected to the DAC data bus (D0–D13). The 14-bit word is written to the DAC in one MOV instruction, and the analog output responds immediately. In this example, the DAC address is D000. Table 6a shows a software routine for Figure 9a.

In a multiple DAC system, the double buffering of the DAC chips allows the user to simultaneously update all DACs. In Figure 10, a 14-bit word is loaded to each of the DAC's input registers in sequence. Then, with one instruction to the appropriate address, CS4 (i.e., $\overline{LDAC}$) is brought low, updating all the DACs simultaneously.

8086 with MX7534

Figure 9b shows an interface circuit to a 16-bit microprocessor. The bottom 8 bits (AD0–AD7) of the 16-bit data bus are connected to the DAC data bus. The

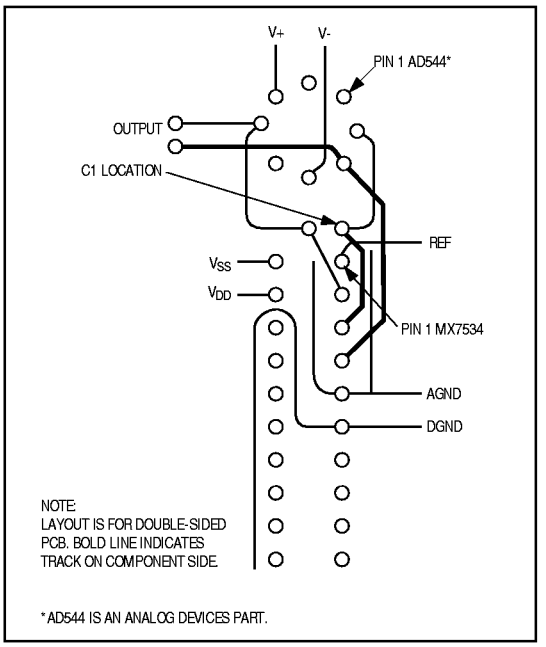


Figure 8. Suggested Layout for MX7534 Incorporating Output Amplifier

14-bit word is loaded in two bytes, using the MOV instruction. A further MOV loads the DAC register and causes the analog data to appear at the converter output. For the example given here, the appropriate DAC register addresses are D002, D004, and D006. Table 6b shows the program for loading the DAC.

8085A with MX7534

A typical interface circuit is shown in Figure 9c. The DAC is treated as four memory locations addressed by A0 and A1. In standard operation, three of these memory locations are used. Table 6c shows a sample program for loading the DAC with a 14-bit word. The MX7534 has address locations 3000–3003.

The six MSBs are written into location 3001, and eight LSBs are written to 3002. Then, with a write instruction to 3003, the full 14-bit word is loaded to the DAC register.

Microprocessor-Compatible, 14-Bit DACs

MC68000 with MX7535

Figure 11a shows an interface diagram. The following routine writes data to the DAC input registers and then outputs the data via the DAC register:

```
01000  MOVE.W   #W,D0        DAC data, W, loaded
                             into Data Register 0.
MOVE.W          D0,$E000     Data W transferred
                             between D0 and DAC
                             Register.
       MOVE.B   #228,D7      Control returned to the
                             System.
       TRAP     #14          Monitor Program
```

MC68000 with MX7534

Figure 11b shows the MC68000 interface diagram. The following routine writes data to the DAC input registers and then outputs the data via the DAC register:

```
       .A2 E003              Address Register 2
                             loaded with E003.
01000  MOVE.W   #W,D0        DAC data, W, loaded
                             into Data Register 0.
       MOVEP.W  D0,$0000(A2) Data W transferred
                             between D0 and the
                             DAC's Input Register.
                             High-ordered byte trans-
                             ferred first. Memory
                             address specified using
                             the address register
                             indirect plus displace-
                             ment addressing mode.
                             Address used here
                             (E003) is odd, so data is
                             transferred on the low-
                             order half of the data
                             bus (D0–D7).
       MOVE.W   D0,$E006     This instruction provides
                             appropriate signals to
                             transfer data W from
                             the DAC Input Register
                             to the DAC Register,
                             which controls the R-2R
                             ladder switches.
       MOVE.B   #228,D7      Control returned to the
                             System.
       TRAP     #14          Monitor Program
```

Since this interfacing system uses only the lower half of the data bus, it is also suitable for use with the MC68008, which provides the user with an 8-bit data bus instead of the MC68000's 16-bit bus.

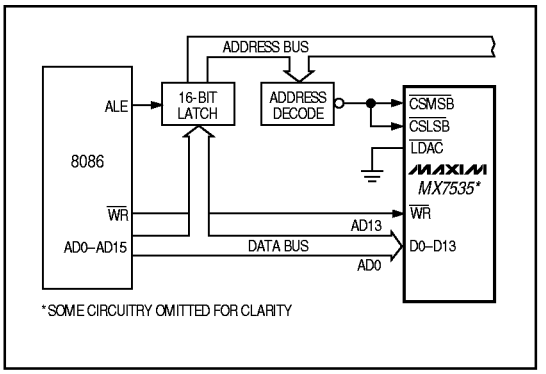


Figure 9a. MX7535—8086 Interface Circuit

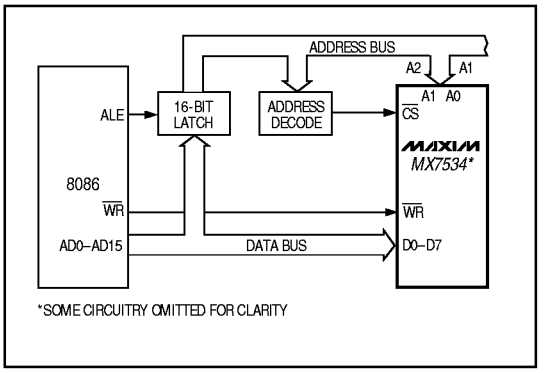


Figure 9b. MX7534—8086 Interface Circuit

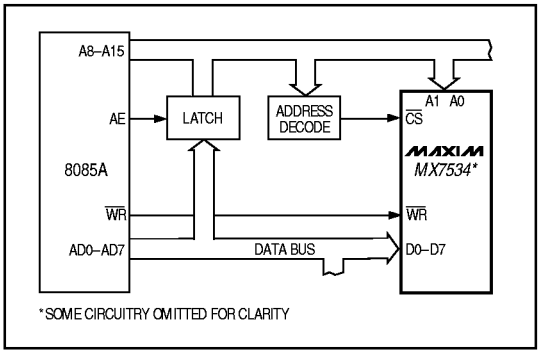


Figure 9c. MX7534—8085A Interface Circuit

Table 6a. Sample Program for Loading the MX7535

```
        ASSUME DS:DACLOAD,CS:DACLOAD
            DACLOAD SEGMENT AT 000
00      8CC9        MOV CX,CS           :DEFINE DATA SEGMENT REGISTER EQUAL
02      8ED9        MOVDS,CX            :TO CODE SEGMENT REGISTER
04      BF00D0      MOVDI,#D000         :LOAD DI WITH D000
07      C705"YZWX"  MOV MEM,#YZWX       :DAC LOADED WITH WXYZ
0B      EA0000                          :CONTROL IS RETURNED TO THE MONITOR PROGRAM
0E      00FF
```

Table 6b. Sample Program for Loading the MX7534 from 8086

```
        ASSUME DS:DACLOAD,CS:DACLOAD
            DACLOAD SEGMENT AT 000
00      8CC9        MOV CX,CS           :DEFINE DATA SEGMENT REGISTER EQUAL
02      8ED9        MOVDS,CX            :TO CODE SEGMENT REGISTER
04      BF02D0      MOVDI.#D002         :LOAD DI WITH D002
07      C605"MS"    MOV MEM,#"MS"       :DAC LOADED WITH "MS"
0A      47          INC DI
0B      47          INC DI
0C      C605"LS"    MOV MEM,#"LS"       :LS INPUT REGISTER LOADED WITH "LS"
0F      47          INC DI
10      47          INC DI
11      C60500      MOV MEM,#00         :CONTENT OF INPUT REGISTERS ARE LOADED TO THE DAC REGISTER
14      EA0000      JMP MEM             :CONTROL IS RETURNED TO THE  MONITOR PROGRAM
```

Table 6c. Sample Program for Loading the MX7534 from 8085A

```
2000    26      MVIH,#30
01      30
02      2E      MVIL,#01
03      01
04      3E      MVIA,#"MS"
05      "MS"
06      77      MOV M,A
07      2C      INR L
08      3E      MVI A#"LS"
09      "LS"
0A      77      MOV M,A
0B      2C      INR L
0C      77      MOV M,A
200D    CF      RST I
```

Z80 with MX7534/MX7535

Figure 12a is an interface circuit for the Z80, using the MX7535. This is an example of an 8-bit processor interface for these DACs. Figure 12b shows the schematic for the MX7534.

MC6809 with MX7534

Figure 13a shows an interface circuit that enables the MX7534 to be programmed using the MC6809 8-bit microprocessor. Use the 16-bit D accumulator to simplify data transfer. The two key processor instructions are:

LDD Load D accumulator from memory

STD Store D accumulator to memory

MC6502 with MX7534

Figure 13b shows an interface diagram for the MC6502 using the MX7534.

Digital Feedthrough

In the interface diagrams shown in Figures 9–13, the digital inputs of the DAC are directly connected to the microprocessor bus. Even when the device is not selected, activity on the bus can feed through on the DAC output through package capacitance and appear as noise. To minimize noise, isolate the DACs from the digital bus, as shown in Figures 14a and 14b.

Microprocessor-Compatible, 14-Bit DACs

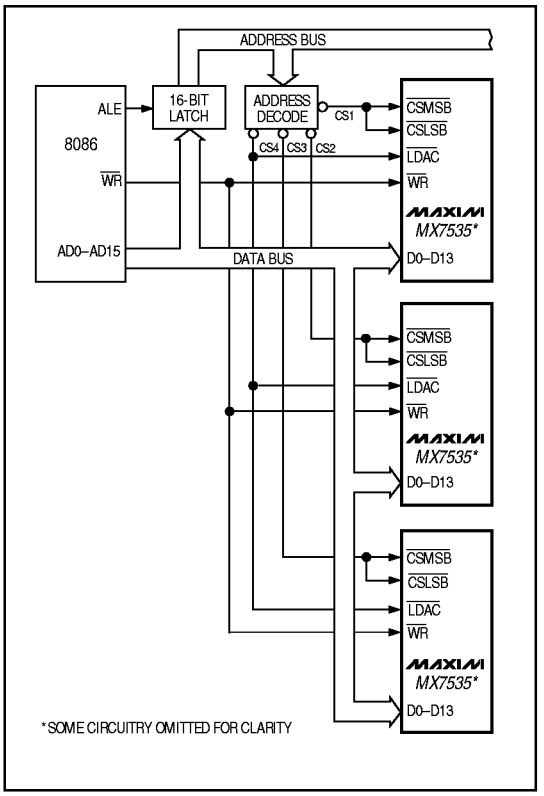


Figure 10. MX7535—8086 Interface: Multiple DAC Systems

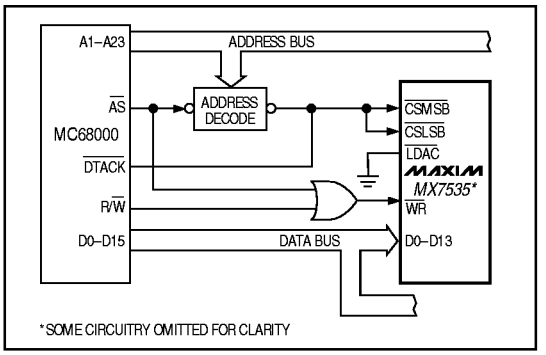


Figure 11a. MX7535—MC68000 Interface

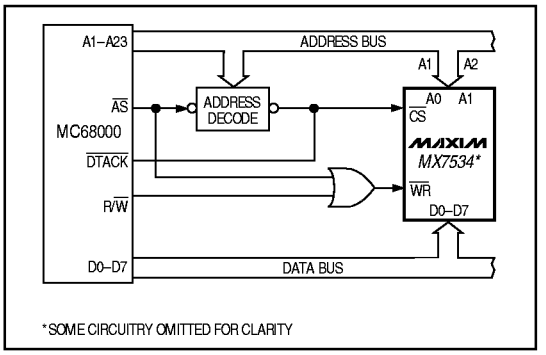


Figure 11b. MX7534—MC68000 Interface

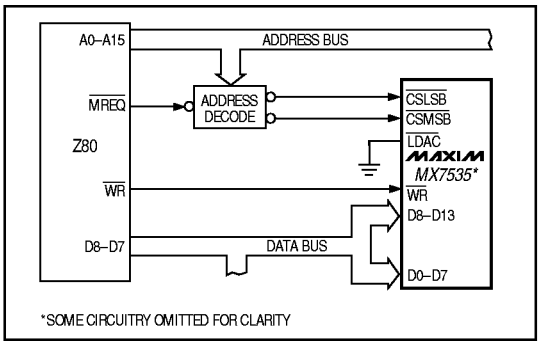


Figure 12a. MX7535—Z80 Interface

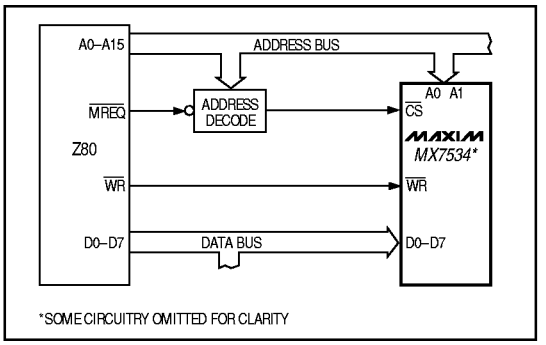


Figure 12b. MX7534—Z80 Interface

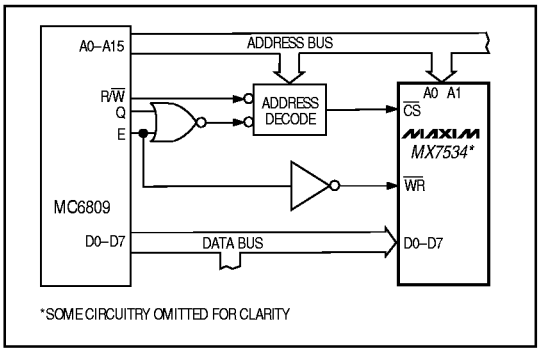


Figure 13a. MX7534—MC6809 Interface Circuit

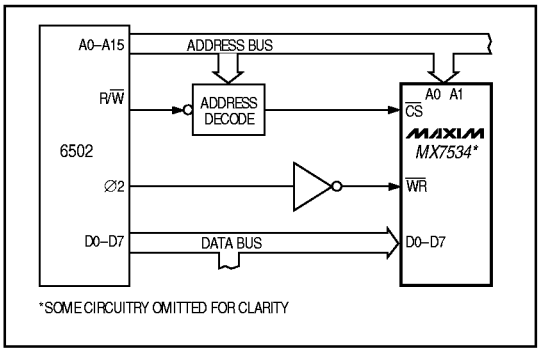


Figure 13b. MX7534—6502 Interface

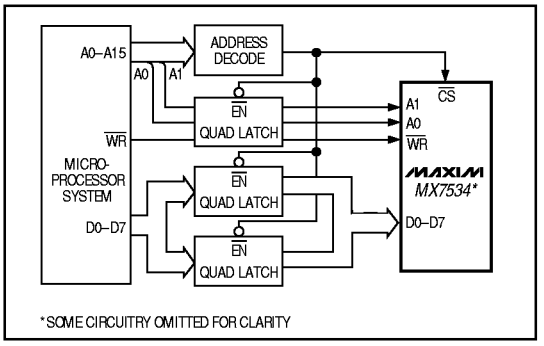


Figure 14a. MX7534—Interface Circuit Using Latches to Minimize Digital Feedthrough

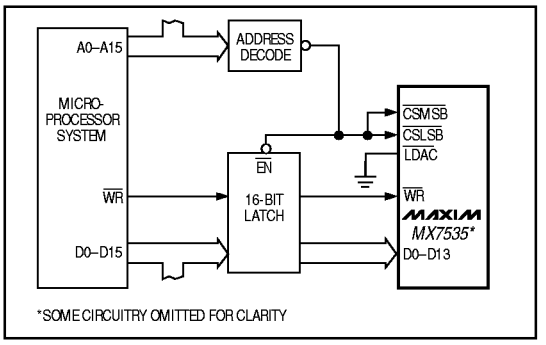
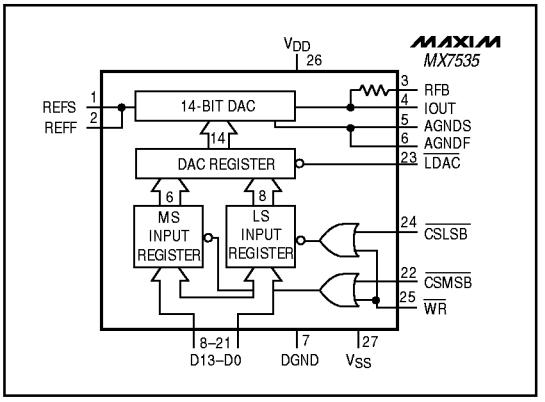


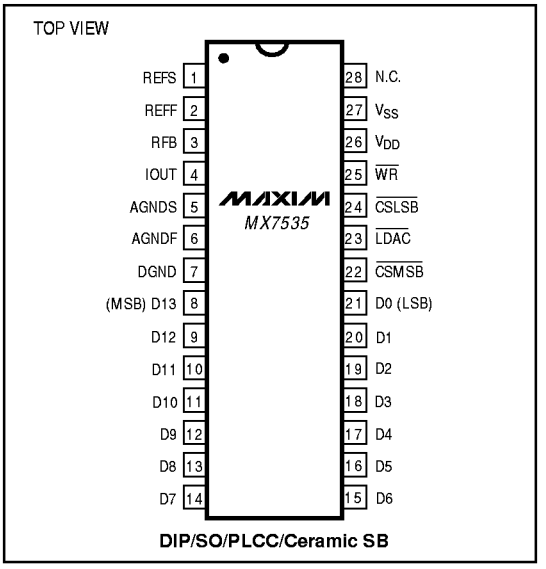
Figure 14b. MX7535—Interface Circuit Using Latches to Minimize Digital Feedthrough

Microprocessor-Compatible, 14-Bit DACs

Functional Diagrams (continued)



Pin Configurations (continued)



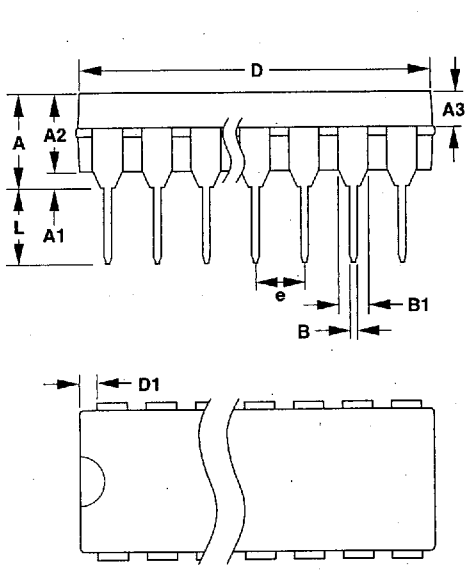
DIP/SO/PLCC/Ceramic SB

Ordering Information (continued)

PART	TEMP. RANGE	PIN PACKAGE	INL (LSBs)
MX7535KN	0°C to +70°C	28 Plastic DIP	±1
MX7535JN	0°C to +70°C	28 Plastic DIP	±2
MX7535KCWI	0°C to +70°C	28 Wide SO	±1
MX7535JCWI	0°C to +70°C	28 Wide SO	±2
MX7535KP	0°C to +70°C	28 PLCC	±1
MX7535JP	0°C to +70°C	28 PLCC	±2
MX7535J/D	0°C to +70°C	Dice*	±2
MX7535BQ	-25°C to +85°C	28 CERDIP	±1
MX7535AQ	-25°C to +85°C	28 CERDIP	±2
MX7535BD	-25°C to +85°C	28 Ceramic SB	±1
MX7535AD	-25°C to +85°C	28 Ceramic SB	±2
MX7535KEWI	-40°C to +85°C	28 Wide SO	±1
MX7535JEWI	-40°C to +85°C	28 Wide SO	±2
MX7535TQ	-55°C to +125°C	28 CERDIP	±1
MX7535SQ	-55°C to +125°C	28 CERDIP	±2
MX7535TD	-55°C to +125°C	28 Ceramic SB	±1
MX7535SD	-55°C to +125°C	28 Ceramic SB	±2

**Dice are tested at +25°C, DC parameters only.*

This section contains physical dimensions for all packages currently supplied by Maxim.

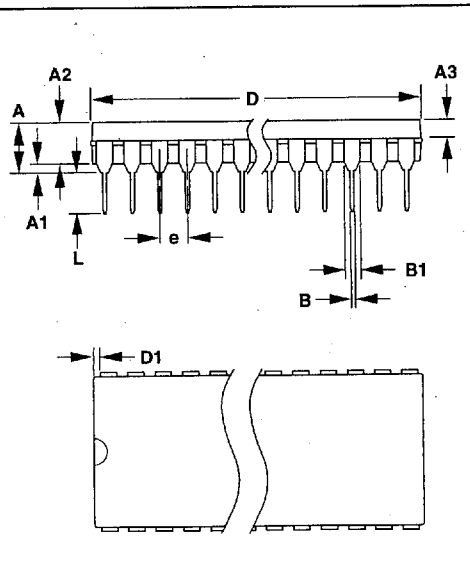


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

21-0043A



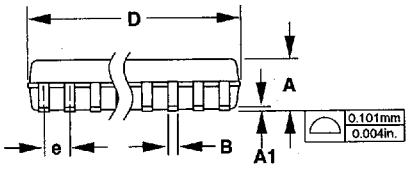
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.020	0.41	0.51
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.050	0.090	1.27	2.29
E	0.600	0.625	15.24	15.88
E1	0.525	0.575	13.34	14.61
e	0.100	–	2.54	–
eA	0.600	–	15.24	–
eB	–	0.700	–	17.78
L	0.120	0.150	3.05	3.81

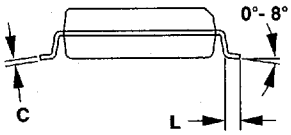
Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.600 in.)

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	24	1.230	1.270	31.24	32.26
P	D	28	1.430	1.470	36.32	37.34
P	D	40	2.025	2.075	51.44	52.71

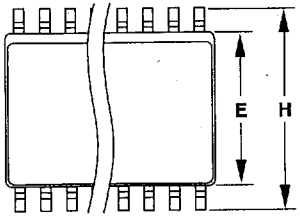
21-0044A

A





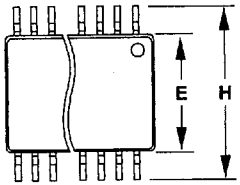
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
E	0.291	0.299	7.40	7.60
e	0.050		1.27	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27

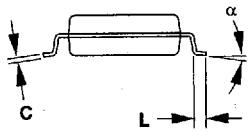


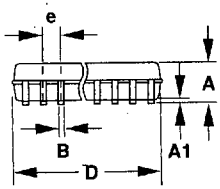
Wide SO
SMALL-OUTLINE
PACKAGE
(0.300 in.)

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.398	0.413	10.10	10.50
D	18	0.447	0.463	11.35	11.75
D	20	0.496	0.512	12.60	13.00
D	24	0.598	0.614	15.20	15.60
D	28	0.697	0.713	17.70	18.10

21-0042A







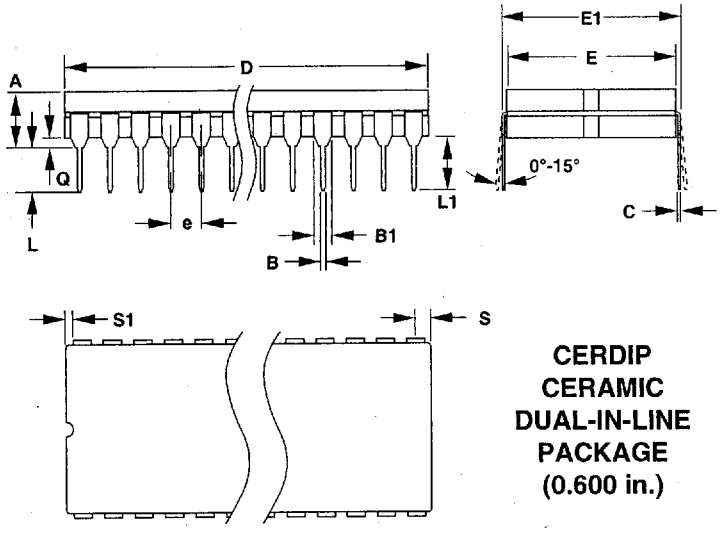
SSOP
SHRINK
SMALL-OUTLINE
PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	14	0.239	0.249	6.07	6.33
D	16	0.239	0.249	6.07	6.33
D	20	0.278	0.289	7.07	7.33
D	24	0.317	0.328	8.07	8.33
D	28	0.397	0.407	10.07	10.33

21-0056A

A

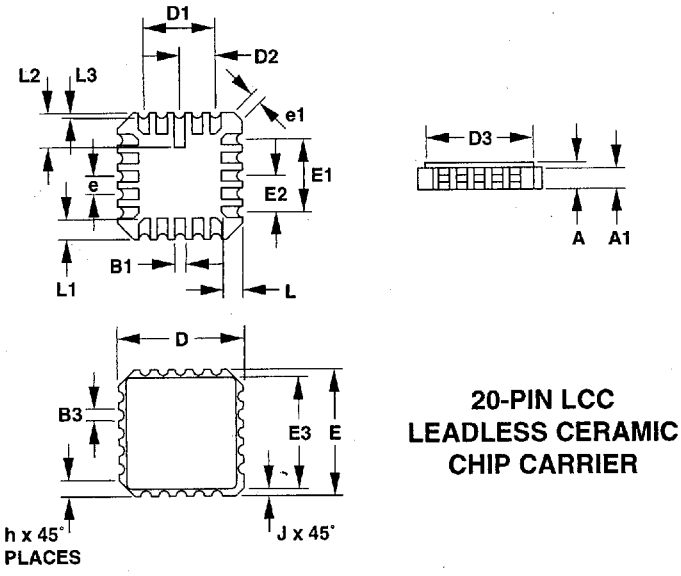


CERDIP
CERAMIC
DUAL-IN-LINE
PACKAGE
(0.600 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.232	–	5.89
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.500	0.620	12.70	15.75
E1	0.590	0.630	14.99	16.00
e	0.100		2.54	
L	0.120	0.200	3.05	5.08
L1	0.150	–	3.81	–
Q	0.015	0.075	0.38	1.91
S	–	0.100	–	2.54
S1	0.005	–	0.13	–

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	24	–	1.290	–	32.77
D	28	–	1.490	–	37.85
D	40	–	2.096	–	53.24

21-0046A

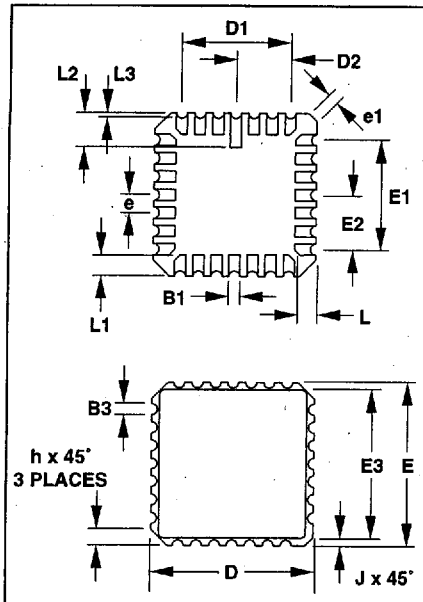


20-PIN LCC
LEADLESS CERAMIC
CHIP CARRIER

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.060	0.100	1.52	2.54
A1	0.050	0.088	1.27	2.24
B1	0.022	0.028	0.56	0.71
B3	0.006	0.022	0.15	0.56
D/E	0.342	0.358	8.69	9.09
D1/E1	0.200 BSC		5.08 BSC	
D2/E2	0.100 BSC		2.54 BSC	
D3/E3	–	0.350	–	9.09
e	0.050 BSC		1.27 BSC	
e1	0.015	–	0.38	–
h	0.040 REF		1.02 REF	
J	0.020 REF		0.51 REF	
L	0.045	0.055	1.14	1.40
L1	0.045	0.055	1.14	1.40
L2	0.075	0.095	1.91	2.41
L3	0.003	0.015	0.08	0.38

21-658A

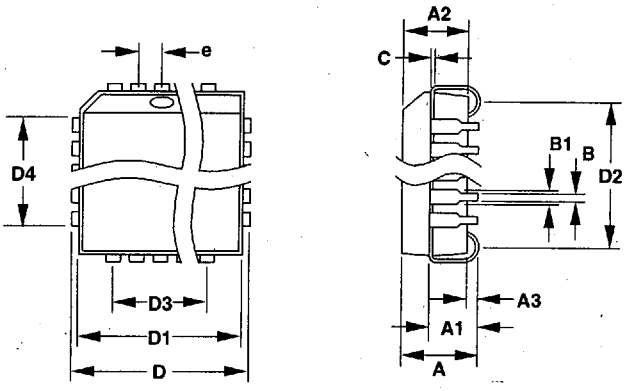
A



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.060	0.100	1.52	2.54
A1	0.050	0.088	1.27	2.24
B1	0.022	0.028	0.56	0.71
B3	0.006	0.022	0.15	0.56
D/E	0.442	0.460	11.23	11.68
D1/E1	0.300		7.62	
D2/E2	0.150		3.81	
D3/E3	–	0.460	–	11.68
e	0.050		1.27	
e1	0.015	–	0.38	–
h	0.040 REF		1.02 REF	
J	0.020 REF		0.51 REF	
L	0.045	0.055	1.14	1.40
L1	0.045	0.055	1.14	1.40
L2	0.075	0.095	1.91	2.41
L3	0.003	0.015	0.08	0.38

21-4497A

28-PIN LCC
LEADLESS CERAMIC
CHIP CARRIER

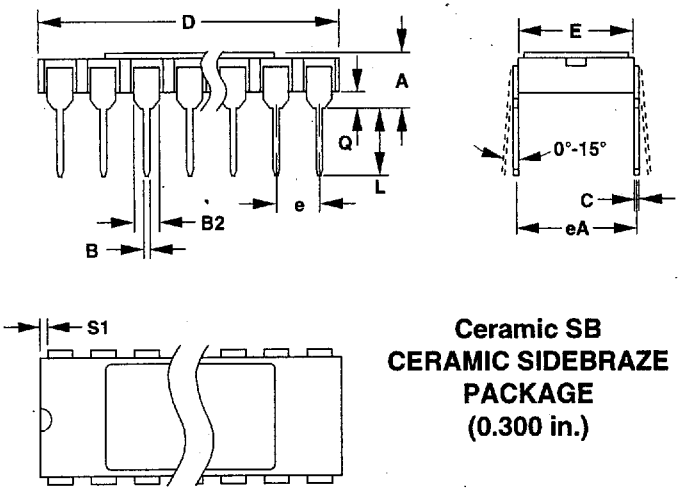


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.145	0.156	3.68	3.96
A3	0.020	–	0.51	–
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.009	0.011	0.23	0.28
e	0.050		1.27	

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	20	0.385	0.395	9.78	10.03
D1		0.350	0.356	8.89	9.04
D2		0.290	0.330	7.37	8.38
D3		0.200 REF		5.08 REF	
D	28	0.485	0.495	12.32	12.57
D1		0.450	0.456	11.43	11.58
D2		0.390	0.430	9.91	10.92
D3		0.300 REF		7.62 REF	
D4		0.300	–	7.62	–
D	44	0.685	0.695	17.40	17.65
D1		0.650	0.656	16.51	16.66
D2		0.590	0.630	14.99	16.00
D3		0.500 REF		12.70 REF	
D4		0.470	–	11.94	–
D	68	0.985	0.995	25.02	25.27
D1		0.950	0.958	24.13	24.33
D2		0.890	0.930	22.61	23.62
D3		0.800 REF		20.32 REF	
D4		0.625	–	15.87	–

21-0049B

PLCC
PLASTIC
LEADED CHIP CARRIER

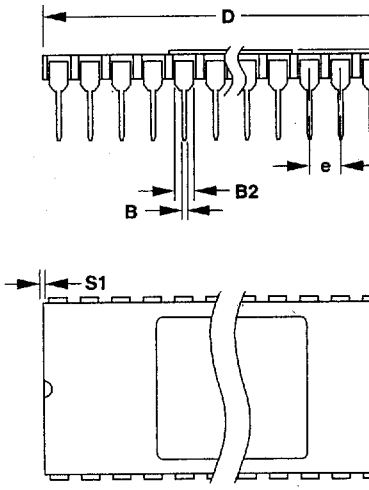


Ceramic SB
CERAMIC SIDEBRAZE
PACKAGE
(0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.225	–	5.72
B	0.014	0.023	0.36	0.58
B2	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
eA	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
Q	0.015	0.070	0.38	1.78
S1	0.005	–	0.13	–

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	–	0.550	–	13.97
D	14	–	0.785	–	19.94
D	16	–	0.840	–	21.34
D	18	–	0.960	–	24.38
D	20	–	1.060	–	26.92
D	24	–	1.280	–	32.51

21-0047A



Ceramic SB
CERAMIC SIDEBRAZE
PACKAGE
(0.600 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.225	–	5.72
B	0.014	0.023	0.36	0.58
B2	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.510	0.610	12.95	15.49
eA	0.600		15.24	
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S1	0.005	–	0.13	–

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	24	–	1.29	–	32.77
D	28	–	1.49	–	37.85
D	40	–	2.096	–	53.24

21-0048A

A