CYPRESS

CY27H010

128K x 8 High-Speed CMOS EPROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **t_{AA} = 25 ns max. (commercial)**
  - **t_{AA} = 35 ns max. (military)**
- **Low power**
  - **275 mW max.**
  - **Less than 85 mW when deselected**
- **Byte-wide memory organization**
- **100% reprogrammable in thewindowed package**
- **EPROM technology**
- **Capable of withstanding >2001V static discharge**
- **Available in**
  - **32-pin PLCC**
  - **32-pin TSOP-I**
  - **32-pin, 600-mil plastic or hermetic DIP**
  - **32-pin hermetic LCC**

Functional Description
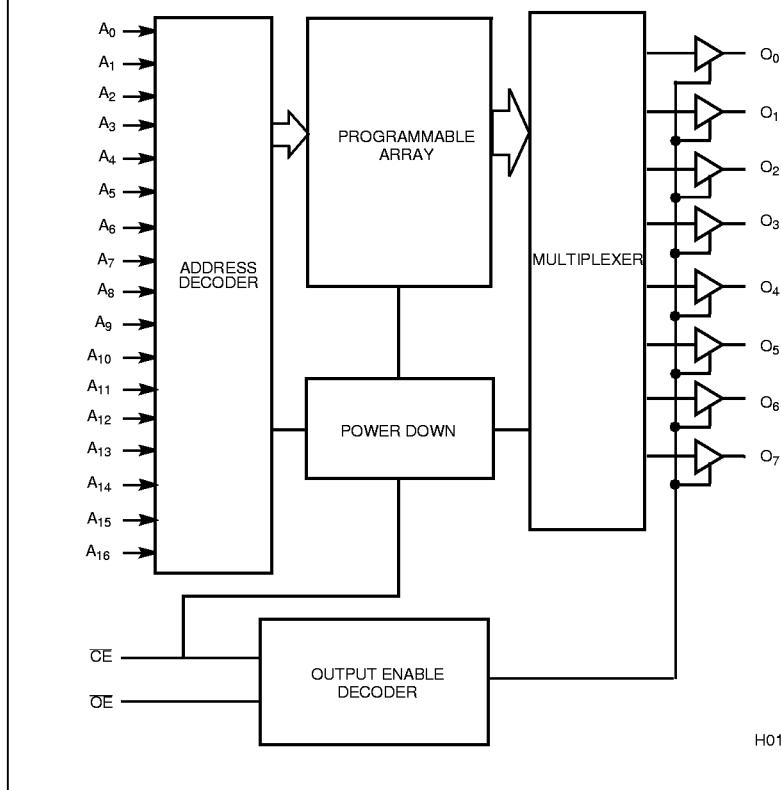
The CY27H010 is a high-performance, 1-megabit CMOS EPROM organized in 128 Kbytes. It is available in indus-try-standard 32-pin, 600-mil DIP, LCC, PLCC, and TSOP-I packages. These devices offer high-density storage combined with 40-MHz performance. The CY27H010 is available in windowed and opaque packages. Windowed packages allow the device to be erased with UV light for 100% reprogrammability.

The CY27H010 is equipped with a power-down chip enable ($\overline{CE}$) input and output enable ($\overline{OE}$). When $\overline{CE}$ is deasserted, the device powers down to a low-power stand-by mode. The $\overline{OE}$ pin three-states the outputs without putting the device into stand-by mode. While $\overline{CE}$ offers lower power, $\overline{OE}$ provides a more rapid transition to and from three-stated outputs.
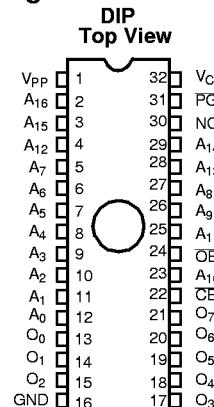
The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms. The EPROM cell requires only 12.75 V for the supervoltage and low programming current allows for gang programming. The device allows for each memory location to be tested 100%, because each location is written to, erased, and repeatedly exercised prior to encapsulation. Each device is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

The CY27H010 is read by asserting both the $\overline{CE}$ and the $\overline{OE}$ inputs. The contents of the memory location selected by the address on inputs A_{16}–A_0 will appear at the outputs O_7–O_0.
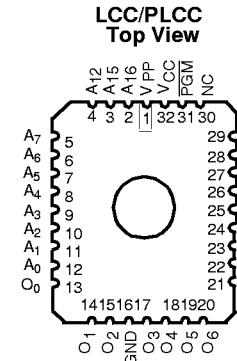
Logic Block Diagram
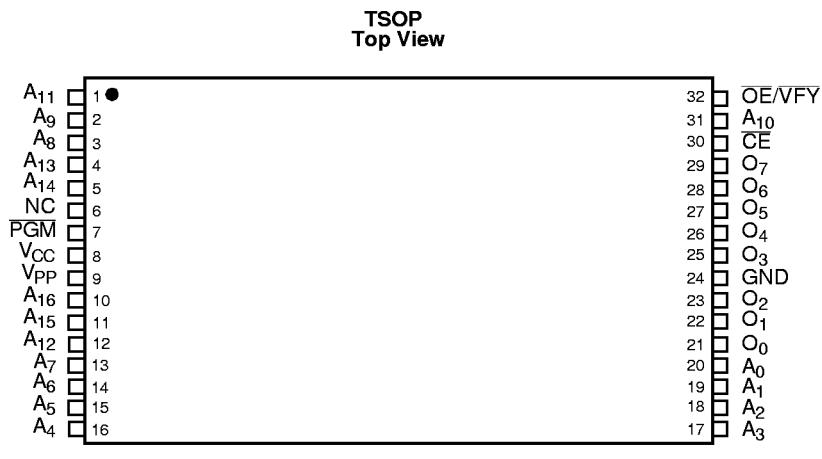
Pin Configurations

Pin Configurations (continued)

TSOP
Top View

Left (pin #)		Right (pin #)	
A_{11}	1●	32	$\overline{OE}/VFY$
A_9	2	31	A_{10}
A_8	3	30	$\overline{CE}$
A_{13}	4	29	O_7
A_{14}	5	28	O_6
NC	6	27	O_5
$\overline{PGM}$	7	26	O_4
V_{CC}	8	25	O_3
V_{PP}	9	24	GND
A_{16}	10	23	O_2
A_{15}	11	22	O_1
A_{12}	12	21	O_0
A_7	13	20	A_0
A_6	14	19	A_1
A_5	15	18	A_2
A_4	16	17	A_3

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Selection Guide

		27H010–25	27H010–30	27H010–35	27H010–45	27H010–55	27H010–70
Maximum Access Time (ns)		25	30	35	45	55	70
$\overline{CE}$ Access Time (ns)	Com'l	30	30	40	45	55	70
$\overline{CE}$ Access Time (ns)	Mil			40	45	55	70
$\overline{OE}$ Access Time (ns)	Com'l	12	20	20	20	25	35
$\overline{OE}$ Access Time (ns)	Mil			20	20	25	35
I_{CC}[1] (mA) Power Supply Current	Com'l	75	75	50	50	50	50
	Mil			85	60	60	60
I_{SB}[2] (mA) Stand-by Current	Com'l	15	15	15	15	15	15
	Mil			25	25	25	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with
Power Applied .... –55°C to +125°C

Supply Voltage to Ground Potential .... –0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State .... –0.5V to +5.5V

DC Input Voltage .... –3.0V to +7.0V

Transient Input Voltage .... –3.0V for <20 ns

DC Program Voltage 13.0V

UV Erasure .... 7258 Wsec/cm^2

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[3]	–40°C to +85°C	5V ± 10%
Military[4]	–55°C to +125°C	5V ± 10%

Notes:
1. V_{CC} = Max., I_{OUT} = 0 mA, f=10 MHz.
2. V_{CC} = Max., $\overline{CE}$ = V_{IH}.
3. Contact a Cypress representative for industrial temperature range specification.
4. T_A is the "instant on" case temperature.

## Electrical Characteristics Over the Operating Range[5, 6]
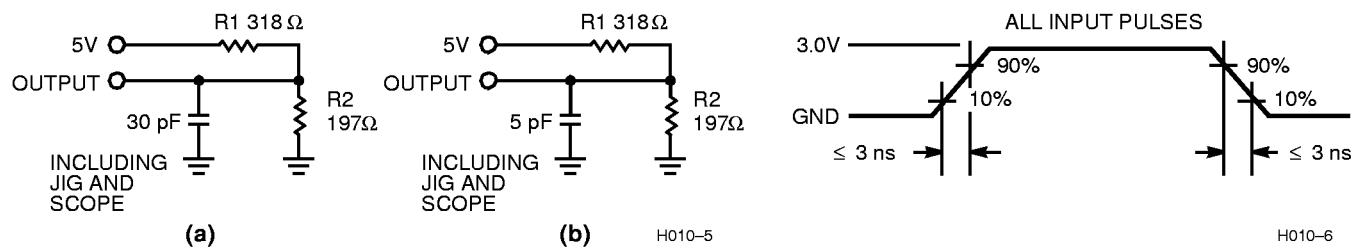
Parameter	Description	Test Conditions		27H010–25 27H010–30 Min.	27H010–25 27H010–30 Max.	27H010–35 Min.	27H010–35 Max.	27H010–45 27H010–55 27H010–70 Min.	27H010–45 27H010–55 27H010–70 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA			0.45		0.45		0.45	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}+0.5	2.0	V_{CC}+0.5	2.0	V_{CC}+0.5	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		–10	+10	–10	+10	–10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disable		–10	+10	–10	+10	–10	+10	μA
I_{CC}	Power Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=10 MHz	Com'l		75		50		50	mA
			Mil				85		60	mA
I_{SB}	Stand-By Current	V_{CC}=Max., $\overline{CE}$ = V_{IH}	Com'l		15		15		15	mA
			Mil				25		25	mA

Capacitance[6]
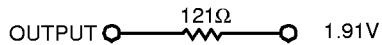
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		12	pF

Notes:
5. See the last page of this specification for Group A subgroup testing information.
6. See Introduction to CMOS PROMs in this Data Book for general information on testing.

AC Test Loads and Waveforms

R1 318Ω
5V
OUTPUT
30 pF
R2 197Ω
INCLUDING JIG AND SCOPE
(a)

R1 318Ω
5V
OUTPUT
5 pF
R2 197Ω
INCLUDING JIG AND SCOPE
(b)   H010–5

ALL INPUT PULSES
3.0V
90%
10%
GND
≤ 3 ns
90%
10%
≤ 3 ns
H010–6
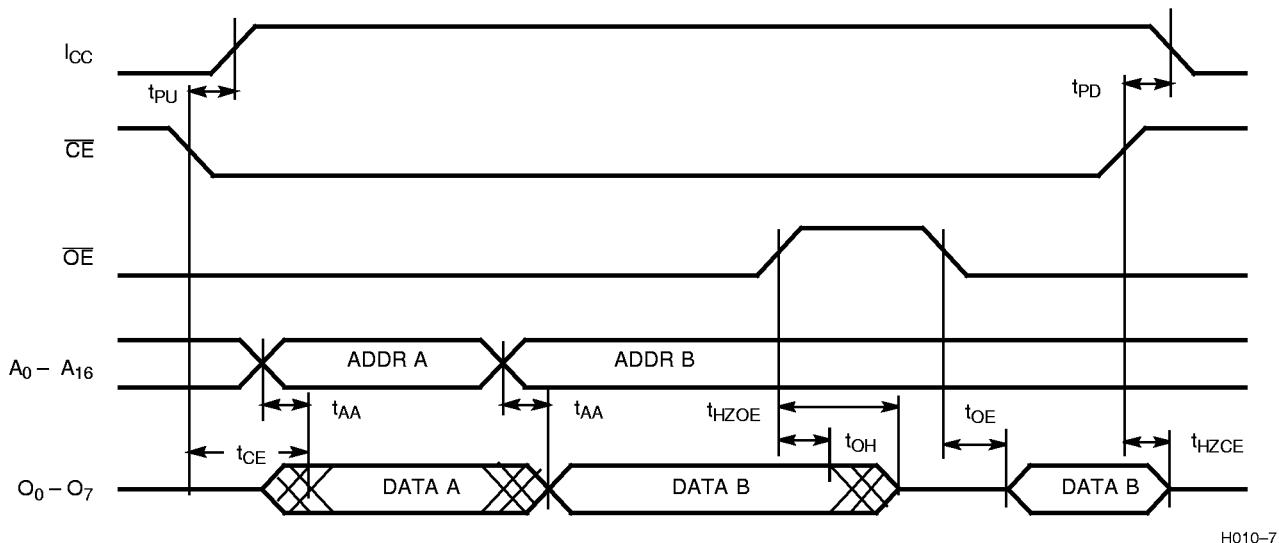
Equivalent to: THÉVENIN EQUIVALENT
121Ω
OUTPUT   1.91V

Switching Characteristics Over the Operating Range

Parameter	Description	27H010–25 Min.	27H010–25 Max.	27H010–30 Min.	27H010–30 Max.	27H010–35 Min.	27H010–35 Max.	27H010–45 Min.	27H010–45 Max.	27H010–55 Min.	27H010–55 Max.	27H010–70 Min.	27H010–70 Max.	Unit
t_{AA}	Address to Output Valid		25		30		35		45		55		70	ns
t_{OE}	$\overline{OE}$ Active to Output Valid		12		20		20		20		25		35	ns
t_{HZOE}	$\overline{OE}$ Inactive to High Z		12		20		20		20		25		35	ns
t_{CE}	$\overline{CE}$ Active to Output Valid		30		30		40		45		55		70	ns
t_{HZCE}	$\overline{CE}$ Inactive to High Z		12		20		20		20		25		35	ns
t_{PU}	$\overline{CE}$ Active to Power-Up	0		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ Inactive to Power-Down		30		35		40		50		60		75	ns
t_{OH}	Output Data Hold	0		0		0		0		0		0		ns

Switching Waveform

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Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the CY27H010 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY27H010 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

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Table 1. Programming Electrical Characteristics

Parameter	Description	Min.	Max.	Unit
V_{PP}	Programming Power Supply	12.5	13	V
I_{PP}	Programming Supply Current		50	mA
V_{IHP}	Programming Input Voltage HIGH	3.0	V_{CC}	V
V_{ILP}	Programming Input Voltage LOW	−0.5	0.4	V
V_{CCP}	Programming V_{CC}	6.0	6.5	V

Table 2. Mode Selection
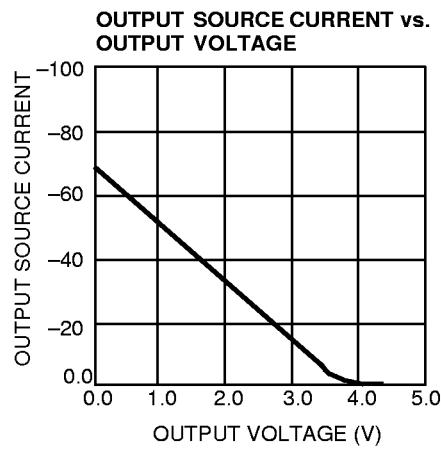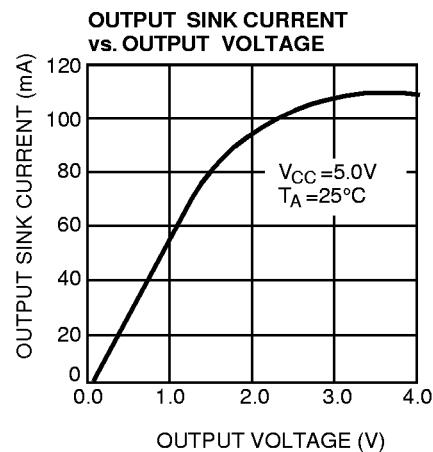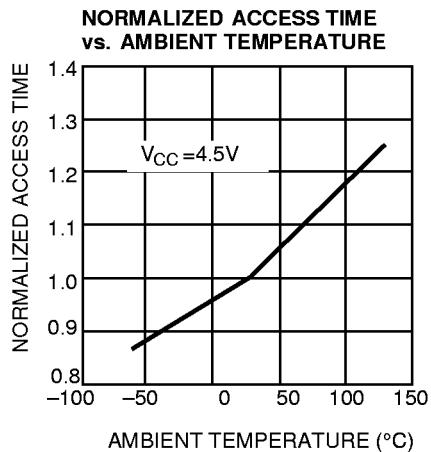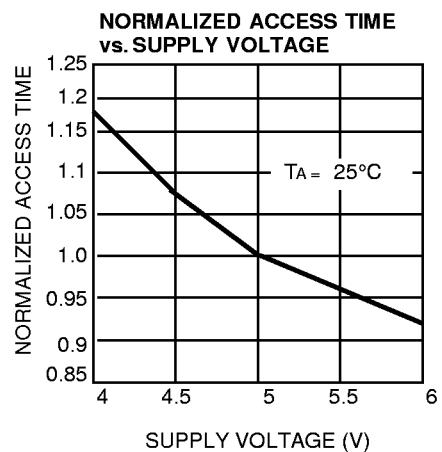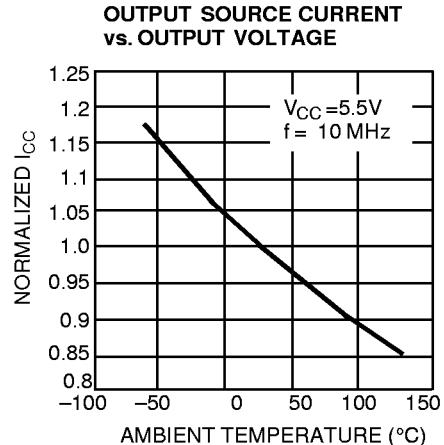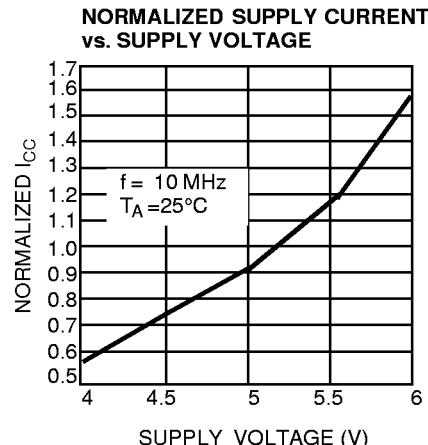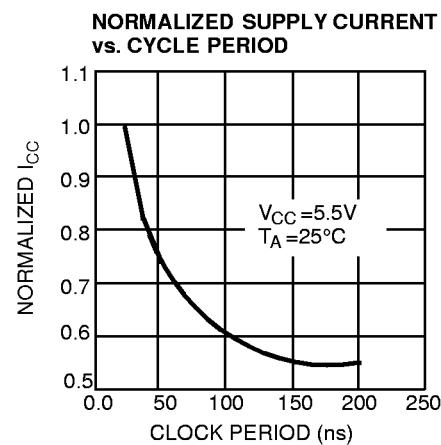
Mode	Pin Function[7]						
	CE	OE	PGM	V_{PP}	A_0	A_9	Data
Read	V_{IL}	V_{IL}	X	V_{IH}	A_0	A_9	$O_7 - O_0$
Output Disable	V_{IL}	V_{IH}	X	V_{IH}	A_0	A_9	High Z
Stand-by	V_{IH}	X	X	V_{IH}	X	X	High Z
Program	V_{ILP}	V_{IHP}	V_{ILP}	V_{PP}	A_0	A_9	$D_7 - D_0$
Program Verify	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	A_0	A_9	$O_7 - O_0$
Program Inhibit	V_{ILP}	V_{IHP}	V_{IHP}	V_{PP}	A_0	A_9	High Z
Signature Read (MFG)	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	V_{HV}[8]	34H
Signature Read (DEV)	V_{IL}	V_{IL}	X	V_{IH}	V_{IH}	V_{HV}[8]	1DH

Notes:
7. X can be V_{IL} or V_{IH}.
8. V_{HV}=12V±0.5V

Typical DC and AC Characteristics

NORMALIZED SUPPLY CURRENT vs. CYCLE PERIOD

$V_{CC} = 5.5V$
$T_A = 25°C$

NORMALIZED I_{CC}

CLOCK PERIOD (ns)

NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

$f = 10 MHz$
$T_A = 25°C$

NORMALIZED I_{CC}

SUPPLY VOLTAGE (V)

OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

$V_{CC} = 5.5V$
$f = 10 MHz$

NORMALIZED I_{CC}

AMBIENT TEMPERATURE (°C)

NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

$T_A = 25°C$

NORMALIZED ACCESS TIME

SUPPLY VOLTAGE (V)

NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

$V_{CC} = 4.5V$

NORMALIZED ACCESS TIME

AMBIENT TEMPERATURE (°C)

OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

$V_{CC} = 5.0V$
$T_A = 25°C$

OUTPUT SINK CURRENT (mA)

OUTPUT VOLTAGE (V)

OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

OUTPUT SOURCE CURRENT

OUTPUT VOLTAGE (V)

H010–8

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Ordering Information[9]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY27H010–25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H010–25ZC	Z32	32-Lead Thin Small Outline Package	
30	CY27H010–30JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H010–30PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27H010–30WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27H010–30ZC	Z32	32-Lead Thin Small Outline Package	
35	CY27H010–35JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H010–35PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27H010–35WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27H010–35ZC	Z32	32-Lead Thin Small Outline Package	
	CY27H010–35LMB	L55	32-Pin Rectangular Leadless Chip Carrier	Military
	CY27H010–35QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
45	CY27H010–45JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H010–45PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27H010–45WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27H010–45ZC	Z32	32-Lead Thin Small Outline Package	
	CY27H010–45DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27H010–45LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H010–45QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H010–45WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
55	CY27H010–55JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H010–55PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27H010–55WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27H010–55ZC	Z32	32-Lead Thin Small Outline Package	
	CY27H010–55DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27H010–55LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H010–55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H010–55WMB	W20	32-Lead (600-Mil) Windowed CerDIP	
70	CY27H010–70JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27H010–70PC	P19	32-Lead (600-Mil) Molded DIP	
	CY27H010–70WC	W20	32-Lead (600-Mil) Windowed CerDIP	
	CY27H010–70ZC	Z32	32-Lead Thin Small Outline Package	
	CY27H010–70DMB	D20	32-Lead (600-Mil) CerDIP	Military
	CY27H010–70LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H010–70QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H010–70WMB	W20	32-Lead (600-Mil) Windowed CerDIP	

Note:
9. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3
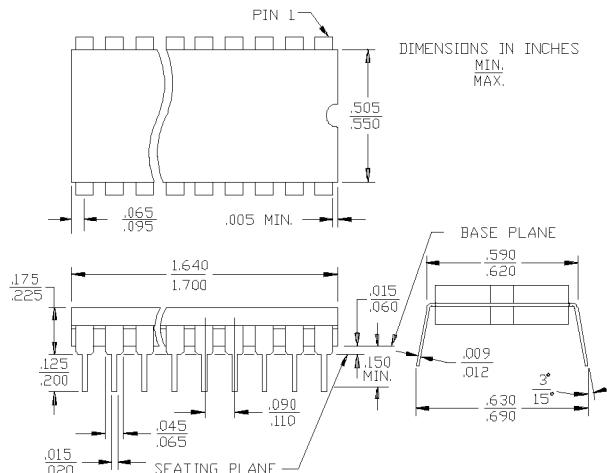
Switching Characteristics

| Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{OE}	7, 8, 9, 10, 11
t_{CE}	7, 8, 9, 10, 11
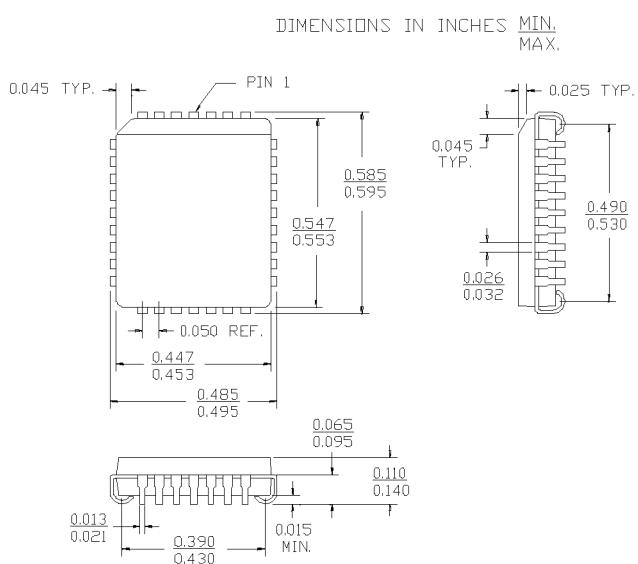
Document #: 38–00171–C

## Package Diagrams
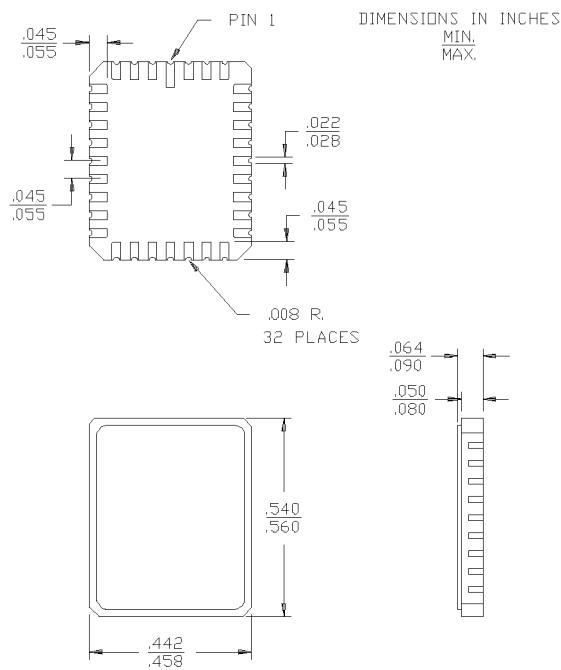
32-Lead (600-Mil) CerDIP D20
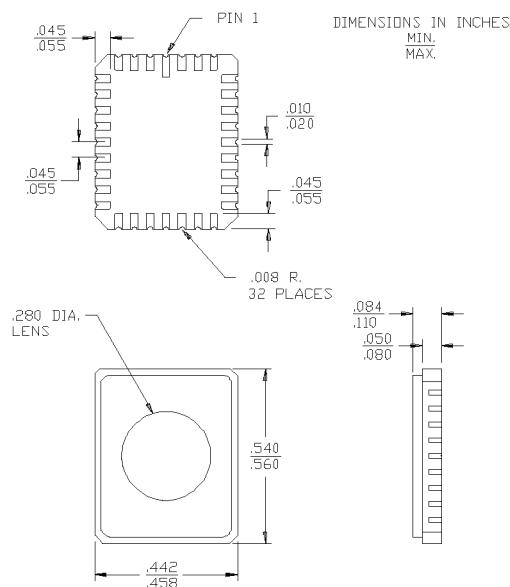
32-Lead Plastic Leaded Chip Carrier J65

32-Pin Rectangular Leadless Chip Carrier L55
MIL-STD-1835 C-12
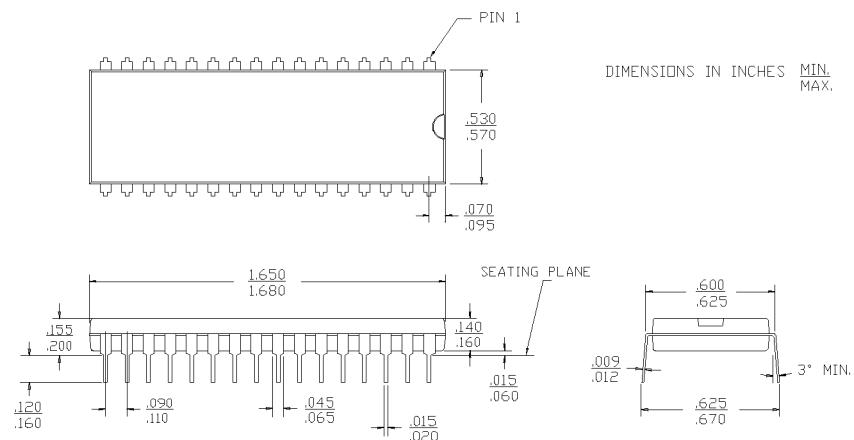
### 32-Pin Windowed Rectangular Leadless Chip Carrier
MIL-STD-1835 C-12
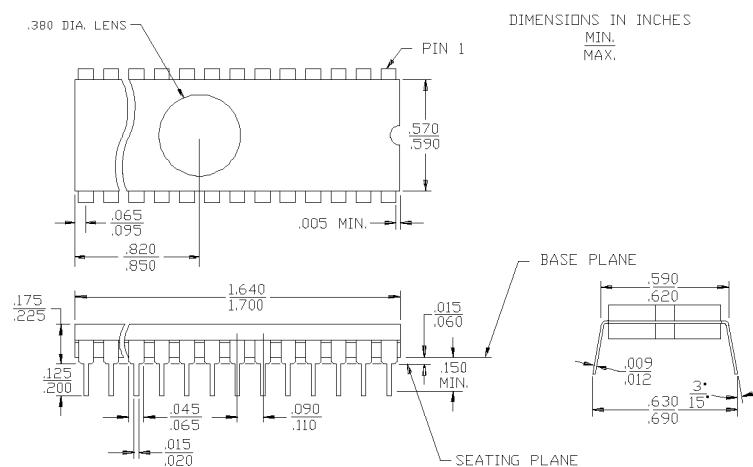
Package Diagrams (continued)

32-Lead (600-Mil) Molded DIP P19

32-Lead (600-Mil) Windowed CerDIP W20

Package Diagrams (continued)

32-Lead Thin Small Outline Package Z32

DIMENSION IN MM (INCH)
$\frac{\text{MIN.}}{\text{MAX.}}$

SEATING PLANE

PIN 1 ID

$\frac{19.80 \ (.780)}{20.20 \ (.795)}$

$\frac{18.30 \ (.720)}{18.50 \ (.728)}$

0.50 (.0197)
TYP.

$\frac{0.15 \ (.006)}{0.25 \ (.010)}$

1.20 (.047)
MAX.

$\frac{0.00 \ (.000)}{0.15 \ (.006)}$

$\frac{7.80 \ (.307)}{8.20 \ (.323)}$

$\frac{0.10 \ (.004)}{0.20 \ (.008)}$

0°–5°

$\frac{0.95 \ (.037)}{1.05 \ (.041)}$

$\frac{0.40 \ (.016)}{0.60 \ (.024)}$

0.30 (.012)
MAX.

DAMBAR PROTRUSION