

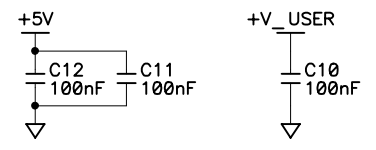
FROM MOTHERBOARD

J2	AGND	1	GND
	D0	2	D0
	D1	3	
	D2	4	
	D3	5	
	D4	6	
	D5	7	
	D6	8	
	D7	9	
	A0	10	A0
	A1	11	A1
	A2	12	A2
	A3	13	
	/IORD	14	/IOWR
	/IOWR	15	/CS
	/SELECT	16	/RESET
	INHIBIT	17	+5V
	/ATTN1	18	+V_USER
	/RESET	19	
	+5V	20	
	+3.3V	21	
	+V_USER	22	
	TX	23	
	RX	24	
	SCLK	25	
	GND	26	

REVISION HISTORY			REVISION APPROVAL			
REV	ECO	DESCRIPTION	PROJECT ENGINEER	APPROVAL DATE	DOCUMENT CONTROL	APPROVAL DATE
A	E11217	INITIAL RELEASE	DM	11/20/01	KIS	7/17/01
B	E11564	CHANGED PE7 TO OUTPUT INHIBIT	DM	28JUN01	KIS	7/17/01
C	E11715	CORRECTED REL2COM TO REL2NO ON J1 PIN 14.	DM	11/2/01	KIS	11/1/01

TABLE A

REF DES	DEVICE	DEVICE VOLTAGE INFORMATION					DEVICE: FILTER CAP REF DES(S)
		AGND	GND	+5V	+V_USER	NO CONNECTS	
U1	7812						
U2	LM311		4		8		C10
U3	74AHC32		3	5			C11
U4	74HC259		8	16			C12

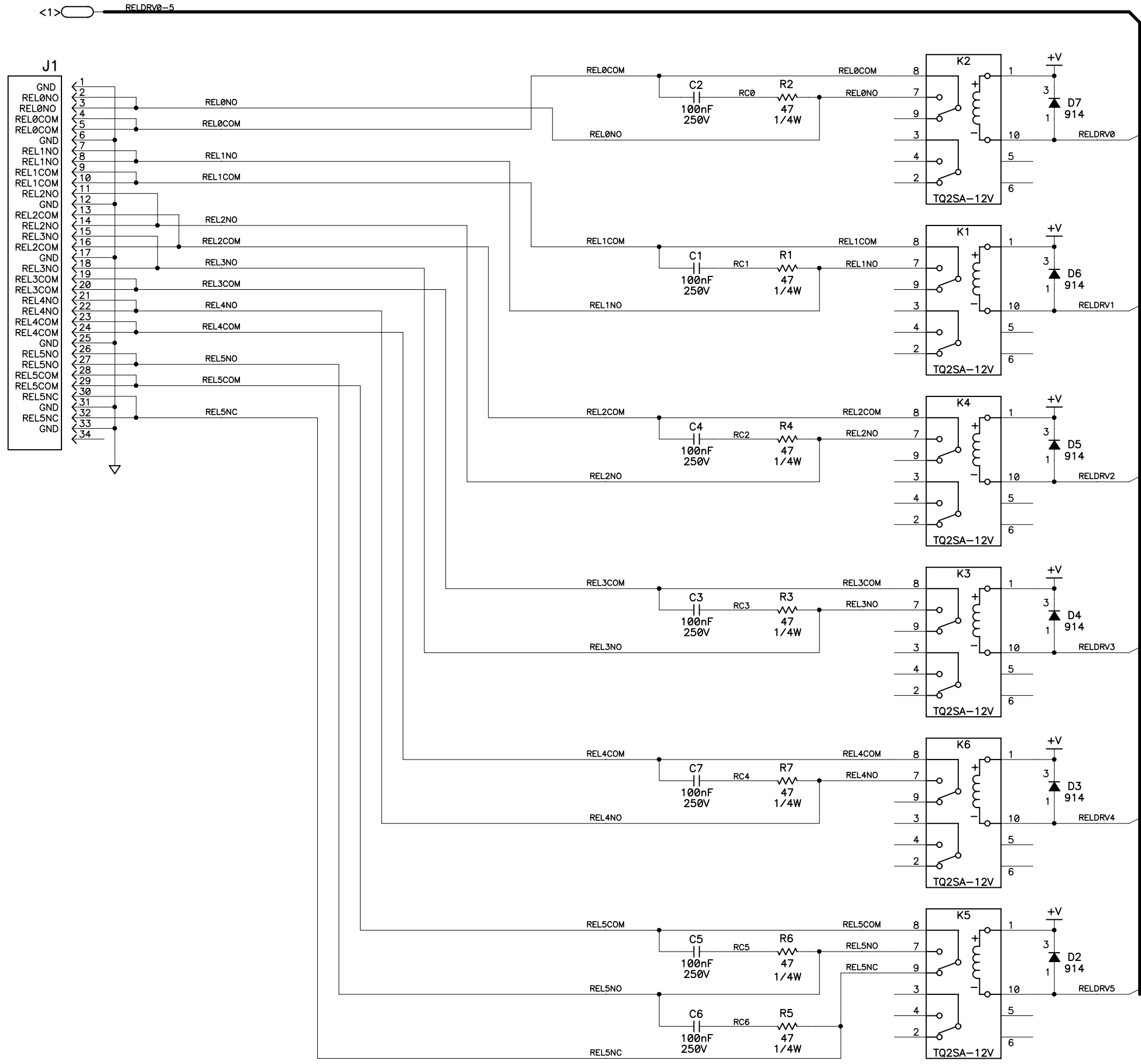


- NOTES: UNLESS OTHERWISE SPECIFIED;
1. ALL RESISTOR VALUES ARE IN OHMS, 1/10W, 5%
 2. ALL CAPACITORS ARE 50VDC OR HIGHER.
 3. THE ORIGINATION SOURCE OF A VOLTAGE IS REPRESENTED BY (VCC), AND ALL REFERENCES TO THAT VOLTAGE ARE REPRESENTED BY (VCC).

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APPEND THE FOLLOWING DOCUMENTS WHEN CHANGING THIS DOCUMENT:	DRAWING CONTENT: DRAWN BY: (INITIAL RELEASE) J.H. 26JAN00 REVISED BY: K.SCHALLER NOV1, 2001 APPROVALS: INITIAL RELEASE PROJECT ENGINEER: DARREN MUSGROVE 11/20/00 ENGINEERING MANAGER: -----		TITLE SCHEMATIC DIAGRAM SR9500 SERIES RELAY BOARD SIZE B DWG NO. 090-0098	 2900 SPAFFORD ST. DAVIS, CA 95616 530-757-4616
	SIGNATURES			
	DATE			
	SCALE NONE			
	RELEASE DATE 11/20/00			
SHEET 1 OF 2				

USER INTERFACE



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NOV1, 2001

SIZE B	DWG NO. 090-0098
SCALE NONE	REV LTR
SHEET 2 OF 2	