

MOSFET - Power, Single N-Channel

60 V, 5.3 mΩ, 89 A

NVTYS005N06CL

Features

- Small Footprint (3.3 x 3.3 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter | Symbol | Value | Unit | |
|---|--|---------------------------|------------------|---|
| Drain-to-Source Voltage | V_{DSS} | 60 | V | |
| Gate-to-Source Voltage | V_{GS} | ± 20 | V | |
| Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3, 4) | Steady State | $T_C = 25^\circ\text{C}$ | 89 | A |
| | | $T_C = 100^\circ\text{C}$ | 63 | |
| Power Dissipation $R_{\theta JC}$ (Notes 1, 2, 3) | Steady State | $T_C = 25^\circ\text{C}$ | 76 | W |
| | | $T_C = 100^\circ\text{C}$ | 38 | |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3, 4) | Steady State | $T_A = 25^\circ\text{C}$ | 18 | A |
| | | $T_A = 100^\circ\text{C}$ | 13 | |
| Power Dissipation $R_{\theta JA}$ (Notes 1, 3) | Steady State | $T_A = 25^\circ\text{C}$ | 3.2 | W |
| | | $T_A = 100^\circ\text{C}$ | 1.6 | |
| Pulsed Drain Current | $T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$ | I_{DM} | 430 | A |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | -55 to +175 | $^\circ\text{C}$ | |
| Source Current (Body Diode) | I_S | 63 | A | |
| Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 4.9 \text{ A}$) | E_{AS} | 155 | mJ | |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | T_L | 260 | $^\circ\text{C}$ | |

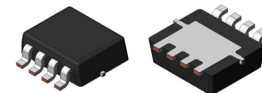
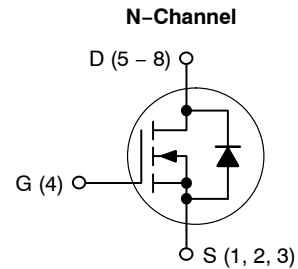
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

| Parameter | Symbol | Value | Unit |
|---|-----------------|-------|---------------------------|
| Junction-to-Case - Steady State (Note 3) | $R_{\theta JC}$ | 2.0 | $^\circ\text{C}/\text{W}$ |
| Junction-to-Ambient - Steady State (Note 3) | $R_{\theta JA}$ | 46.7 | |

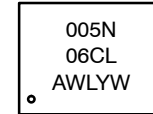
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

| $V_{(BR)DSS}$ | $R_{DS(on)} \text{ MAX}$ | $I_D \text{ MAX}$ |
|---------------|--------------------------|-------------------|
| 60 V | 5.3 mΩ @ 10 V | 89 A |
| | 7.3 mΩ @ 4.5 V | |



LFPAK8
3.3x3.3
CASE 760AD

MARKING DIAGRAM



005N06CL = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--------|----------------|-----|-----|-----|------|
|-----------|--------|----------------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|-----------------------------------|----------------------|--|------------------------|--|-----|----|
| Drain-to-Source Breakdown Voltage | V _{(BR)DSS} | V _{GS} = 0 V, I _D = 250 μA | 60 | | | V |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{GS} = 0 V, V _{DS} = 60 V | T _J = 25°C | | 10 | μA |
| | | | T _J = 125°C | | 250 | |
| Gate-to-Source Leakage Current | I _{GSS} | V _{DS} = 0 V, V _{GS} = 20 V | | | 100 | nA |

ON CHARACTERISTICS (Note 5)

| | | | | | | |
|-------------------------------|---------------------|--|-----|-----|-----|----|
| Gate Threshold Voltage | V _{GS(TH)} | V _{GS} = V _{DS} , I _D = 75 μA | 1.2 | | 2.2 | V |
| Drain-to-Source On Resistance | R _{DS(on)} | V _{GS} = 10 V, I _D = 50 A | | 4.4 | 5.3 | mΩ |
| | | V _{GS} = 4.5 V, I _D = 50 A | | 6.1 | 7.3 | |
| Forward Transconductance | g _{FS} | V _{DS} = 5 V, I _D = 50 A | | 100 | | S |

CHARGES AND CAPACITANCES

| | | | | | | |
|------------------------------|---------------------|--|--|------|--|----|
| Input Capacitance | C _{iss} | V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V | | 1890 | | pF |
| Output Capacitance | C _{oss} | | | 1060 | | |
| Reverse Transfer Capacitance | C _{rss} | | | 11 | | |
| Total Gate Charge | Q _{G(TOT)} | V _{GS} = 4.5 V, V _{DS} = 48 V, I _D = 50 A | | 11.5 | | nC |
| Threshold Gate Charge | Q _{G(TH)} | | | 2.7 | | |
| Gate-to-Source Charge | Q _{GS} | | | 5.3 | | |
| Gate-to-Drain Charge | Q _{GD} | | | 2.9 | | |
| Total Gate Charge | Q _{G(TOT)} | V _{GS} = 10 V, V _{DS} = 48 V, I _D = 50 A | | 25 | | nC |

SWITCHING CHARACTERISTICS (Note 6)

| | | | | | | |
|---------------------|---------------------|---|--|----|--|----|
| Turn-On Delay Time | t _{d(on)} | V _{GS} = 4.5 V, V _{DS} = 48 V, I _D = 50 A, R _G = 2.5 Ω | | 15 | | ns |
| Rise Time | t _r | | | 9 | | |
| Turn-Off Delay Time | t _{d(off)} | | | 19 | | |
| Fall Time | t _f | | | 8 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | | |
|-------------------------|-----------------|---|------------------------|----|-----|-----|----|
| Forward Diode Voltage | V _{SD} | V _{GS} = 0 V, I _S = 50 A | T _J = 25°C | | 0.9 | 1.2 | V |
| | | | T _J = 125°C | | 0.8 | | |
| Reverse Recovery Time | t _{RR} | V _{GS} = 0 V, di _S /dt = 100 A/μs, I _S = 50 A | | 43 | | ns | |
| Charge Time | t _a | | | 14 | | | |
| Discharge Time | t _b | | | 29 | | | |
| Reverse Recovery Charge | Q _{RR} | | | 32 | | | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

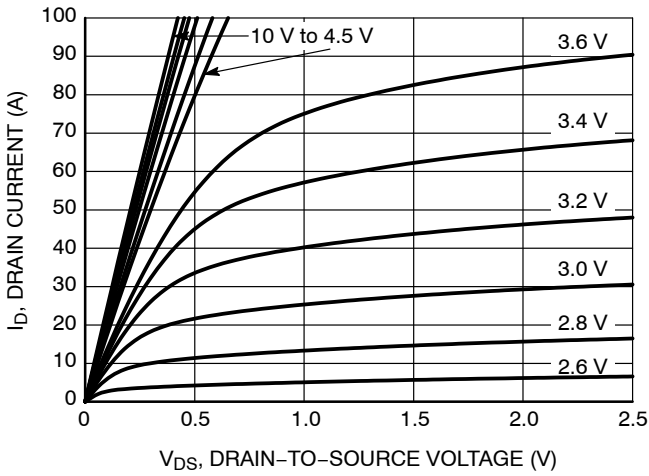


Figure 1. On-Region Characteristics

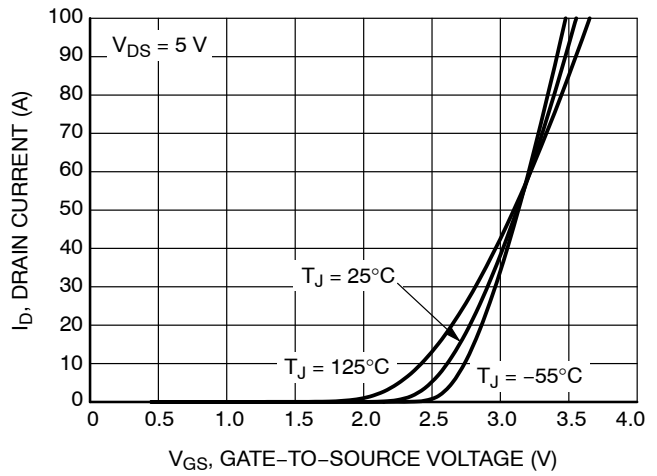


Figure 2. Transfer Characteristics

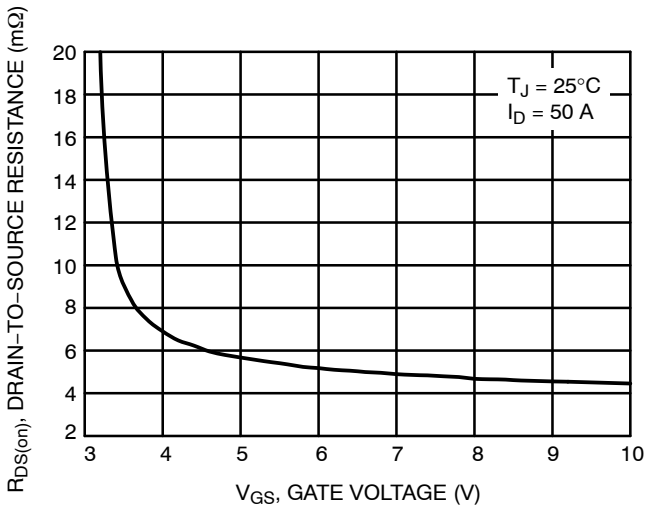


Figure 3. On-Resistance vs. Gate-to-Source Voltage

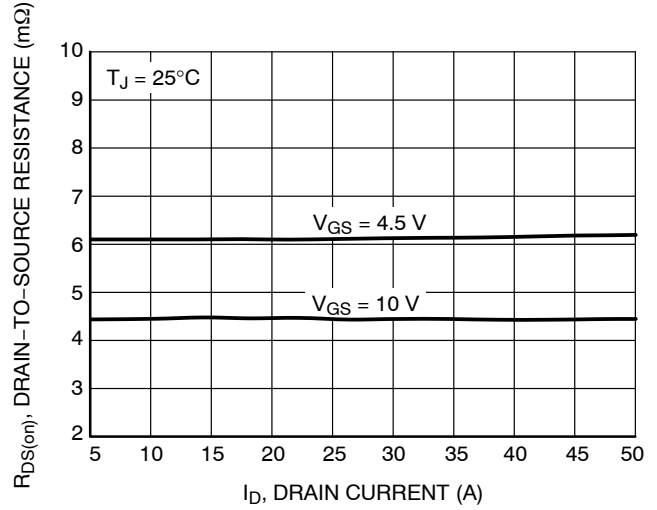


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

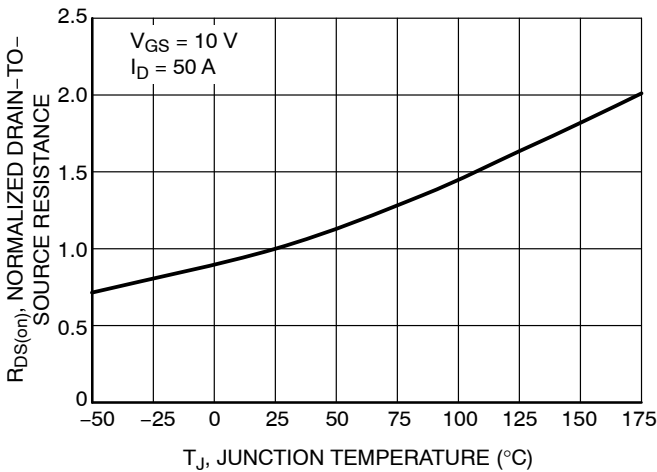


Figure 5. On-Resistance Variation with Temperature

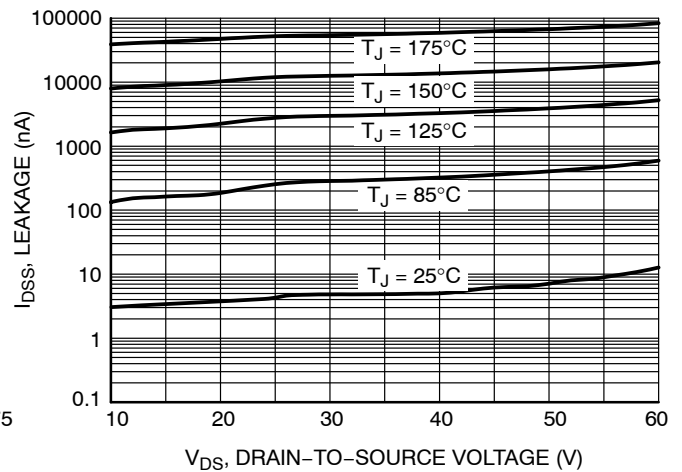


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

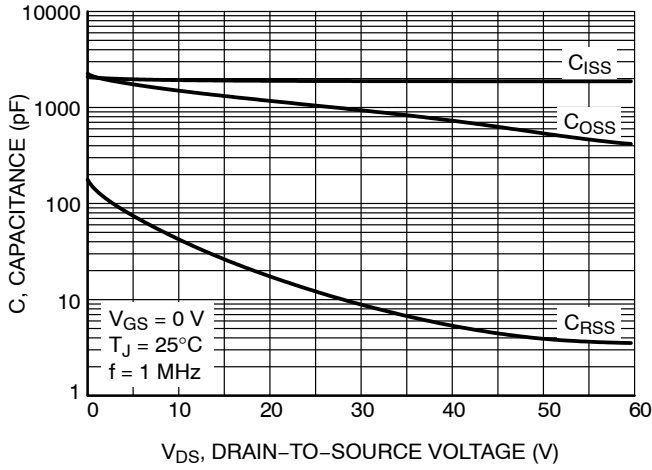


Figure 7. Capacitance Variation

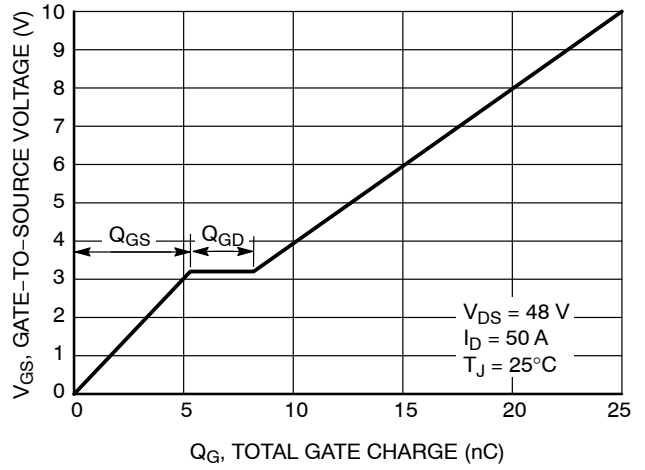


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

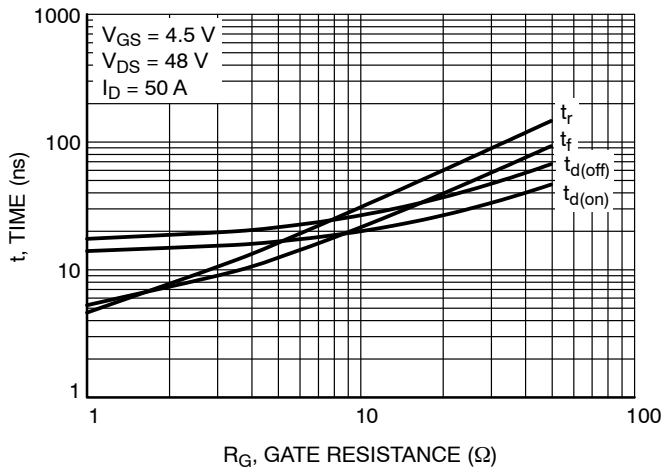


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

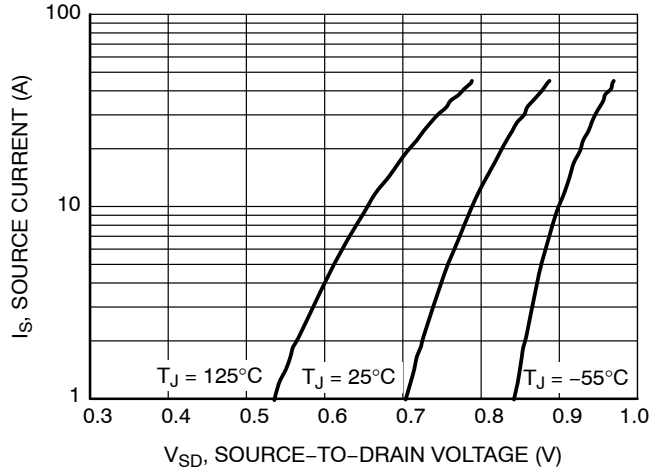


Figure 10. Diode Forward Voltage vs. Current

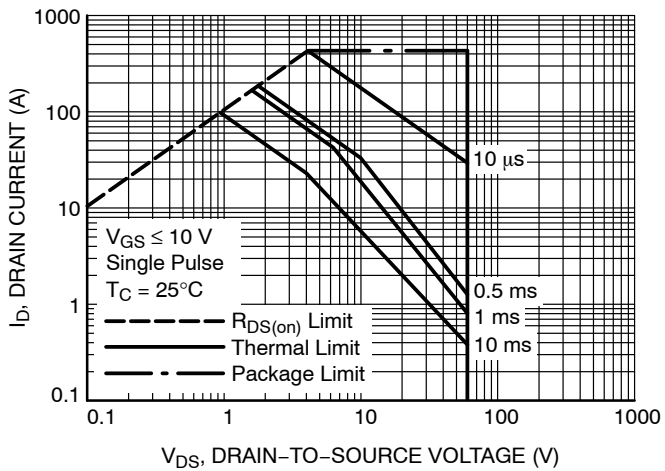


Figure 11. Maximum Rated Forward Biased Safe Operating Area

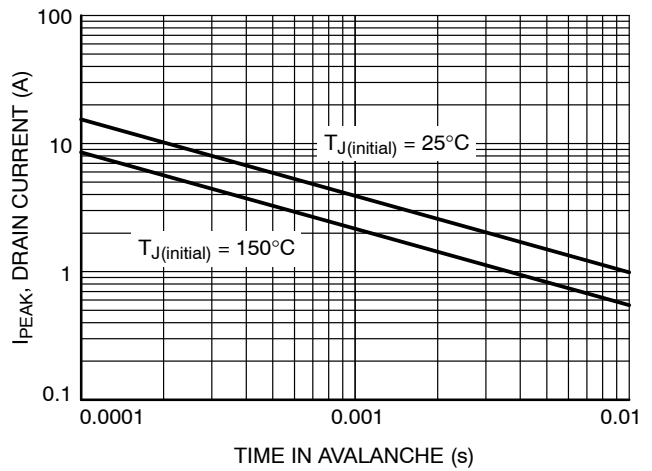


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

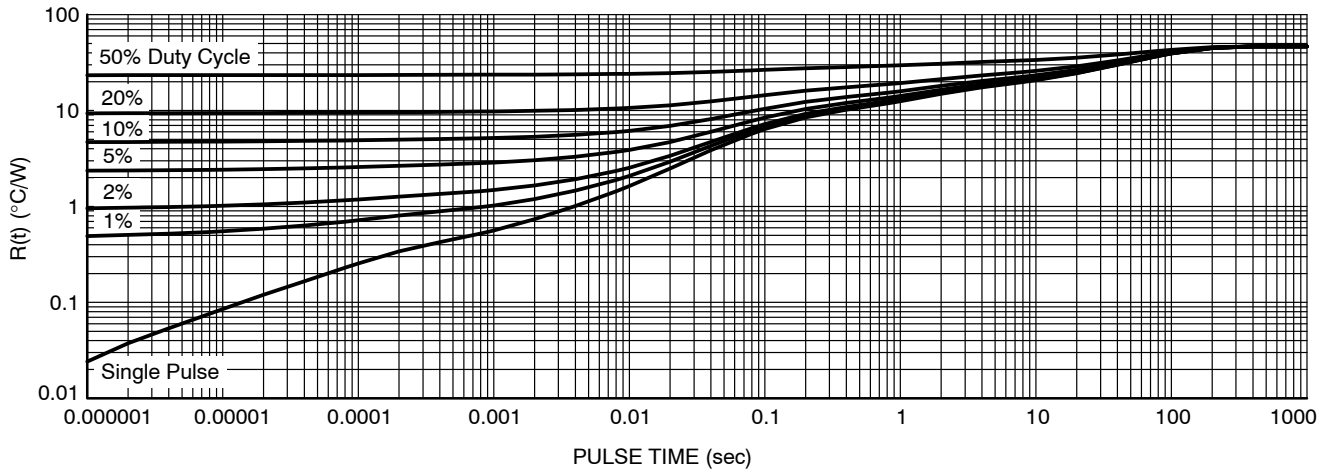


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

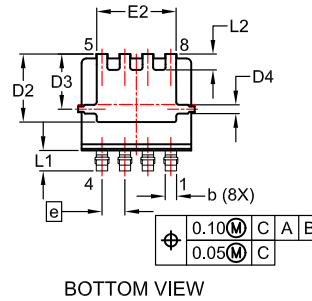
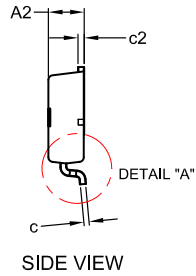
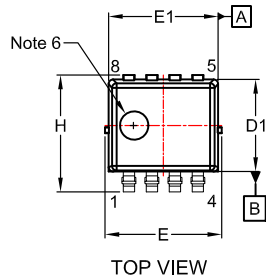
| Device | Marking | Package | Shipping [†] |
|------------------|--------------|----------------------|-----------------------|
| NVTYS005N06CLTWG | 005N 06CL | LFPAK33 (Pb-Free) | 3000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

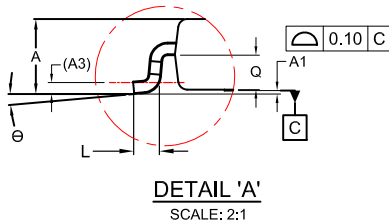
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PACKAGE DIMENSIONS

LFPAK8 3.3x3.3, 0.65P CASE 760AD ISSUE E

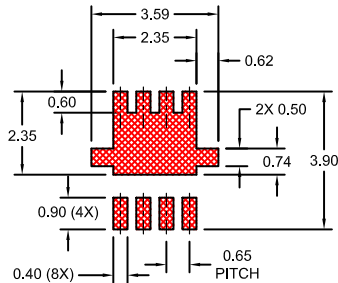


| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.95 | 1.05 | 1.15 |
| A1 | 0.00 | 0.05 | 0.10 |
| A2 | 0.95 | 1.00 | 1.05 |
| A3 | 0.15 REF | | |
| b | 0.27 | 0.32 | 0.37 |
| c | 0.12 | 0.17 | 0.22 |
| c2 | 0.12 | 0.17 | 0.22 |
| D1 | 2.50 | 2.60 | 2.70 |
| D2 | 1.82 | 1.92 | 2.02 |
| D3 | 1.46 | 1.56 | 1.66 |
| D4 | 0.20 | 0.25 | 0.30 |
| E | 3.20 | 3.30 | 3.40 |
| E1 | 3.00 | 3.10 | 3.20 |
| E2 | 2.15 | 2.25 | 2.35 |
| e | 0.65 BSC | | |
| H | 3.20 | 3.30 | 3.40 |
| L | 0.25 | 0.37 | 0.50 |
| L1 | 0.48 | 0.58 | 0.68 |
| L2 | 0.35 | 0.45 | 0.55 |
| Q | 0.45 | 0.50 | 0.55 |
| Θ | 0° | 4° | 8° |



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS OR BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
6. OPTIONAL MOLD FEATURE.



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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