

Preliminary Data

# HiPerFET™ Power MOSFET

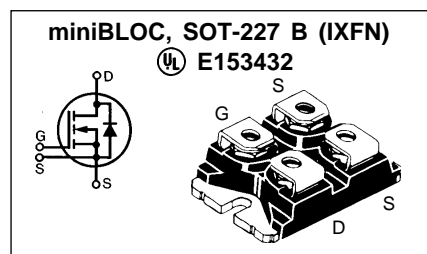
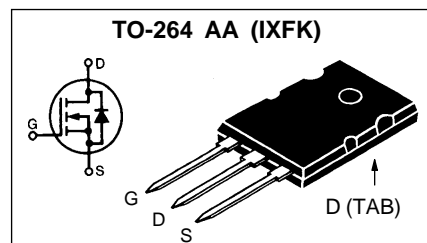
N-Channel Enhancement Mode

Avalanche Rated, High dv/dt, Low  $t_{rr}$

	$V_{DSS}$	$I_{D25}$	$R_{DS(on)}$	$t_{rr}$
IXFK/FN 36N60	600V	36A	0.18Ω	250ns
IXFK/FN 32N60	600V	32A	0.25Ω	250ns

Symbol	Test Conditions	Maximum Ratings			
		IXFK	IXFN		
$V_{DSS}$	$T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$	600	600		V
$V_{DGR}$	$T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$ ; $R_{GS} = 1\text{ M}\Omega$	600	600		V
$V_{GS}$	Continuous	±20	±20		V
$V_{GSM}$	Transient	±30	±30		V
$I_{D25}$	$T_C = 25^\circ\text{C}$ , Chip capability	32N60	32	32	A
		36N60	36	36	A
$I_{DM}$	$T_C = 25^\circ\text{C}$ , pulse width limited by $T_{JM}$	32N60	128	128	A
		36N60	144	144	A
$I_{AR}$	$T_C = 25^\circ\text{C}$	20	20		A
$E_{AR}$	$T_C = 25^\circ\text{C}$	30	30		mJ
$dv/dt$	$I_S \leq I_{DM}$ , $di/dt \leq 100\text{ A}/\mu\text{s}$ , $V_{DD} \leq V_{DSS}$ $T_J \leq 150^\circ\text{C}$ , $R_G = 2\ \Omega$	5	5		V/ns
$P_D$	$T_C = 25^\circ\text{C}$	500	520		W
$T_J$		-55 ...	+150		$^\circ\text{C}$
$T_{JM}$			150		$^\circ\text{C}$
$T_{stg}$		-55 ...	+150		$^\circ\text{C}$
$T_L$	1.6 mm (0.063 in) from case for 10 s	300	-		$^\circ\text{C}$
$V_{ISOL}$	50/60 Hz, RMSt = 1 min $I_{ISOL} \leq 1\text{ mA}$ at 1 s	-	2500		V~
		-	3000		V~
$M_d$	Mounting torque	0.9/6	1.5/13		Nm/lb.in.
	Terminal connection torque	-	1.5/13		Nm/lb.in.
<b>Weight</b>		10	30		g

Symbol	Test Conditions	Characteristic Values		
		$(T_J = 25^\circ\text{C}$ , unless otherwise specified)		
		Min.	Typ.	Max.
$V_{DSS}$	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	600		V
$V_{GH(th)}$	$V_{DS} = V_{GS}$ , $I_D = 8\text{ mA}$	2		4.5 V
$I_{GSS}$	$V_{GS} = \pm 20\text{ V}_{DC}$ , $V_{DS} = 0$			±200 nA
$I_{DSS}$	$V_{DS} = 0.8\text{ V}_{DSS}$ $V_{GS} = 0\text{ V}$	$T_J = 25^\circ\text{C}$		400 $\mu\text{A}$
		$T_J = 125^\circ\text{C}$		2 mA
$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 0.5\text{ I}_{D25}$ Pulse test, $t \leq 300\ \mu\text{s}$ , duty cycle $\leq 2\%$	36N60		0.18 $\Omega$
		32N60		0.25 $\Omega$



G = Gate      D = Drain  
S = Source      TAB = Drain  
Either Source terminal at miniBLOC can be used as Main or Kelvin Source

## Features

- International standard packages
- JEDEC TO-264 AA, epoxy meet UL 94 V-0, flammability classification
- miniBLOC with Aluminium nitride isolation
- Low  $R_{DS(on)}$  HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
- Fast intrinsic Rectifier

## Applications

- DC-DC converters
- Synchronous rectification
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- Temperature and lighting controls
- Low voltage relays

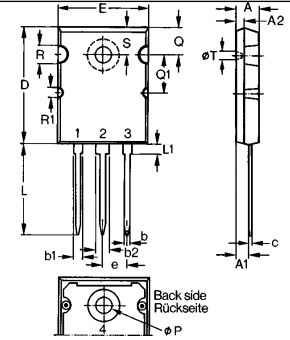
## Advantages

- Easy to mount
- Space savings
- High power density

Symbol	Test Conditions	Characteristic Values		
		(T <sub>J</sub> = 25°C, unless otherwise specified)		
		min.	typ.	max.
<b>g<sub>fs</sub></b>	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 0.5 I <sub>D25</sub> ; pulse test		36	S
<b>C<sub>iss</sub></b>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		9000	pF
<b>C<sub>oss</sub></b>			840	pF
<b>C<sub>rss</sub></b>			280	pF
<b>t<sub>d(on)</sub></b>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 0.5 V <sub>DSS</sub> ; I <sub>D</sub> = 0.5 I <sub>D25</sub> R <sub>G</sub> = 1 Ω (External),		30	ns
<b>t<sub>r</sub></b>			45	ns
<b>t<sub>d(off)</sub></b>			100	ns
<b>t<sub>f</sub></b>			60	ns
<b>Q<sub>g(on)</sub></b>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 0.5 V <sub>DSS</sub> ; I <sub>D</sub> = 0.5 I <sub>D25</sub>		325	nC
<b>Q<sub>gs</sub></b>			60	nC
<b>Q<sub>gd</sub></b>			120	nC
<b>R<sub>thJC</sub></b>	TO-264 AA		0.25	K/W
<b>R<sub>thCK</sub></b>	TO-264 AA		0.15	K/W
<b>R<sub>thJC</sub></b>	miniBLOC, SOT-227 B		0.24	K/W
<b>R<sub>thCK</sub></b>	miniBLOC, SOT-227 B		0.05	K/W

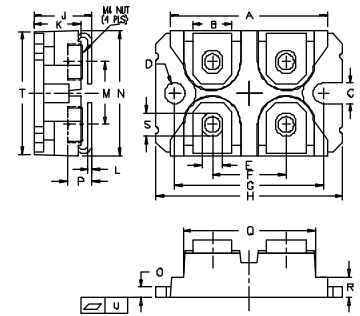
Symbol	Test Conditions	Characteristic Values		
		(T <sub>J</sub> = 25°C, unless otherwise specified)		
		Min.	Typ.	Max.
<b>I<sub>S</sub></b>	V <sub>GS</sub> = 0	36N60		36 A
<b>I<sub>S</sub></b>	V <sub>GS</sub> = 0	32N60		32 A
<b>I<sub>SM</sub></b>	Repetitive; pulse width limited by T <sub>JM</sub>	36N60		144 A
		32N60		128 A
<b>V<sub>SD</sub></b>	I <sub>F</sub> = I <sub>S</sub> A, V <sub>GS</sub> = 0 V, Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %			1.5 V
<b>t<sub>rr</sub></b>	I <sub>F</sub> = I <sub>S</sub> , -di/dt = 100 A/μs, V <sub>R</sub> = 100 V		20	ns
<b>I<sub>RM</sub></b>				

### TO-264 AA Outline



Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.82	5.13	.190	.202
A1	2.54	2.89	.100	.114
A2	2.00	2.10	.079	.083
b	1.12	1.42	.044	.056
b1	2.39	2.69	.094	.106
b2	2.90	3.09	.114	.122
c	0.53	0.83	.021	.033
D	25.91	26.16	1.020	1.030
E	19.81	19.96	.780	.786
e	5.46 BSC		.215 BSC	
J	0.00	0.25	.000	.010
K	0.00	0.25	.000	.010
L	20.32	20.83	.800	.820
L1	2.29	2.59	.090	.102
P	3.17	3.66	.125	.144
Q	6.07	6.27	.239	.247
Q1	8.38	8.69	.330	.342
R	3.81	4.32	.150	.170
R1	1.78	2.29	.070	.090
S	6.04	6.30	.238	.248
T	1.57	1.83	.062	.072

### miniBLOC, SOT-227 B



### M4 screws (4x) supplied

Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	31.50	31.88	1.240	1.255
B	7.80	8.20	0.307	0.323
C	4.09	4.29	0.161	0.169
D	4.09	4.29	0.161	0.169
E	4.09	4.29	0.161	0.169
F	14.91	15.11	0.587	0.595
G	30.12	30.30	1.186	1.193
H	38.00	38.23	1.496	1.505
J	11.68	12.22	0.460	0.481
K	8.92	9.60	0.351	0.378
L	0.76	0.84	0.030	0.033
M	12.60	12.85	0.496	0.506
N	25.15	25.42	0.990	1.001
O	1.98	2.13	0.078	0.084
P	4.95	5.97	0.195	0.235
Q	26.54	26.90	1.045	1.059
R	3.94	4.42	0.155	0.174
S	4.72	4.85	0.186	0.191
T	24.59	25.07	0.968	0.987
U	-0.05	0.1	-0.002	0.004

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592    4,881,106    5,017,508    5,049,961    5,187,117    5,486,715  
4,850,072    4,931,844    5,034,796    5,063,307    5,237,481    5,381,025

Fig.1. Output Characteristics

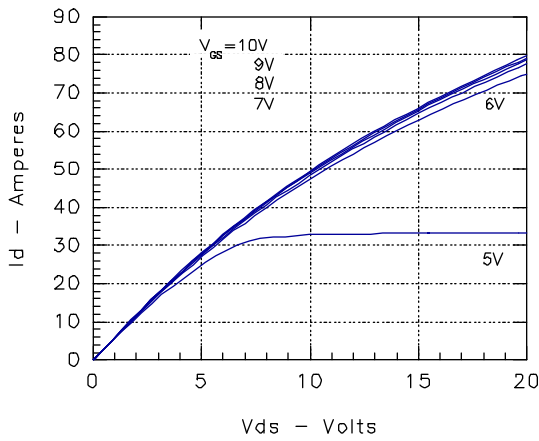


Fig. 2. Input Admittance

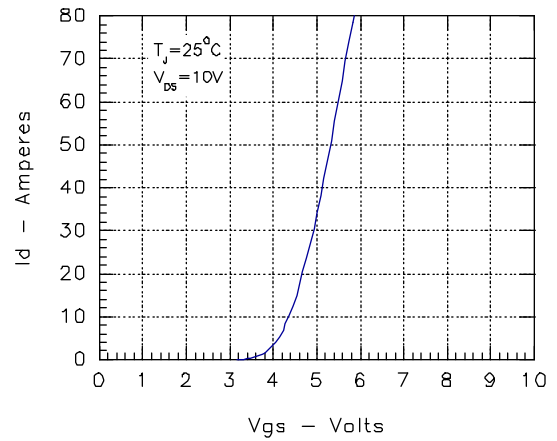


Fig. 3. Rds(on) vs. Drain Current

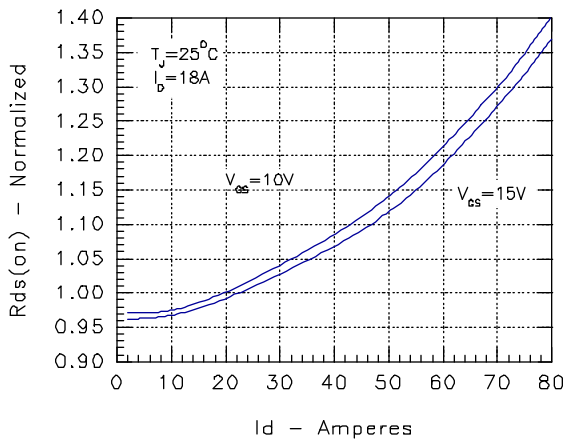


Fig. 4. Temperature Dependence of Drain to Source Resistance

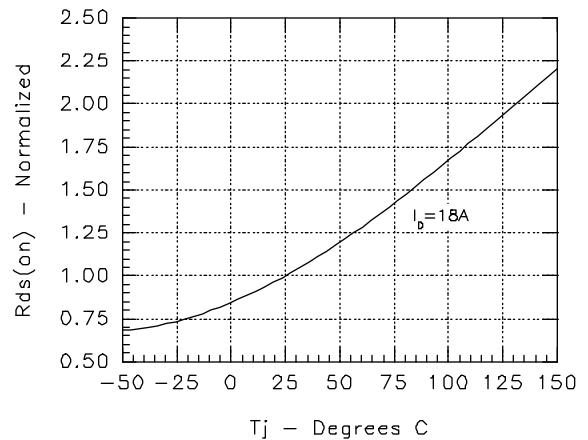


Fig. 5. Drain Current vs. Case Temperature

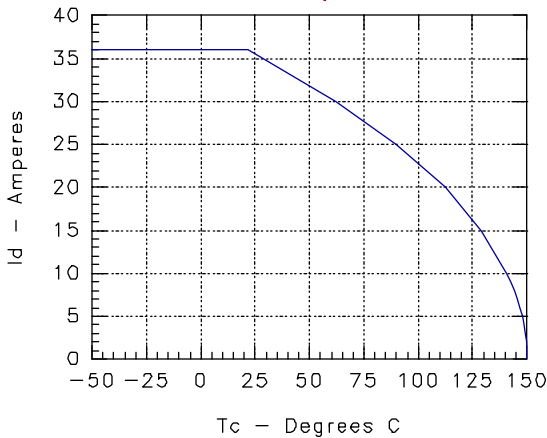
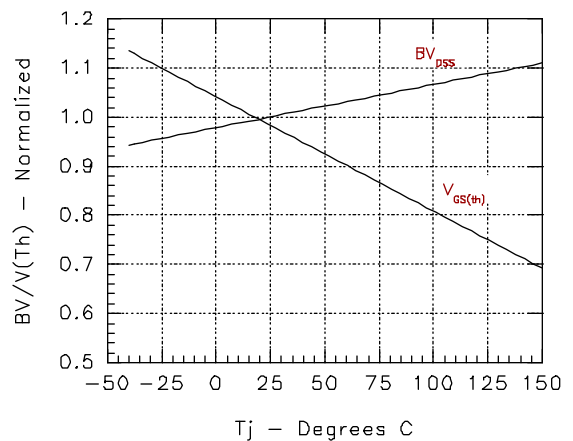


Fig. 6. Temperature Dependence of Breakdown Voltage and Threshold Voltage



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Fig. 7. Gate Charge

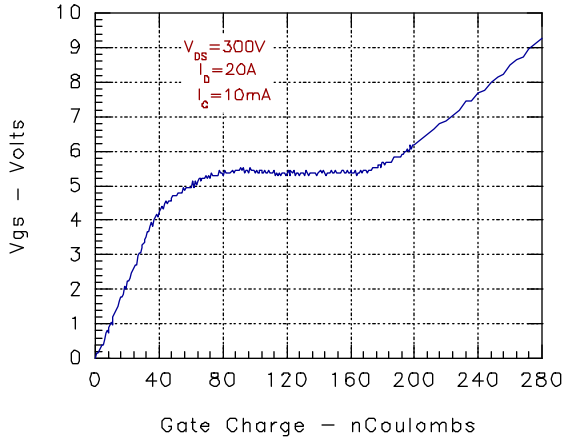


Fig. 8. Capacitance Curves

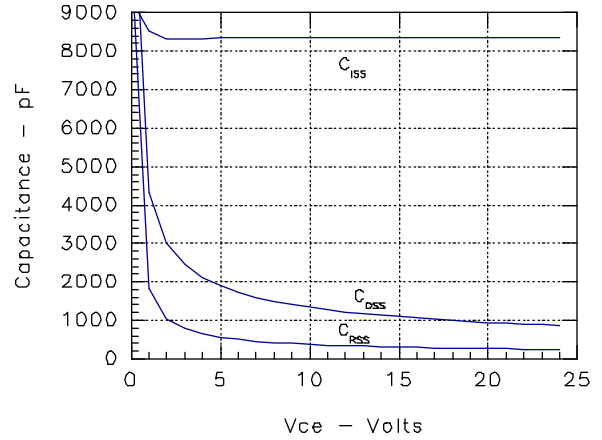


Fig. 9. Source Current vs. Source to Drain Voltage

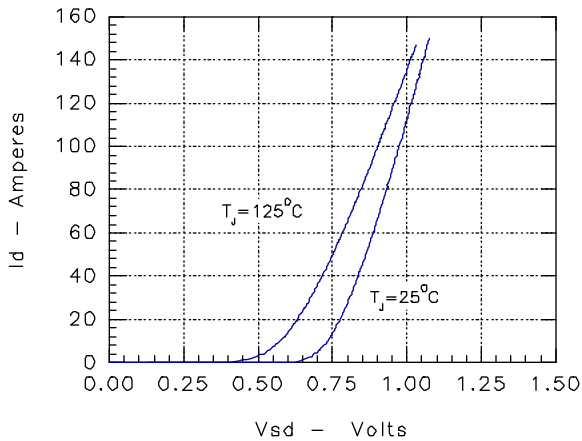
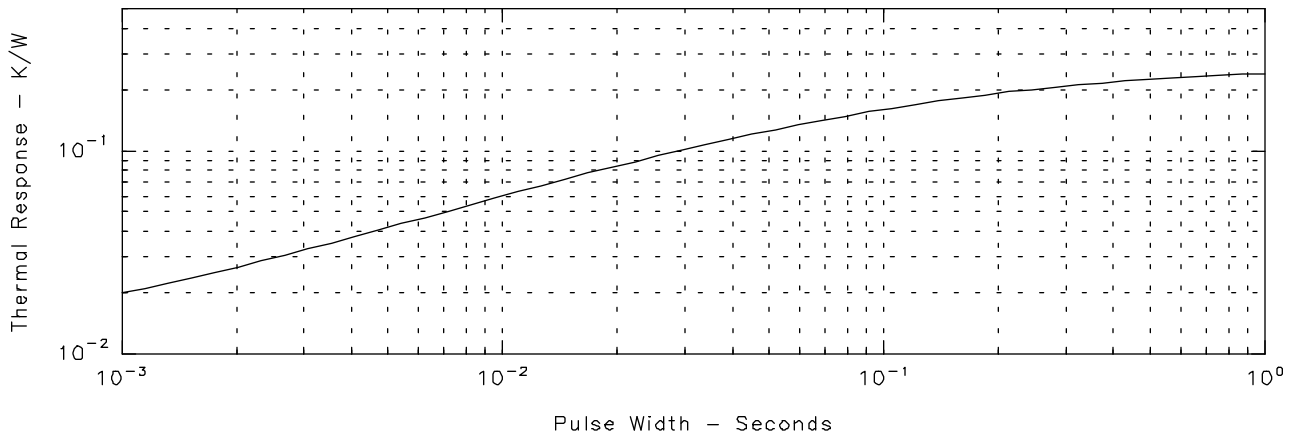


Fig. 10. Transient Thermal Impedance



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