

EMG2DXV5, EMG5DXV5

Dual Bias Resistor Transistors

NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the SOT-553 package which is designed for low power surface mount applications.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Moisture Sensitivity Level: 1
- Available in 8 mm, 7 inch Tape and Reel
- Lead-Free Solder Plating
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CB0}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	230 (Note 1) 338 (Note 2) 1.8 (Note 1) 2.7 (Note 2)	mW $^\circ\text{C}/\text{W}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	540 (Note 1) 370 (Note 2)	$^\circ\text{C}/\text{W}$
Thermal Resistance – Junction-to-Lead	$R_{\theta JL}$	264 (Note 1) 287 (Note 2)	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

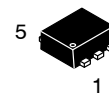
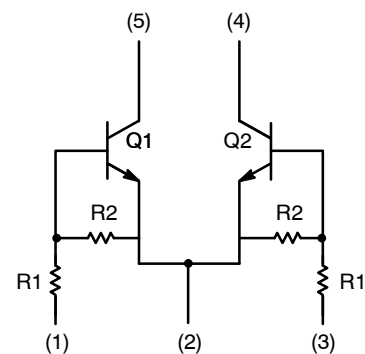
1. FR-4 @ Minimum Pad
2. FR-4 @ 1.0 x 1.0 inch Pad



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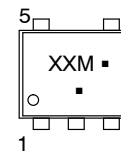
<http://onsemi.com>

NPN SILICON BIAS RESISTOR TRANSISTORS



SOT-553
CASE 463B

MARKING DIAGRAM



- XX = UF (EMG5)
UP (EMG2)
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

EMG2DXV5, EMG5DXV5

DEVICE MARKING AND RESISTOR VALUES

Device	Package	Marking	R1 (K)	R2 (K)
EMG2DXV5	SOT-553	UP	47	47
EMG5DXV5	SOT-553	UF	10	47

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS (Q1 & Q2)

Collector-Base Cutoff Current ($V_{CB} = 50\text{ V}$, $I_E = 0$)	I_{CBO}	-	-	100	nA _{dc}
Collector-Emitter Cutoff Current ($V_{CE} = 50\text{ V}$, $I_B = 0$)	I_{CEO}	-	-	500	nA _{dc}
Emitter-Base Cutoff Current ($V_{EB} = 6.0\text{ V}$, $I_C = 0$)	I_{EBO}	-	-	0.1	mA _{dc}
		-	-	0.2	
Collector-Base Breakdown Voltage ($I_C = 10\ \mu\text{A}$, $I_E = 0$)	$V_{(BR)CBO}$	50	-	-	V _{dc}
Collector-Emitter Breakdown Voltage (Note 3) ($I_C = 2.0\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	50	-	-	V _{dc}

ON CHARACTERISTICS (Q1 & Q2) (Note 3)

DC Current Gain ($V_{CE} = 10\text{ V}$, $I_C = 5.0\text{ mA}$)	EMG2DXV5 EMG5DXV5	h_{FE}	80 80	140 140	- -	
Collector-Emitter Saturation Voltage ($I_C = 10\text{ mA}$, $I_B = 0.3\text{ mA}$)		$V_{CE(sat)}$	-	-	0.25	V _{dc}
Output Voltage (on) ($V_{CC} = 5.0\text{ V}$, $V_B = 3.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	EMG2DXV5	V_{OL}	-	-	0.2	V _{dc}
($V_{CC} = 5.0\text{ V}$, $V_B = 2.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	EMG5DXV5		-	-	0.2	
Output Voltage (off) ($V_{CC} = 5.0\text{ V}$, $V_B = 0.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$)		V_{OH}	4.9	-	-	V _{dc}
Input Resistor	EMG2DXV5 EMG5DXV5	R_1	32.9 7.0	47 10	61.1 13	k Ω
Resistor Ratio	EMG2DXV5 EMG5DXV5	R_1/R_2	0.8 0.17	1.0 0.21	1.2 0.25	

3. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

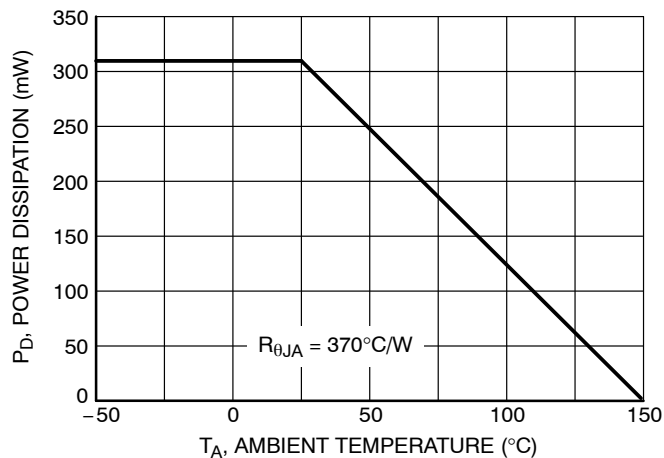


Figure 1. Derating Curve

EMG2DXV5, EMG5DXV5

TYPICAL ELECTRICAL CHARACTERISTICS — EMG2DXV5

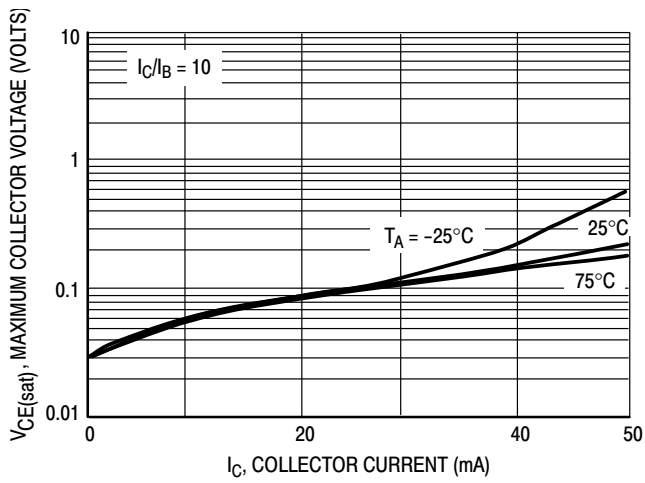


Figure 2. $V_{CE(sat)}$ versus I_C

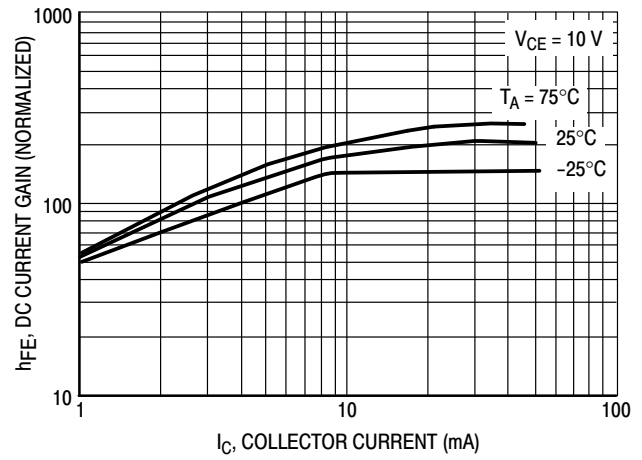


Figure 3. DC Current Gain

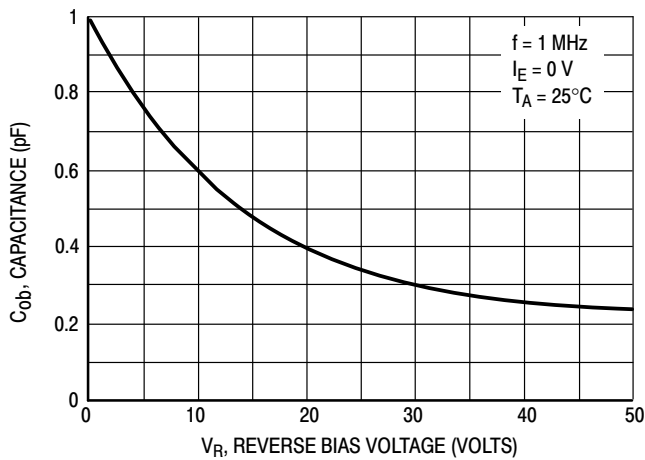


Figure 4. Output Capacitance

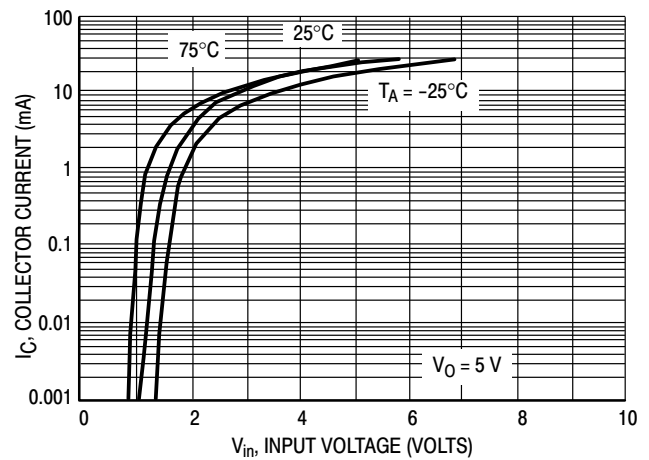


Figure 5. Output Current versus Input Voltage

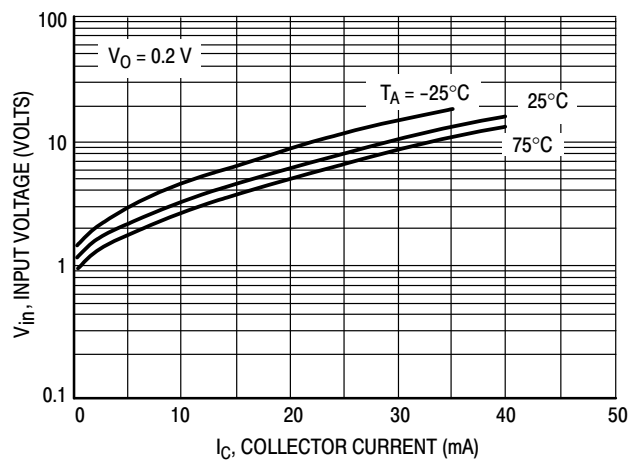


Figure 6. Input Voltage versus Output Current

EMG2DXV5, EMG5DXV5

TYPICAL ELECTRICAL CHARACTERISTICS – EMG5DXV5

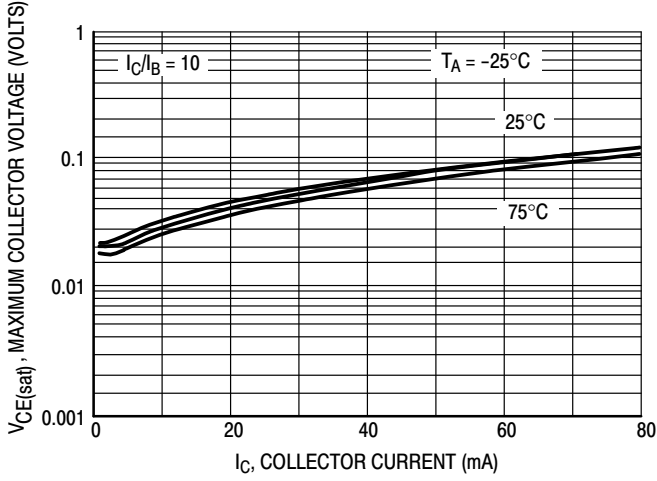


Figure 7. $V_{CE(sat)}$ versus I_C

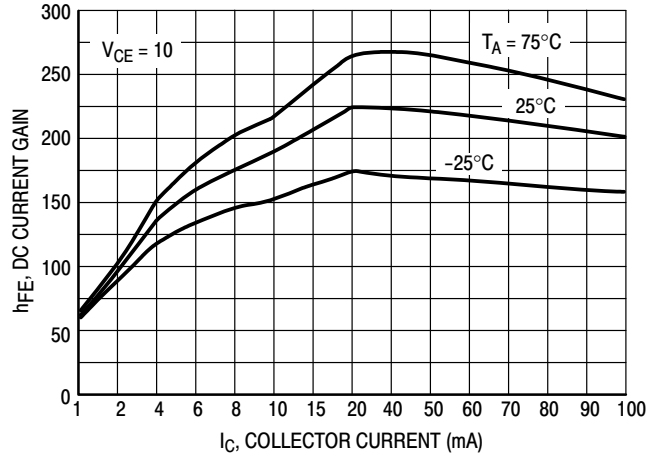


Figure 8. DC Current Gain

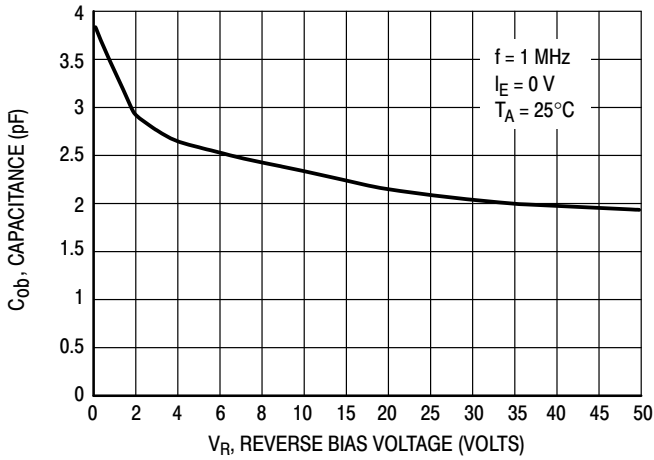


Figure 9. Output Capacitance

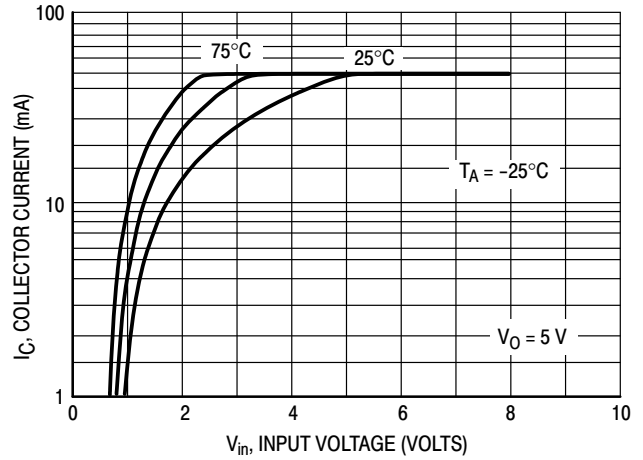


Figure 10. Output Current versus Input Voltage

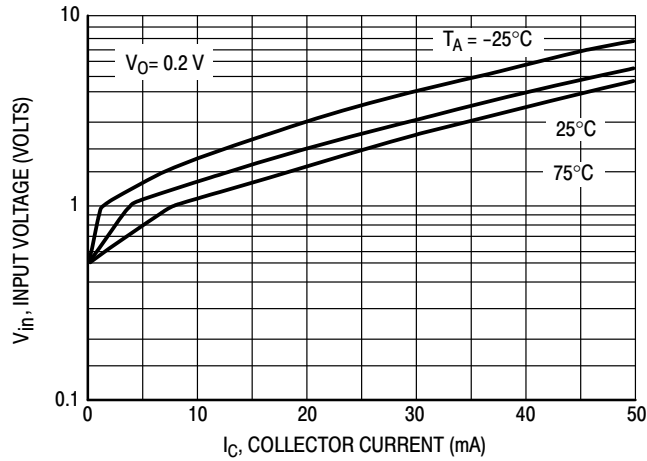


Figure 11. Input Voltage versus Output Current

EMG2DXV5, EMG5DXV5

TYPICAL APPLICATIONS FOR NPN BRTs

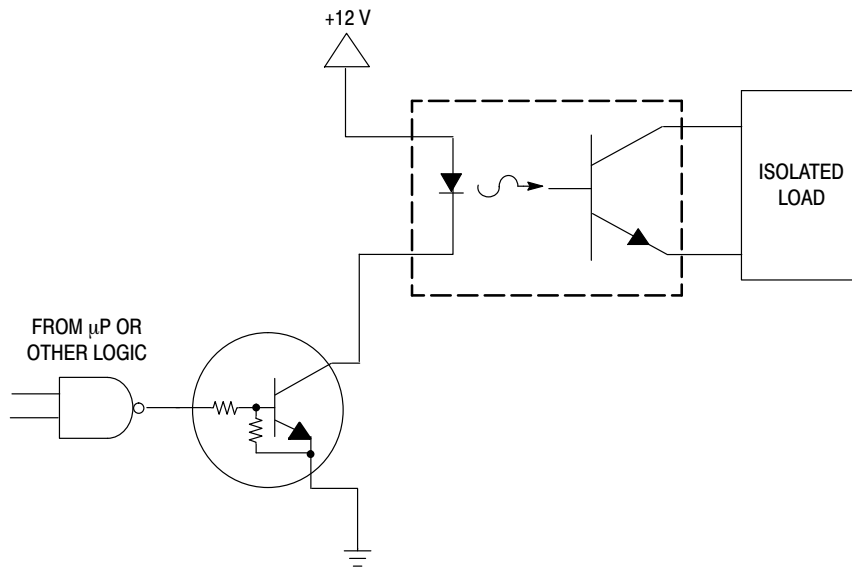


Figure 12. Level Shifter: Connects 12 or 24 Volt Circuits to Logic

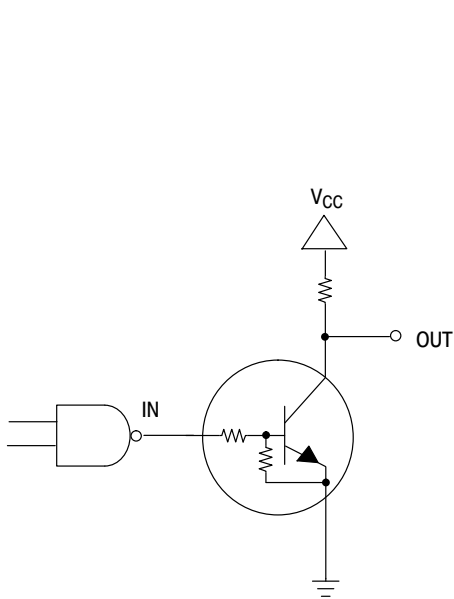


Figure 13. Open Collector Inverter: Inverts the Input Signal

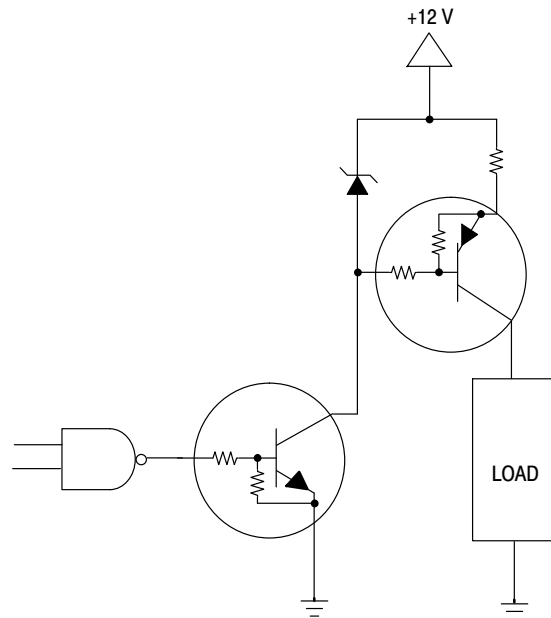


Figure 14. Inexpensive, Unregulated Current Source

EMG2DXV5, EMG5DXV5

DEVICE ORDERING INFORMATION

Device	Package	Shipping [†]
EMG2DXV5T1G	SOT-553 (Pb-Free)	4000 / Tape & Reel
EMG2DXV5T5G	SOT-553 (Pb-Free)	8000 / Tape & Reel
EMG5DXV5T1G	SOT-553 (Pb-Free)	4000 / Tape & Reel
EMG5DXV5T5G	SOT-553 (Pb-Free)	8000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

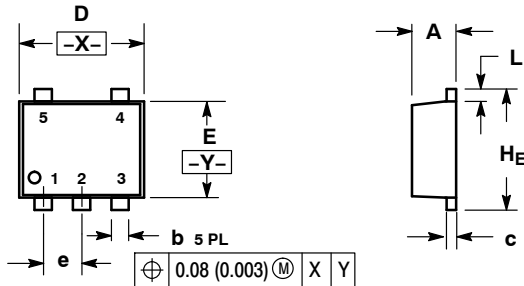
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SCALE 4:1

SOT-553, 5 LEAD CASE 463B ISSUE C

DATE 20 MAR 2013

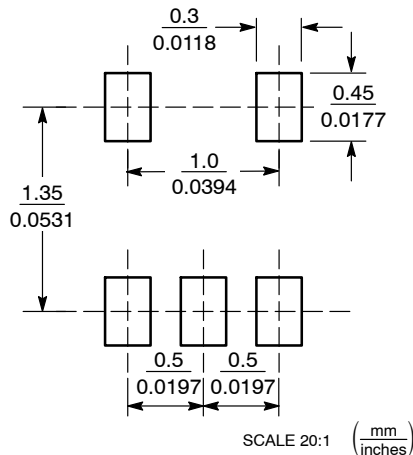


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.55	1.60	1.65	0.061	0.063	0.065
E	1.15	1.20	1.25	0.045	0.047	0.049
e	0.50 BSC			0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H _E	1.55	1.60	1.65	0.061	0.063	0.065

RECOMMENDED SOLDERING FOOTPRINT*



SCALE 20:1 ($\frac{\text{mm}}{\text{inches}}$)

GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLE 1:

- PIN 1. BASE
- 2. EMITTER
- 3. BASE
- 4. COLLECTOR
- 5. COLLECTOR

STYLE 2:

- PIN 1. CATHODE
- 2. COMMON ANODE
- 3. CATHODE 2
- 4. CATHODE 3
- 5. CATHODE 4

STYLE 3:

- PIN 1. ANODE 1
- 2. N/C
- 3. ANODE 2
- 4. CATHODE 2
- 5. CATHODE 1

STYLE 4:

- PIN 1. SOURCE 1
- 2. DRAIN 1/2
- 3. SOURCE 1
- 4. GATE 1
- 5. GATE 2

STYLE 5:

- PIN 1. ANODE
- 2. EMITTER
- 3. BASE
- 4. COLLECTOR
- 5. CATHODE

STYLE 6:

- PIN 1. EMITTER 2
- 2. BASE 2
- 3. EMITTER 1
- 4. COLLECTOR 1
- 5. COLLECTOR 2/BASE 1

STYLE 7:

- PIN 1. BASE
- 2. EMITTER
- 3. BASE
- 4. COLLECTOR
- 5. COLLECTOR

STYLE 8:

- PIN 1. CATHODE
- 2. COLLECTOR
- 3. N/C
- 4. BASE
- 5. EMITTER

STYLE 9:

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. ANODE
- 5. ANODE

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NEW STANDARD:		
DESCRIPTION:	SOT-553, 5 LEAD	PAGE 1 OF 2



ISSUE	REVISION	DATE
A	ADDED STYLES 3-9. REQ. BY D. BARLOW	11 NOV 2003
B	ADDED NOMINAL VALUES AND UPDATED GENERIC MARKING DIAGRAM. REQ. BY HONG XIAO	27 MAY 2005
C	UPDATED DIMENSIONS D, E, AND HE. REQ. BY J. LETTERMAN.	20 MAR 2013

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