National Semiconductor

T-43-21

MM54HC125/MM74HC125
MM54HC126/MM74HC126
TRI-STATE® Quad Buffers

General Description

These are general purpose TRI-STATE high speed non-inverting buffers utilizing advanced silicon-gate CMOS technology. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. Both circuits are capable of driving up to 15 low power Schottky inputs.

The MM54HC125/MM74HC125 require the TRI-STATE control input C to be taken high to put the output into the high impedance condition, whereas the MM54HC126/MM74HC126 require the control input to be low to put the output into high impedance.

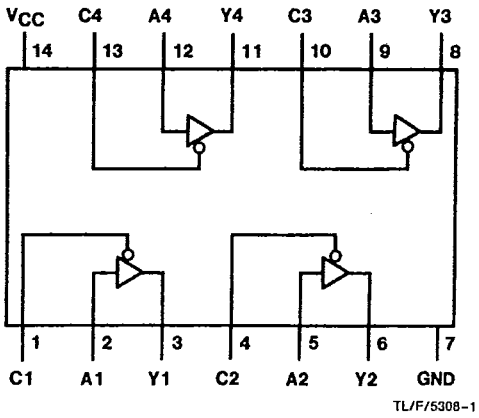
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC)
- Fanout of 15 LS-TTL loads

Connection Diagrams

Dual-In-Line Package



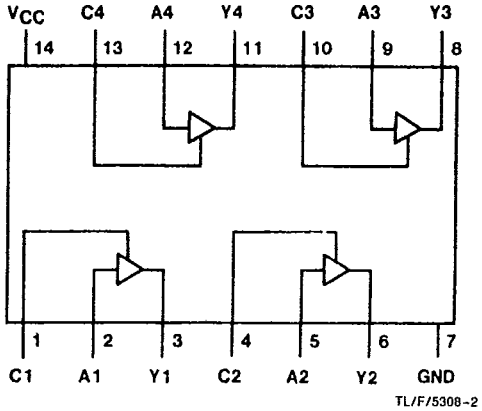
TL/F/5308–1

Top View

Order Number MM54HC125* or MM74HC125*

*Please look into Section 8, Appendix D for availability of various package types.

Dual-In-Line Package



TL/F/5308–2

Top View

Order Number MM54HC126* or MM74HC126*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Tables

Inputs		Output
A	C	Y
H	L	H
L	L	L
X	H	Z

Inputs		Output
A	C	Y
H	H	H
L	H	L
X	L	Z

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND C_n=Disabled	6.0V		±0.5	±5	±10	μA
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=45$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time		13	18	ns
t_{PZH}	Maximum Output Enable Time to High Level	$R_L=1$ kΩ	13	25	ns
t_{PHZ}	Maximum Output Disable Time from High Level	$R_L=1$ kΩ $C_L=5$ pF	17	25	ns
t_{PZL}	Maximum Output Enable Time to Low Level	$R_L=1$ kΩ	18	25	ns
t_{PLZ}	Maximum Output Disable Time from Low Level	$R_L=1$ kΩ $C_L=5$ pF	13	25	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	Temperature °C				Units
				54HC/74HC $T_A=25°C$	74HC −40 to 85°C		54HC −55 to 125°C	
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time		2.0V	40	100	125	150	ns
			4.5V	14	20	25	30	ns
			6.0V	12	17	21	25	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	$C_L=150$ pF	2.0V	35	130	163	195	ns
			4.5V	14	26	33	39	ns
			6.0V	12	22	28	33	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ	2.0V	25	125	156	188	ns
			4.5V	14	25	31	38	ns
			6.0V	12	21	26	31	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	25	125	156	188	ns
			4.5V	14	25	31	38	ns
			6.0V	12	21	26	31	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$C_L=150$ pF $R_L=1$ kΩ	2.0V	35	140	175	210	ns
			4.5V	15	28	35	42	ns
			6.0V	13	24	30	36	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	30	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{IN}	Input Capacitance			5	10	10	10	pF
C_{OUT}	Output Capacitance Outputs			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)						
		Enabled		45				pF
		Disabled		6				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

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