

**BATTERY PROTECTION IC  
WITH CHARGE-DISCHARGE CONTROL FUNCTION  
FOR 1-CELL PACK**

The S-82K1A Series is a protection IC for lithium-ion / lithium polymer rechargeable batteries, which includes high-accuracy voltage detection circuits and delay circuits. It is suitable for protecting 1-cell lithium-ion / lithium polymer rechargeable battery packs from overcharge, overdischarge, and overcurrent.

By using an external overcurrent detection resistor, the S-82K1A Series realizes high-accuracy overcurrent protection with less effect from temperature change.

The S-82K1A Series also has an input pin for charge-discharge control signal, allowing for charge-discharge control with an external signal.

## ■ Features

- High-accuracy voltage detection circuit
 

|   |                                    |                       |
|---|------------------------------------|-----------------------|
| Overcharge detection voltage              | 3.500 V to 4.600 V (5 mV step)     | Accuracy $\pm 15$ mV  |
| Overcharge release voltage                | 3.100 V to 4.600 V <sup>*1</sup>   | Accuracy $\pm 50$ mV  |
| Overdischarge detection voltage           | 2.000 V to 3.000 V (10 mV step)    | Accuracy $\pm 50$ mV  |
| Overdischarge release voltage             | 2.000 V to 3.400 V <sup>*2</sup>   | Accuracy $\pm 75$ mV  |
| Discharge overcurrent detection voltage 1 | 0.003 V to 0.100 V (0.5 mV step)   | Accuracy $\pm 1.0$ mV |
| Discharge overcurrent detection voltage 2 | 0.010 V to 0.100 V (1 mV step)     | Accuracy $\pm 3$ mV   |
| Load short-circuiting detection voltage   | 0.020 V to 0.100 V (1 mV step)     | Accuracy $\pm 5$ mV   |
| Charge overcurrent detection voltage      | -0.100 V to -0.003 V (0.5 mV step) | Accuracy $\pm 1.0$ mV |
- Detection delay times are generated only by an internal circuit (external capacitors are unnecessary).
- Charge-discharge control function
 

|                                    |   |
|------------------------------------|---|
| CTL pin control logic:             | Active "H", active "L"                            |
| CTL pin internal resistance:       | Pull-up, pull-down                                |
| CTL pin internal resistance value: | 1 M $\Omega$ to 10 M $\Omega$ (1 M $\Omega$ step) |
- Discharge overcurrent control function
 

|  |                                       |
|--|---------------------------------------|
| Release condition of discharge overcurrent status: | Load disconnection                    |
| Release voltage of discharge overcurrent status:   | $V_{RIOV} = V_{DD} \times 0.8$ (typ.) |
- Discharge overcurrent status reset function by CTL pin: Available, unavailable
- 0 V battery charge: Enabled, inhibited
- Power-down function: Available, unavailable
- High-withstand voltage: VM pin and CO pin: Absolute maximum rating 28 V
- Wide operation temperature range: Ta = -40°C to +85°C
- Low current consumption
 

|                       |   |
|-----------------------|---|
| During operation:     | 2.0 $\mu$ A typ., 4.0 $\mu$ A max. (Ta = +25°C) |
| During power-down:    | 50 nA max. (Ta = +25°C)                         |
| During overdischarge: | 0.5 $\mu$ A max. (Ta = +25°C)                   |
- Lead-free (Sn 100%), halogen-free

\*1. Overcharge release voltage = Overcharge detection voltage – Overcharge hysteresis voltage  
(Overcharge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.4 V in 50 mV step.)

\*2. Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage  
(Overdischarge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.7 V in 100 mV step.)

## ■ Applications

- Lithium-ion rechargeable battery pack
- Lithium polymer rechargeable battery pack

## ■ Package

- HSNT-8(1616)

■ **Block Diagram**

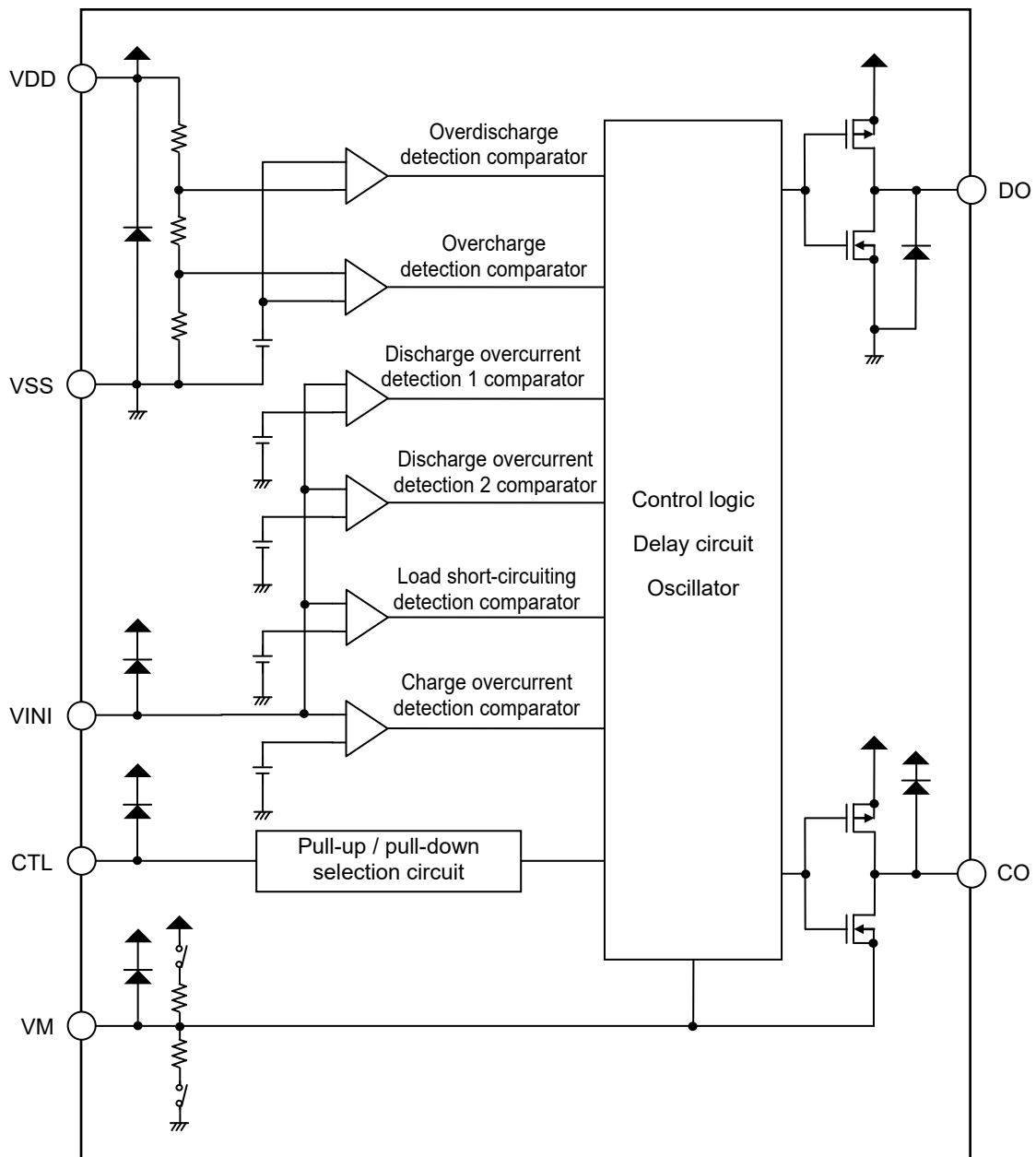
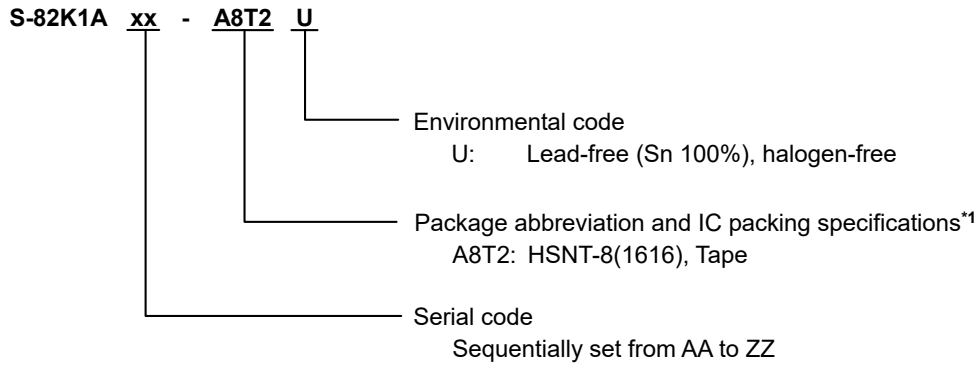


Figure 1

■ **Product Name Structure**

1. **Product name**



\*1. Refer to the tape drawing.

2. **Package**

**Table 1 Package Drawing Codes**

| Package Name | Dimension    | Tape         | Reel         | Land         |
|--------------|--------------|--------------|--------------|--------------|
| HSNT-8(1616) | PY008-A-P-SD | PY008-A-C-SD | PY008-A-R-SD | PY008-A-L-SD |

■ Pin Configuration

1. HSNT-8(1616)

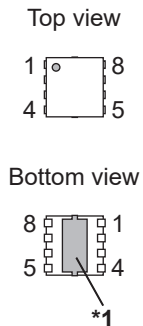


Figure 2

Table 2

| Pin No. | Symbol           | Description  |
|---------|------------------|--|
| 1       | CTL              | Input pin for charge-discharge control signal              |
| 2       | VM               | Input pin for external negative voltage                    |
| 3       | CO               | Connection pin of charge control FET gate (CMOS output)    |
| 4       | DO               | Connection pin of discharge control FET gate (CMOS output) |
| 5       | VSS              | Input pin for negative power supply                        |
| 6       | VDD              | Input pin for positive power supply                        |
| 7       | VINI             | Overcurrent detection pin                                  |
| 8       | NC <sup>*2</sup> | No connection  |

- \*1. Connect the heat sink of backside at shadowed area to the board, and set electric potential open or V<sub>DD</sub>. However, do not use it as the function of electrode.
- \*2. The NC pin is electrically open. The NC pin can be connected to VDD pin or VSS pin.

■ Absolute Maximum Ratings

Table 3

(Ta = +25°C unless otherwise specified)

| Item                                      | Symbol            | Applied Pin | Absolute Maximum Rating                        | Unit |
|---|-------------------|-------------|--|------|
| Input voltage between VDD pin and VSS pin | V <sub>DS</sub>   | VDD         | V <sub>SS</sub> - 0.3 to V <sub>SS</sub> + 6   | V    |
| VINI pin input voltage                    | V <sub>VINI</sub> | VINI        | V <sub>DD</sub> - 6 to V <sub>DD</sub> + 0.3   | V    |
| CTL pin input voltage                     | V <sub>CTL</sub>  | CTL         | V <sub>DD</sub> - 6 to V <sub>DD</sub> + 0.3   | V    |
| VM pin input voltage                      | V <sub>VM</sub>   | VM          | V <sub>DD</sub> - 28 to V <sub>DD</sub> + 0.3  | V    |
| DO pin output voltage                     | V <sub>DO</sub>   | DO          | V <sub>SS</sub> - 0.3 to V <sub>DD</sub> + 0.3 | V    |
| CO pin output voltage                     | V <sub>CO</sub>   | CO          | V <sub>DD</sub> - 28 to V <sub>DD</sub> + 0.3  | V    |
| Operation ambient temperature             | T <sub>opr</sub>  | -           | -40 to +85                                     | °C   |
| Storage temperature                       | T <sub>stg</sub>  | -           | -55 to +125                                    | °C   |

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 4

| Item                                     | Symbol          | Condition    | Min.    | Typ. | Max. | Unit |      |
|--|-----------------|--------------|---------|------|------|------|------|
| Junction-to-ambient thermal resistance*1 | θ <sub>JA</sub> | HSNT-8(1616) | Board A | -    | 214  | -    | °C/W |
|  |                 |              | Board B | -    | 172  | -    | °C/W |
|  |                 |              | Board C | -    | -    | -    | °C/W |
|  |                 |              | Board D | -    | -    | -    | °C/W |
|  |                 |              | Board E | -    | -    | -    | °C/W |

\*1. Test environment: compliance with JEDEC STANDARD JESD51-2A

**Remark** Refer to "■ Power Dissipation" and "Test Board" for details.

■ **Electrical Characteristics**

1. Ta = +25°C

**Table 5**

(Ta = +25°C unless otherwise specified)

| Item  | Symbol              | Condition  | Min.                        | Typ.                   | Max.                        | Unit | Test Circuit |
|---|---------------------|--|-----------------------------|------------------------|-----------------------------|------|--------------|
| <b>Detection Voltage</b>                      |                     |  |                             |                        |                             |      |              |
| Overcharge detection voltage                  | V <sub>CU</sub>     | –  | V <sub>CU</sub> – 0.015     | V <sub>CU</sub>        | V <sub>CU</sub> + 0.015     | V    | 1            |
| Overcharge release voltage                    | V <sub>CL</sub>     | V <sub>CL</sub> ≠ V <sub>CU</sub>                | V <sub>CL</sub> – 0.050     | V <sub>CL</sub>        | V <sub>CL</sub> + 0.050     | V    | 1            |
|   |                     | V <sub>CL</sub> = V <sub>CU</sub>                | V <sub>CL</sub> – 0.020     | V <sub>CL</sub>        | V <sub>CL</sub> + 0.015     | V    | 1            |
| Overdischarge detection voltage               | V <sub>DL</sub>     | –  | V <sub>DL</sub> – 0.050     | V <sub>DL</sub>        | V <sub>DL</sub> + 0.050     | V    | 2            |
| Overdischarge release voltage                 | V <sub>DU</sub>     | V <sub>DL</sub> ≠ V <sub>DU</sub>                | V <sub>DU</sub> – 0.075     | V <sub>DU</sub>        | V <sub>DU</sub> + 0.075     | V    | 2            |
|   |                     | V <sub>DL</sub> = V <sub>DU</sub>                | V <sub>DU</sub> – 0.050     | V <sub>DU</sub>        | V <sub>DU</sub> + 0.050     | V    | 2            |
| Discharge overcurrent detection voltage 1     | V <sub>DIOV1</sub>  | –  | V <sub>DIOV1</sub> – 0.0010 | V <sub>DIOV1</sub>     | V <sub>DIOV1</sub> + 0.0010 | V    | 5            |
| Discharge overcurrent detection voltage 2     | V <sub>DIOV2</sub>  | –  | V <sub>DIOV2</sub> – 0.003  | V <sub>DIOV2</sub>     | V <sub>DIOV2</sub> + 0.003  | V    | 2            |
| Load short-circuiting detection voltage       | V <sub>SHORT</sub>  | –  | V <sub>SHORT</sub> – 0.005  | V <sub>SHORT</sub>     | V <sub>SHORT</sub> + 0.005  | V    | 2            |
| Load short-circuiting detection voltage 2     | V <sub>SHORT2</sub> | –  | V <sub>DD</sub> – 1.2       | V <sub>DD</sub> – 0.8  | V <sub>DD</sub> – 0.5       | V    | 2            |
| Charge overcurrent detection voltage          | V <sub>CIOV</sub>   | –  | V <sub>CIOV</sub> – 0.0010  | V <sub>CIOV</sub>      | V <sub>CIOV</sub> + 0.0010  | V    | 2            |
| Discharge overcurrent release voltage         | V <sub>RIOV</sub>   | V <sub>DD</sub> = 3.4 V                          | V <sub>DD</sub> × 0.77      | V <sub>DD</sub> × 0.80 | V <sub>DD</sub> × 0.83      | V    | 5            |
| <b>0 V Battery Charge</b>                     |                     |  |                             |                        |                             |      |              |
| 0 V battery charge starting charger voltage   | V <sub>0CHA</sub>   | 0 V battery charge enabled                       | 0.7                         | 1.1                    | 1.5                         | V    | 4            |
| 0 V battery charge inhibition battery voltage | V <sub>0INH</sub>   | 0 V battery charge inhibited                     | 0.9                         | 1.2                    | 1.5                         | V    | 2            |
| <b>Internal Resistance</b>                    |                     |  |                             |                        |                             |      |              |
| Resistance between VDD pin and VM pin         | R <sub>VMD</sub>    | V <sub>DD</sub> = 1.8 V, V <sub>VM</sub> = 0 V   | 500                         | 1250                   | 2500                        | kΩ   | 3            |
| Resistance between VM pin and VSS pin         | R <sub>VMS</sub>    | V <sub>DD</sub> = 3.4 V, V <sub>VM</sub> = 1.0 V | 5                           | 10                     | 15                          | kΩ   | 3            |
| CTL pin internal resistance                   | R <sub>CTL</sub>    | –  | R <sub>CTL</sub> × 0.5      | R <sub>CTL</sub>       | R <sub>CTL</sub> × 2.0      | MΩ   | 3            |
| <b>Input Voltage</b>                          |                     |  |                             |                        |                             |      |              |
| Operation voltage between VDD pin and VSS pin | V <sub>DSOP1</sub>  | –  | 1.5                         | –                      | 6.0                         | V    | –            |
| Operation voltage between VDD pin and VM pin  | V <sub>DSOP2</sub>  | –  | 1.5                         | –                      | 28                          | V    | –            |
| CTL pin voltage "H"                           | V <sub>CTLH</sub>   | V <sub>DD</sub> = 3.4 V                          | V <sub>CTLH</sub> – 0.3     | V <sub>CTLH</sub>      | V <sub>CTLH</sub> + 0.3     | V    | 2            |
| CTL pin voltage "L"                           | V <sub>CTLL</sub>   | –  | V <sub>CTLL</sub> – 0.3     | V <sub>CTLL</sub>      | V <sub>CTLL</sub> + 0.3     | V    | 2            |
| <b>Input Current</b>                          |                     |  |                             |                        |                             |      |              |
| Current consumption during operation          | I <sub>OPE</sub>    | V <sub>DD</sub> = 3.4 V, V <sub>VM</sub> = 0 V   | –                           | 2.0                    | 4.0                         | μA   | 3            |
| Current consumption during power-down         | I <sub>PDN</sub>    | V <sub>DD</sub> = V <sub>VM</sub> = 1.5 V        | –                           | –                      | 0.05                        | μA   | 3            |
| Current consumption during overdischarge      | I <sub>OPEd</sub>   | V <sub>DD</sub> = V <sub>VM</sub> = 1.5 V        | –                           | –                      | 0.5                         | μA   | 3            |
| <b>Output Resistance</b>                      |                     |  |                             |                        |                             |      |              |
| CO pin resistance "H"                         | R <sub>COH</sub>    | –  | 5                           | 10                     | 20                          | kΩ   | 4            |
| CO pin resistance "L"                         | R <sub>COL</sub>    | –  | 5                           | 10                     | 20                          | kΩ   | 4            |
| DO pin resistance "H"                         | R <sub>DOH</sub>    | –  | 5                           | 10                     | 20                          | kΩ   | 4            |
| DO pin resistance "L"                         | R <sub>DOl</sub>    | –  | 1                           | 2                      | 4                           | kΩ   | 4            |
| <b>Delay Time</b>                             |                     |  |                             |                        |                             |      |              |
| Overcharge detection delay time               | t <sub>CU</sub>     | –  | t <sub>CU</sub> × 0.7       | t <sub>CU</sub>        | t <sub>CU</sub> × 1.3       | –    | 5            |
| Overdischarge detection delay time            | t <sub>DL</sub>     | –  | t <sub>DL</sub> × 0.7       | t <sub>DL</sub>        | t <sub>DL</sub> × 1.3       | –    | 5            |
| Discharge overcurrent detection delay time 1  | t <sub>DIOV1</sub>  | –  | t <sub>DIOV1</sub> × 0.75   | t <sub>DIOV1</sub>     | t <sub>DIOV1</sub> × 1.25   | –    | 5            |
| Discharge overcurrent detection delay time 2  | t <sub>DIOV2</sub>  | –  | t <sub>DIOV2</sub> × 0.7    | t <sub>DIOV2</sub>     | t <sub>DIOV2</sub> × 1.3    | –    | 5            |
| Load short-circuiting detection delay time    | t <sub>SHORT</sub>  | –  | t <sub>SHORT</sub> × 0.7    | t <sub>SHORT</sub>     | t <sub>SHORT</sub> × 1.3    | –    | 5            |
| Charge overcurrent detection delay time       | t <sub>CIOV</sub>   | –  | t <sub>CIOV</sub> × 0.7     | t <sub>CIOV</sub>      | t <sub>CIOV</sub> × 1.3     | –    | 5            |
| Charge-discharge inhibition delay time        | t <sub>CTL</sub>    | –  | t <sub>CTL</sub> × 0.7      | t <sub>CTL</sub>       | t <sub>CTL</sub> × 1.3      | –    | 5            |

**BATTERY PROTECTION IC WITH CHARGE-DISCHARGE CONTROL FUNCTION FOR 1-CELL PACK**  
**Rev.1.1\_00** **S-82K1A Series**

2. Ta = -20°C to +60°C\*1

**Table 6**

(Ta = -20°C to +60°C\*1 unless otherwise specified)

| Item  | Symbol              | Condition  | Min.                        | Typ.                   | Max.                        | Unit | Test Circuit |
|---|---------------------|--|-----------------------------|------------------------|-----------------------------|------|--------------|
| <b>Detection Voltage</b>                      |                     |  |                             |                        |                             |      |              |
| Overcharge detection voltage                  | V <sub>CU</sub>     | -  | V <sub>CU</sub> - 0.020     | V <sub>CU</sub>        | V <sub>CU</sub> + 0.020     | V    | 1            |
| Overcharge release voltage                    | V <sub>CL</sub>     | V <sub>CL</sub> ≠ V <sub>CU</sub>                | V <sub>CL</sub> - 0.065     | V <sub>CL</sub>        | V <sub>CL</sub> + 0.057     | V    | 1            |
|   |                     | V <sub>CL</sub> = V <sub>CU</sub>                | V <sub>CL</sub> - 0.025     | V <sub>CL</sub>        | V <sub>CL</sub> + 0.020     | V    | 1            |
| Overdischarge detection voltage               | V <sub>DL</sub>     | -  | V <sub>DL</sub> - 0.060     | V <sub>DL</sub>        | V <sub>DL</sub> + 0.055     | V    | 2            |
| Overdischarge release voltage                 | V <sub>DU</sub>     | V <sub>DL</sub> ≠ V <sub>DU</sub>                | V <sub>DU</sub> - 0.085     | V <sub>DU</sub>        | V <sub>DU</sub> + 0.080     | V    | 2            |
|   |                     | V <sub>DL</sub> = V <sub>DU</sub>                | V <sub>DU</sub> - 0.060     | V <sub>DU</sub>        | V <sub>DU</sub> + 0.055     | V    | 2            |
| Discharge overcurrent detection voltage 1     | V <sub>DIOV1</sub>  | -  | V <sub>DIOV1</sub> - 0.0015 | V <sub>DIOV1</sub>     | V <sub>DIOV1</sub> + 0.0015 | V    | 5            |
| Discharge overcurrent detection voltage 2     | V <sub>DIOV2</sub>  | -  | V <sub>DIOV2</sub> - 0.003  | V <sub>DIOV2</sub>     | V <sub>DIOV2</sub> + 0.003  | V    | 2            |
| Load short-circuiting detection voltage       | V <sub>SHORT</sub>  | -  | V <sub>SHORT</sub> - 0.005  | V <sub>SHORT</sub>     | V <sub>SHORT</sub> + 0.005  | V    | 2            |
| Load short-circuiting detection voltage 2     | V <sub>SHORT2</sub> | -  | V <sub>DD</sub> - 1.4       | V <sub>DD</sub> - 0.8  | V <sub>DD</sub> - 0.3       | V    | 2            |
| Charge overcurrent detection voltage          | V <sub>CIOV</sub>   | -  | V <sub>CIOV</sub> - 0.0015  | V <sub>CIOV</sub>      | V <sub>CIOV</sub> + 0.0015  | V    | 2            |
| Discharge overcurrent release voltage         | V <sub>RIOV</sub>   | V <sub>DD</sub> = 3.4 V                          | V <sub>DD</sub> × 0.77      | V <sub>DD</sub> × 0.80 | V <sub>DD</sub> × 0.83      | V    | 5            |
| <b>0 V Battery Charge</b>                     |                     |  |                             |                        |                             |      |              |
| 0 V battery charge starting charger voltage   | V <sub>0CHA</sub>   | 0 V battery charge enabled                       | 0.5                         | 1.1                    | 1.7                         | V    | 4            |
| 0 V battery charge inhibition battery voltage | V <sub>0INH</sub>   | 0 V battery charge inhibited                     | 0.7                         | 1.2                    | 1.7                         | V    | 2            |
| <b>Internal Resistance</b>                    |                     |  |                             |                        |                             |      |              |
| Resistance between VDD pin and VM pin         | R <sub>VMD</sub>    | V <sub>DD</sub> = 1.8 V, V <sub>VM</sub> = 0 V   | 250                         | 1250                   | 3500                        | kΩ   | 3            |
| Resistance between VM pin and VSS pin         | R <sub>VMS</sub>    | V <sub>DD</sub> = 3.4 V, V <sub>VM</sub> = 1.0 V | 3.5                         | 10                     | 20                          | kΩ   | 3            |
| CTL pin internal resistance                   | R <sub>CTL</sub>    | -  | R <sub>CTL</sub> × 0.25     | R <sub>CTL</sub>       | R <sub>CTL</sub> × 3.0      | MΩ   | 3            |
| <b>Input Voltage</b>                          |                     |  |                             |                        |                             |      |              |
| Operation voltage between VDD pin and VSS pin | V <sub>DSOP1</sub>  | -  | 1.5                         | -                      | 6.0                         | V    | -            |
| Operation voltage between VDD pin and VM pin  | V <sub>DSOP2</sub>  | -  | 1.5                         | -                      | 28                          | V    | -            |
| CTL pin voltage "H"                           | V <sub>CTLH</sub>   | V <sub>DD</sub> = 3.4 V                          | V <sub>CTLH</sub> - 0.4     | V <sub>CTLH</sub>      | V <sub>CTLH</sub> + 0.4     | V    | 2            |
| CTL pin voltage "L"                           | V <sub>CTLL</sub>   | -  | V <sub>CTLL</sub> - 0.4     | V <sub>CTLL</sub>      | V <sub>CTLL</sub> + 0.4     | V    | 2            |
| <b>Input Current</b>                          |                     |  |                             |                        |                             |      |              |
| Current consumption during operation          | I <sub>OPE</sub>    | V <sub>DD</sub> = 3.4 V, V <sub>VM</sub> = 0 V   | -                           | 2.0                    | 5.0                         | μA   | 3            |
| Current consumption during power-down         | I <sub>PDN</sub>    | V <sub>DD</sub> = V <sub>VM</sub> = 1.5 V        | -                           | -                      | 0.1                         | μA   | 3            |
| Current consumption during overdischarge      | I <sub>OPED</sub>   | V <sub>DD</sub> = V <sub>VM</sub> = 1.5 V        | -                           | -                      | 1.0                         | μA   | 3            |
| <b>Output Resistance</b>                      |                     |  |                             |                        |                             |      |              |
| CO pin resistance "H"                         | R <sub>COH</sub>    | -  | 2.5                         | 10                     | 30                          | kΩ   | 4            |
| CO pin resistance "L"                         | R <sub>COL</sub>    | -  | 2.5                         | 10                     | 30                          | kΩ   | 4            |
| DO pin resistance "H"                         | R <sub>DOH</sub>    | -  | 2.5                         | 10                     | 30                          | kΩ   | 4            |
| DO pin resistance "L"                         | R <sub>DOL</sub>    | -  | 0.5                         | 2                      | 6                           | kΩ   | 4            |
| <b>Delay Time</b>                             |                     |  |                             |                        |                             |      |              |
| Overcharge detection delay time               | t <sub>CU</sub>     | -  | t <sub>CU</sub> × 0.6       | t <sub>CU</sub>        | t <sub>CU</sub> × 1.4       | -    | 5            |
| Overdischarge detection delay time            | t <sub>DL</sub>     | -  | t <sub>DL</sub> × 0.6       | t <sub>DL</sub>        | t <sub>DL</sub> × 1.4       | -    | 5            |
| Discharge overcurrent detection delay time 1  | t <sub>DIOV1</sub>  | -  | t <sub>DIOV1</sub> × 0.65   | t <sub>DIOV1</sub>     | t <sub>DIOV1</sub> × 1.35   | -    | 5            |
| Discharge overcurrent detection delay time 2  | t <sub>DIOV2</sub>  | -  | t <sub>DIOV2</sub> × 0.6    | t <sub>DIOV2</sub>     | t <sub>DIOV2</sub> × 1.4    | -    | 5            |
| Load short-circuiting detection delay time    | t <sub>SHORT</sub>  | -  | t <sub>SHORT</sub> × 0.6    | t <sub>SHORT</sub>     | t <sub>SHORT</sub> × 1.4    | -    | 5            |
| Charge overcurrent detection delay time       | t <sub>CIOV</sub>   | -  | t <sub>CIOV</sub> × 0.6     | t <sub>CIOV</sub>      | t <sub>CIOV</sub> × 1.4     | -    | 5            |
| Charge-discharge inhibition delay time        | t <sub>CTL</sub>    | -  | t <sub>CTL</sub> × 0.6      | t <sub>CTL</sub>       | t <sub>CTL</sub> × 1.4      | -    | 5            |

\*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

**BATTERY PROTECTION IC WITH CHARGE-DISCHARGE CONTROL FUNCTION FOR 1-CELL PACK**  
**S-82K1A Series**

Rev.1.1\_00

**3. Ta = -40°C to +85°C\*1**

**Table 7**

(Ta = -40°C to +85°C\*1 unless otherwise specified)

| Item  | Symbol              | Condition  | Min.                        | Typ.                   | Max.                        | Unit | Test Circuit |
|---|---------------------|--|-----------------------------|------------------------|-----------------------------|------|--------------|
| <b>Detection Voltage</b>                      |                     |  |                             |                        |                             |      |              |
| Overcharge detection voltage                  | V <sub>CU</sub>     | -  | V <sub>CU</sub> - 0.045     | V <sub>CU</sub>        | V <sub>CU</sub> + 0.030     | V    | 1            |
| Overcharge release voltage                    | V <sub>CL</sub>     | V <sub>CL</sub> ≠ V <sub>CU</sub>                | V <sub>CL</sub> - 0.080     | V <sub>CL</sub>        | V <sub>CL</sub> + 0.060     | V    | 1            |
|   |                     | V <sub>CL</sub> = V <sub>CU</sub>                | V <sub>CL</sub> - 0.050     | V <sub>CL</sub>        | V <sub>CL</sub> + 0.030     | V    | 1            |
| Overdischarge detection voltage               | V <sub>DL</sub>     | -  | V <sub>DL</sub> - 0.080     | V <sub>DL</sub>        | V <sub>DL</sub> + 0.060     | V    | 2            |
| Overdischarge release voltage                 | V <sub>DU</sub>     | V <sub>DL</sub> ≠ V <sub>DU</sub>                | V <sub>DU</sub> - 0.105     | V <sub>DU</sub>        | V <sub>DU</sub> + 0.085     | V    | 2            |
|   |                     | V <sub>DL</sub> = V <sub>DU</sub>                | V <sub>DU</sub> - 0.080     | V <sub>DU</sub>        | V <sub>DU</sub> + 0.060     | V    | 2            |
| Discharge overcurrent detection voltage 1     | V <sub>DIOV1</sub>  | -  | V <sub>DIOV1</sub> - 0.0015 | V <sub>DIOV1</sub>     | V <sub>DIOV1</sub> + 0.0015 | V    | 5            |
| Discharge overcurrent detection voltage 2     | V <sub>DIOV2</sub>  | -  | V <sub>DIOV2</sub> - 0.003  | V <sub>DIOV2</sub>     | V <sub>DIOV2</sub> + 0.003  | V    | 2            |
| Load short-circuiting detection voltage       | V <sub>SHORT</sub>  | -  | V <sub>SHORT</sub> - 0.005  | V <sub>SHORT</sub>     | V <sub>SHORT</sub> + 0.005  | V    | 2            |
| Load short-circuiting detection voltage 2     | V <sub>SHORT2</sub> | -  | V <sub>DD</sub> - 1.4       | V <sub>DD</sub> - 0.8  | V <sub>DD</sub> - 0.3       | V    | 2            |
| Charge overcurrent detection voltage          | V <sub>CIOV</sub>   | -  | V <sub>CIOV</sub> - 0.0015  | V <sub>CIOV</sub>      | V <sub>CIOV</sub> + 0.0015  | V    | 2            |
| Discharge overcurrent release voltage         | V <sub>RIOV</sub>   | V <sub>DD</sub> = 3.4 V                          | V <sub>DD</sub> × 0.77      | V <sub>DD</sub> × 0.80 | V <sub>DD</sub> × 0.83      | V    | 5            |
| <b>0 V Battery Charge</b>                     |                     |  |                             |                        |                             |      |              |
| 0 V battery charge starting charger voltage   | V <sub>0CHA</sub>   | 0 V battery charge enabled                       | 0.5                         | 1.1                    | 1.7                         | V    | 4            |
| 0 V battery charge inhibition battery voltage | V <sub>0INH</sub>   | 0 V battery charge inhibited                     | 0.7                         | 1.2                    | 1.7                         | V    | 2            |
| <b>Internal Resistance</b>                    |                     |  |                             |                        |                             |      |              |
| Resistance between VDD pin and VM pin         | R <sub>VMD</sub>    | V <sub>DD</sub> = 1.8 V, V <sub>VM</sub> = 0 V   | 250                         | 1250                   | 3500                        | kΩ   | 3            |
| Resistance between VM pin and VSS pin         | R <sub>VMS</sub>    | V <sub>DD</sub> = 3.4 V, V <sub>VM</sub> = 1.0 V | 3.5                         | 10                     | 20                          | kΩ   | 3            |
| CTL pin internal resistance                   | R <sub>CTL</sub>    | -  | R <sub>CTL</sub> × 0.25     | R <sub>CTL</sub>       | R <sub>CTL</sub> × 3.0      | MΩ   | 3            |
| <b>Input Voltage</b>                          |                     |  |                             |                        |                             |      |              |
| Operation voltage between VDD pin and VSS pin | V <sub>DSOP1</sub>  | -  | 1.5                         | -                      | 6.0                         | V    | -            |
| Operation voltage between VDD pin and VM pin  | V <sub>DSOP2</sub>  | -  | 1.5                         | -                      | 28                          | V    | -            |
| CTL pin voltage "H"                           | V <sub>CTLH</sub>   | V <sub>DD</sub> = 3.4 V                          | V <sub>CTLH</sub> - 0.4     | V <sub>CTLH</sub>      | V <sub>CTLH</sub> + 0.4     | V    | 2            |
| CTL pin voltage "L"                           | V <sub>CTLL</sub>   | -  | V <sub>CTLL</sub> - 0.4     | V <sub>CTLL</sub>      | V <sub>CTLL</sub> + 0.4     | V    | 2            |
| <b>Input Current</b>                          |                     |  |                             |                        |                             |      |              |
| Current consumption during operation          | I <sub>OPE</sub>    | V <sub>DD</sub> = 3.4 V, V <sub>VM</sub> = 0 V   | -                           | 2.0                    | 5.0                         | μA   | 3            |
| Current consumption during power-down         | I <sub>PDN</sub>    | V <sub>DD</sub> = V <sub>VM</sub> = 1.5 V        | -                           | -                      | 0.1                         | μA   | 3            |
| Current consumption during overdischarge      | I <sub>OPED</sub>   | V <sub>DD</sub> = V <sub>VM</sub> = 1.5 V        | -                           | -                      | 1.0                         | μA   | 3            |
| <b>Output Resistance</b>                      |                     |  |                             |                        |                             |      |              |
| CO pin resistance "H"                         | R <sub>COH</sub>    | -  | 2.5                         | 10                     | 30                          | kΩ   | 4            |
| CO pin resistance "L"                         | R <sub>COL</sub>    | -  | 2.5                         | 10                     | 30                          | kΩ   | 4            |
| DO pin resistance "H"                         | R <sub>DOH</sub>    | -  | 2.5                         | 10                     | 30                          | kΩ   | 4            |
| DO pin resistance "L"                         | R <sub>DOL</sub>    | -  | 0.5                         | 2                      | 6                           | kΩ   | 4            |
| <b>Delay Time</b>                             |                     |  |                             |                        |                             |      |              |
| Overcharge detection delay time               | t <sub>CU</sub>     | -  | t <sub>CU</sub> × 0.4       | t <sub>CU</sub>        | t <sub>CU</sub> × 1.6       | -    | 5            |
| Overdischarge detection delay time            | t <sub>DL</sub>     | -  | t <sub>DL</sub> × 0.4       | t <sub>DL</sub>        | t <sub>DL</sub> × 1.6       | -    | 5            |
| Discharge overcurrent detection delay time 1  | t <sub>DIOV1</sub>  | -  | t <sub>DIOV1</sub> × 0.4    | t <sub>DIOV1</sub>     | t <sub>DIOV1</sub> × 1.6    | -    | 5            |
| Discharge overcurrent detection delay time 2  | t <sub>DIOV2</sub>  | -  | t <sub>DIOV2</sub> × 0.4    | t <sub>DIOV2</sub>     | t <sub>DIOV2</sub> × 1.6    | -    | 5            |
| Load short-circuiting detection delay time    | t <sub>SHORT</sub>  | -  | t <sub>SHORT</sub> × 0.4    | t <sub>SHORT</sub>     | t <sub>SHORT</sub> × 1.6    | -    | 5            |
| Charge overcurrent detection delay time       | t <sub>CIOV</sub>   | -  | t <sub>CIOV</sub> × 0.4     | t <sub>CIOV</sub>      | t <sub>CIOV</sub> × 1.6     | -    | 5            |
| Charge-discharge inhibition delay time        | t <sub>CTL</sub>    | -  | t <sub>CTL</sub> × 0.4      | t <sub>CTL</sub>       | t <sub>CTL</sub> × 1.6      | -    | 5            |

\*1. Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.



## ■ Test Circuits

When CTL pin control logic is active "H", SW1 and SW3 are turned off, SW2 and SW4 are turned on. When CTL pin control logic is active "L", SW1 and SW3 are turned on, SW2 and SW4 are turned off.

**Caution** Unless otherwise specified, the output voltage levels "H" and "L" at CO pin ( $V_{CO}$ ) and DO pin ( $V_{DO}$ ) are judged by the threshold voltage (1.0 V) of the N-channel FET. Judge the CO pin level with respect to  $V_M$  and the DO pin level with respect to  $V_{SS}$ .

### 1. Overcharge detection voltage, overcharge release voltage (Test circuit 1)

Overcharge detection voltage ( $V_{CU}$ ) is defined as the voltage V1 at which  $V_{CO}$  goes from "H" to "L" when the voltage V1 is gradually increased after setting  $V1 = 3.4$  V. Overcharge release voltage ( $V_{CL}$ ) is defined as the voltage V1 at which  $V_{CO}$  goes from "L" to "H" when the voltage V1 is then gradually decreased. Overcharge hysteresis voltage ( $V_{HC}$ ) is defined as the difference between  $V_{CU}$  and  $V_{CL}$ .

### 2. Overdischarge detection voltage, overdischarge release voltage (Test circuit 2)

Overdischarge detection voltage ( $V_{DL}$ ) is defined as the voltage V1 at which  $V_{DO}$  goes from "H" to "L" when the voltage V1 is gradually decreased after setting  $V1 = 3.4$  V,  $V2 = V5 = V6 = 0$  V. Overdischarge release voltage ( $V_{DU}$ ) is defined as the voltage V1 at which  $V_{DO}$  goes from "L" to "H" when setting  $V2 = 0.01$  V,  $V5 = V6 = 0$  V and when the voltage V1 is then gradually increased. Overdischarge hysteresis voltage ( $V_{HD}$ ) is defined as the difference between  $V_{DU}$  and  $V_{DL}$ .

### 3. Discharge overcurrent detection voltage 1, discharge overcurrent release voltage (Test circuit 5)

Discharge overcurrent detection voltage 1 ( $V_{DIOV1}$ ) is defined as the voltage V5 whose delay time for changing  $V_{DO}$  from "H" to "L" is discharge overcurrent detection delay time 1 ( $t_{DIOV1}$ ) when the voltage V5 is increased after setting  $V1 = 3.4$  V,  $V2 = 1.4$  V,  $V5 = V6 = 0$  V. Discharge overcurrent release voltage ( $V_{RIOV}$ ) is defined as the voltage V2 at which  $V_{DO}$  goes from "L" to "H" when setting  $V2 = 3.4$  V,  $V5 = 0$  V and when the voltage V2 is then gradually decreased.

When the voltage V2 falls below  $V_{RIOV}$ ,  $V_{DO}$  will go to "H" after 1.0 ms typ. and maintain "H" during load short-circuiting detection delay time ( $t_{SHORT}$ ).

### 4. Discharge overcurrent detection voltage 2 (Test circuit 2)

Discharge overcurrent detection voltage 2 ( $V_{DIOV2}$ ) is defined as the voltage V5 whose delay time for changing  $V_{DO}$  from "H" to "L" is discharge overcurrent detection delay time 2 ( $t_{DIOV2}$ ) when the voltage V5 is increased after setting  $V1 = 3.4$  V,  $V2 = 1.4$  V,  $V5 = V6 = 0$  V.

### 5. Load short-circuiting detection voltage (Test circuit 2)

Load short-circuiting detection voltage ( $V_{SHORT}$ ) is defined as the voltage V5 whose delay time for changing  $V_{DO}$  from "H" to "L" is  $t_{SHORT}$  when the voltage V5 is increased after setting  $V1 = 3.4$  V,  $V2 = 1.4$  V,  $V5 = V6 = 0$  V.

### 6. Load short-circuiting detection voltage 2 (Test circuit 2)

Load short-circuiting detection voltage 2 ( $V_{SHORT2}$ ) is defined as the voltage V2 whose delay time for changing  $V_{DO}$  from "H" to "L" is  $t_{SHORT}$  when the voltage V2 is increased after setting  $V1 = 3.4$  V,  $V2 = V5 = V6 = 0$  V.

**7. Charge overcurrent detection voltage**  
**(Test circuit 2)**

Charge overcurrent detection voltage ( $V_{CIOV}$ ) is defined as the voltage  $V_5$  whose delay time for changing  $V_{CO}$  from "H" to "L" is charge overcurrent detection delay time ( $t_{CIOV}$ ) when the voltage  $V_5$  is decreased after setting  $V_1 = 3.4\text{ V}$ ,  $V_2 = V_5 = V_6 = 0\text{ V}$ .

**8. CTL pin voltage "H", CTL pin voltage "L"**  
**(Test circuit 2)****8.1 CTL pin control logic active "H"**

The CTL pin voltage "H" ( $V_{CTLH}$ ) is defined as the voltage  $V_6$  at which  $V_{CO}$  and  $V_{DO}$  go from "H" to "L" when the voltage  $V_6$  is gradually increased after setting  $V_1 = 3.4\text{ V}$ ,  $V_2 = V_5 = V_6 = 0\text{ V}$ .

After that, the CTL pin voltage "L" ( $V_{CTLL}$ ) is defined as the voltage  $V_6$  at which  $V_{CO}$  and  $V_{DO}$  go from "L" to "H" after  $V_6$  is gradually decreased.

**8.2 CTL pin control logic active "L"**

$V_{CTLL}$  is defined as the voltage difference between the voltage  $V_6$  and the voltage  $V_1$  ( $V_1 - V_6$ ) at which  $V_{CO}$  and  $V_{DO}$  go from "H" to "L" when the voltage  $V_6$  is gradually increased after setting  $V_1 = 3.4\text{ V}$ ,  $V_2 = V_5 = V_6 = 0\text{ V}$ . After that,  $V_{CTLH}$  is defined as  $V_1 - V_6$  at which  $V_{CO}$  and  $V_{DO}$  go from "L" to "H" after  $V_6$  is gradually decreased.

**9. Current consumption during operation**  
**(Test circuit 3)**

The current consumption during operation ( $I_{OPE}$ ) is the current that flows through the VDD pin ( $I_{DD}$ ) under the set conditions of  $V_1 = 3.4\text{ V}$ ,  $V_2 = V_5 = V_6 = 0\text{ V}$ . However, the current flowing through the CTL pin internal resistance is excluded.

**10. Current consumption during power-down, current consumption during overdischarge**  
**(Test circuit 3)****10.1 With power-down function**

The current consumption during power-down ( $I_{PDN}$ ) is  $I_{DD}$  under the set conditions of  $V_1 = V_2 = 1.5\text{ V}$ ,  $V_5 = V_6 = 0\text{ V}$ .

**10.2 Without power-down function**

The current consumption during overdischarge ( $I_{OPED}$ ) is  $I_{DD}$  under the set conditions of  $V_1 = V_2 = 1.5\text{ V}$ ,  $V_5 = V_6 = 0\text{ V}$ .

**11. Resistance between VDD pin and VM pin**  
**(Test circuit 3)**

$R_{VMD}$  is the resistance between VDD pin and VM pin under the set conditions of  $V_1 = 1.8\text{ V}$ ,  $V_2 = V_5 = V_6 = 0\text{ V}$ .

**12. Resistance between VM pin and VSS pin**  
**(Test circuit 3)**

$R_{VMS}$  is the resistance between VM pin and VSS pin when the voltage  $V_5$  is decreased to  $0\text{ V}$  after setting  $V_1 = 3.4\text{ V}$ ,  $V_2 = V_5 = 1.0\text{ V}$ ,  $V_6 = 0\text{ V}$ .

**13. CTL pin internal resistance**  
**(Test circuit 3)**

**13.1 CTL pin control logic active "H", CTL pin internal resistance "pull-up"**

The CTL pin internal resistance ( $R_{CTL}$ ) is the resistance between CTL pin and VDD pin under the set conditions of  $V1 = 3.4\text{ V}$ ,  $V2 = V5 = V6 = 0\text{ V}$ .

**13.2 CTL pin control logic active "H", CTL pin internal resistance "pull-down"**

$R_{CTL}$  is the resistance between CTL pin and VSS pin under the set conditions of  $V1 = V6 = 3.4\text{ V}$ ,  $V2 = V5 = 0\text{ V}$ .

**13.3 CTL pin control logic active "L", CTL pin internal resistance "pull-up"**

$R_{CTL}$  is the resistance between CTL pin and VDD pin under the set conditions of  $V1 = V6 = 3.4\text{ V}$ ,  $V2 = V5 = 0\text{ V}$ .

**13.4 CTL pin control logic active "L", CTL pin internal resistance "pull-down"**

$R_{CTL}$  is the resistance between CTL pin and VSS pin under the set conditions of  $V1 = 3.4\text{ V}$ ,  $V2 = V5 = V6 = 0\text{ V}$ .

**14. CO pin resistance "H"**  
**(Test circuit 4)**

The CO pin resistance "H" ( $R_{COH}$ ) is the resistance between VDD pin and CO pin under the set conditions of  $V1 = 3.4\text{ V}$ ,  $V2 = V5 = 0\text{ V}$ ,  $V3 = 3.0\text{ V}$ .

**15. CO pin resistance "L"**  
**(Test circuit 4)**

The CO pin resistance "L" ( $R_{COL}$ ) is the resistance between VM pin and CO pin under the set conditions of  $V1 = 4.7\text{ V}$ ,  $V2 = V5 = 0\text{ V}$ ,  $V3 = 0.4\text{ V}$ .

**16. DO pin resistance "H"**  
**(Test circuit 4)**

The DO pin resistance "H" ( $R_{DOH}$ ) is the resistance between VDD pin and DO pin under the set conditions of  $V1 = 3.4\text{ V}$ ,  $V2 = V5 = 0\text{ V}$ ,  $V4 = 3.0\text{ V}$ .

**17. DO pin resistance "L"**  
**(Test circuit 4)**

The DO pin resistance "L" ( $R_{DOL}$ ) is the resistance between VSS pin and DO pin under the set conditions of  $V1 = 1.8\text{ V}$ ,  $V2 = V5 = 0\text{ V}$ ,  $V4 = 0.4\text{ V}$ .

**18. Overcharge detection delay time**  
**(Test circuit 5)**

After setting  $V1 = 3.4\text{ V}$ ,  $V2 = V5 = V6 = 0\text{ V}$ , the voltage  $V1$  is increased. The time interval from when the voltage  $V1$  exceeds  $V_{CU}$  until  $V_{CO}$  goes to "L" is the overcharge detection delay time ( $t_{CU}$ ).

**19. Overdischarge detection delay time**  
**(Test circuit 5)**

After setting  $V1 = 3.4\text{ V}$ ,  $V2 = V5 = V6 = 0\text{ V}$ , the voltage  $V1$  is decreased. The time interval from when the voltage  $V1$  falls below  $V_{DL}$  until  $V_{DO}$  goes to "L" is the overdischarge detection delay time ( $t_{DL}$ ).

**20. Discharge overcurrent detection delay time 1**  
**(Test circuit 5)**

After setting  $V1 = 3.4\text{ V}$ ,  $V2 = 1.4\text{ V}$ ,  $V5 = V6 = 0\text{ V}$ , the voltage  $V5$  is increased. The time interval from when the voltage  $V5$  exceeds  $V_{DIOV1}$  until  $V_{DO}$  goes to "L" is the discharge overcurrent detection delay time 1 ( $t_{DIOV1}$ ).

**21. Discharge overcurrent detection delay time 2**  
**(Test circuit 5)**

After setting  $V1 = 3.4\text{ V}$ ,  $V2 = 1.4\text{ V}$ ,  $V5 = V6 = 0\text{ V}$ , the voltage  $V5$  is increased. The time interval from when the voltage  $V5$  exceeds  $V_{DIOV2}$  until  $V_{DO}$  goes to "L" is the discharge overcurrent detection delay time 2 ( $t_{DIOV2}$ ).

**22. Load short-circuiting detection delay time**  
**(Test circuit 5)**

After setting  $V1 = 3.4\text{ V}$ ,  $V2 = 1.4\text{ V}$ ,  $V5 = V6 = 0\text{ V}$ , the voltage  $V5$  is increased. The time interval from when the voltage  $V5$  exceeds  $V_{SHORT}$  until  $V_{DO}$  goes to "L" is the load short-circuiting detection delay time ( $t_{SHORT}$ ).

**23. Charge overcurrent detection delay time**  
**(Test circuit 5)**

After setting  $V1 = 3.4\text{ V}$ ,  $V2 = V5 = V6 = 0\text{ V}$ , the voltage  $V5$  is decreased. The time interval from when the voltage  $V5$  falls below  $V_{CIOV}$  until  $V_{CO}$  goes to "L" is the charge overcurrent detection delay time ( $t_{CIOV}$ ).

**24. Charge-discharge inhibition delay time**  
**(Test circuit 5)****24. 1 CTL pin control logic active "H"**

After setting  $V1 = 3.4\text{ V}$ ,  $V2 = V5 = V6 = 0\text{ V}$ , the voltage  $V6$  is increased. The time interval from when the voltage  $V6$  exceeds  $V_{CTLH}$  until  $V_{CO}$  and  $V_{DO}$  go to "L" is the charge-discharge inhibition delay time ( $t_{CTL}$ ).

**24. 2 CTL pin control logic active "L"**

After setting  $V1 = 3.4\text{ V}$ ,  $V2 = V5 = V6 = 0\text{ V}$ , the voltage  $V6$  is increased. The time interval from when the voltage  $V1 - V6$  falls below  $V_{CTLL}$  until  $V_{CO}$  and  $V_{DO}$  go to "L" is  $t_{CTL}$ .

**25. 0 V battery charge starting charger voltage (0 V battery charge enabled)**  
**(Test circuit 4)**

The 0 V battery charge starting charger voltage ( $V_{0CHA}$ ) is defined as the absolute value of voltage  $V2$  at which the current flowing through the CO pin ( $I_{CO}$ ) exceeds  $1.0\text{ }\mu\text{A}$  when the voltage  $V2$  is gradually decreased after setting  $V1 = V5 = 0\text{ V}$ ,  $V2 = V3 = -0.5\text{ V}$ .

**26. 0 V battery charge inhibition battery voltage (0 V battery charge inhibited)**  
**(Test circuit 2)**

The 0 V battery charge inhibition battery voltage ( $V_{0INH}$ ) is defined as the voltage  $V1$  at which  $V_{CO}$  goes to "L" ( $V_{CO} = V_{VM}$ ) when the voltage  $V1$  is gradually decreased after setting  $V1 = 1.8\text{ V}$ ,  $V2 = -2.0\text{ V}$ ,  $V5 = V6 = 0\text{ V}$ .

# BATTERY PROTECTION IC WITH CHARGE-DISCHARGE CONTROL FUNCTION FOR 1-CELL PACK

Rev.1.1\_00

S-82K1A Series

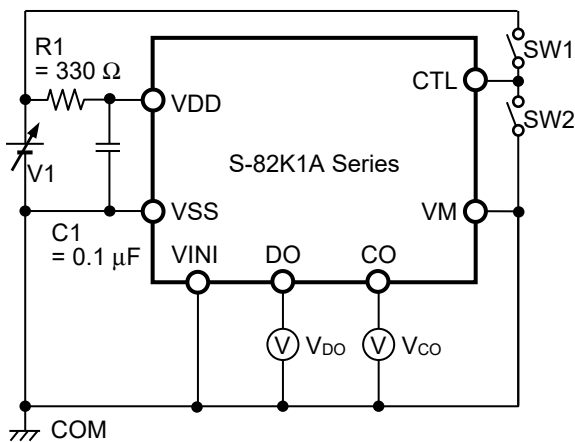


Figure 3 Test Circuit 1

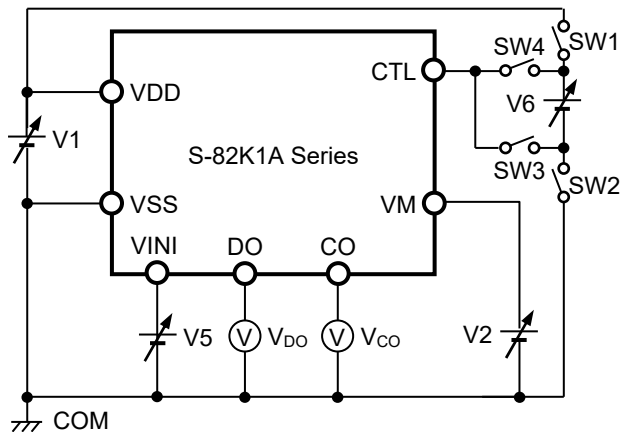


Figure 4 Test Circuit 2

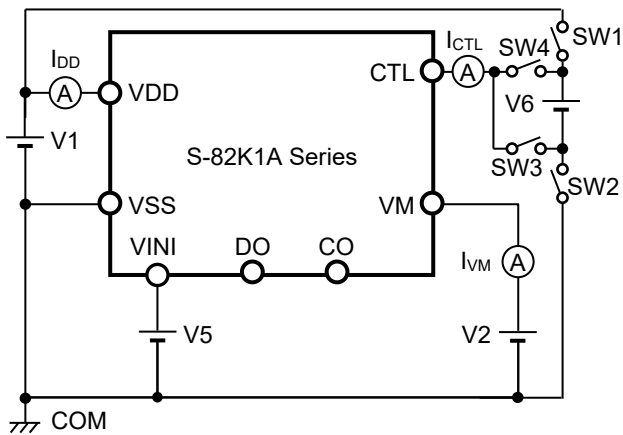


Figure 5 Test Circuit 3

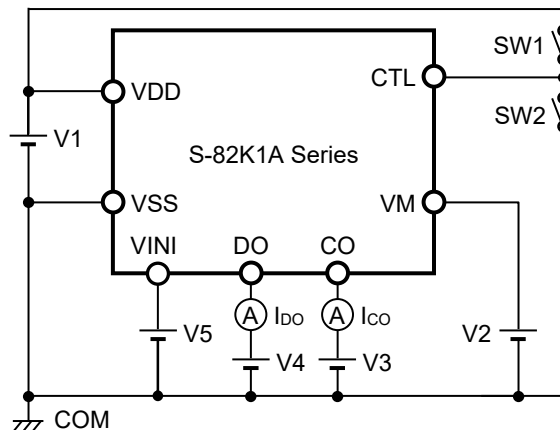


Figure 6 Test Circuit 4

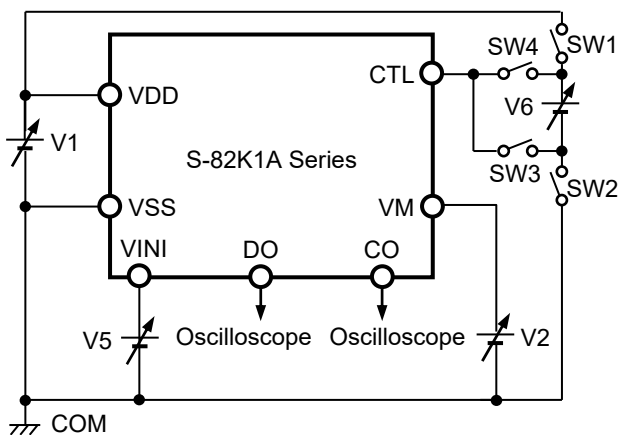


Figure 7 Test Circuit 5

## ■ Operation

**Remark** Refer to "■ Battery Protection IC Connection Example".

### 1. Normal status

The S-82K1A Series monitors the voltage of the battery connected between VDD pin and VSS pin, the voltage between VINI pin and VSS pin, and the voltage between CTL pin and VSS pin to control charging and discharging.

#### 1.1 CTL pin control logic active "H"

When the battery voltage is in the range from overdischarge detection voltage ( $V_{DL}$ ) to overcharge detection voltage ( $V_{CU}$ ), the VINI pin voltage is in the range from charge overcurrent detection voltage ( $V_{CIOV}$ ) to discharge overcurrent detection voltage 1 ( $V_{DIOV1}$ ), and the CTL pin voltage is equal to or lower than the CTL pin voltage "L" ( $V_{CTL L}$ ), the S-82K1A Series turns both the charge and discharge control FETs on. This status is called the normal status, and in this condition charging and discharging can be carried out freely.

The resistance between VDD pin and VM pin ( $R_{VMD}$ ), and the resistance between VM pin and VSS pin ( $R_{VMS}$ ) are not connected in the normal status.

#### 1.2 CTL pin control logic active "L"

When the battery voltage is in the range from  $V_{DL}$  to  $V_{CU}$ , the VINI pin voltage is in the range from  $V_{CIOV}$  to  $V_{DIOV1}$ , and the CTL pin voltage is equal to or higher than the CTL pin voltage "H" ( $V_{CTL H}$ ), the S-82K1A Series turns both the charge and discharge control FETs on. This status is called the normal status, and in this condition charging and discharging can be carried out freely.

$R_{VMD}$  and  $R_{VMS}$  are not connected in the normal status.

**Caution** After the battery is connected, discharging may not be carried out. In this case, the S-82K1A Series returns to the normal status by connecting a charger.

### 2. Overcharge status

#### 2.1 $V_{CL} \neq V_{CU}$ (Product in which overcharge release voltage differs from overcharge detection voltage)

When the battery voltage becomes higher than  $V_{CU}$  during charging in the normal status and the condition continues for the overcharge detection delay time ( $t_{CU}$ ) or longer, the S-82K1A Series turns the charge control FET off to stop charging. This status is called the overcharge status.

The overcharge status is released in the following two cases.

- (1) In the case that the VM pin voltage is lower than 0.35 V typ., the S-82K1A Series releases the overcharge status when the battery voltage falls below overcharge release voltage ( $V_{CL}$ ).
- (2) In the case that the VM pin voltage is equal to or higher than 0.35 V typ., the S-82K1A Series releases the overcharge status when the battery voltage falls below  $V_{CU}$ .

When the discharge is started by connecting a load after the overcharge detection, the VM pin voltage rises by the  $V_f$  voltage of the internal parasitic diode than the VSS pin voltage, because the discharge current flows through the parasitic diode in the charge control FET. If this VM pin voltage is equal to or higher than 0.35 V typ., the S-82K1A Series releases the overcharge status when the battery voltage is equal to or lower than  $V_{CU}$ .

**Caution** If the battery is charged to a voltage higher than  $V_{CU}$  and the battery voltage does not fall below  $V_{CU}$  even when a heavy load is connected, discharge overcurrent detection and load short-circuiting detection do not function until the battery voltage falls below  $V_{CU}$ . Since an actual battery has an internal impedance of tens of m $\Omega$ , the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection and load short-circuiting detection function.

## **2.2 $V_{CL} = V_{CU}$ (Product in which overcharge release voltage is the same as overcharge detection voltage)**

When the battery voltage becomes higher than  $V_{CU}$  during charging in the normal status and the condition continues for  $t_{CU}$  or longer, the S-82K1A Series turns the charge control FET off to stop charging. This status is called the overcharge status.

In the case that the VM pin voltage is equal to or higher than 0.35 V typ. and the battery voltage falls below  $V_{CU}$ , the S-82K1A Series releases the overcharge status.

When the discharge is started by connecting a load after the overcharge detection, the VM pin voltage rises by the  $V_f$  voltage of the internal parasitic diode than the VSS pin voltage, because the discharge current flows through the parasitic diode in the charge control FET. If this VM pin voltage is equal to or higher than 0.35 V typ., the S-82K1A Series releases the overcharge status when the battery voltage is equal to or lower than  $V_{CU}$ .

**Caution 1. If the battery is charged to a voltage higher than  $V_{CU}$  and the battery voltage does not fall below  $V_{CU}$  even when a heavy load is connected, discharge overcurrent detection and load short-circuiting detection do not function until the battery voltage falls below  $V_{CU}$ . Since an actual battery has an internal impedance of tens of  $m\Omega$ , the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection and load short-circuiting detection function.**

**2. When a charger is connected after overcharge detection, the overcharge status is not released even if the battery voltage is below  $V_{CL}$ . The overcharge status is released when the discharge current flows and the VM pin voltage goes over 0.35 V typ. by removing the charger.**

## **3. Overdischarge status**

When the battery voltage falls below  $V_{DL}$  during discharging in the normal status and the condition continues for the overdischarge detection delay time ( $t_{DL}$ ) or longer, the S-82K1A Series turns the discharge control FET off to stop discharging. This status is called the overdischarge status.

Under the overdischarge status, VDD pin and VM pin are shorted by  $R_{VMD}$  in the S-82K1A Series. The VM pin voltage is pulled up by  $R_{VMD}$ .

When connecting a charger in the overdischarge status, the battery voltage reaches  $V_{DL}$  or higher and the S-82K1A Series releases the overdischarge status if the VM pin voltage is below 0 V typ.

The battery voltage reaches the overdischarge release voltage ( $V_{DU}$ ) or higher and the S-82K1A Series releases the overdischarge status if the VM pin voltage is not below 0 V typ.

$R_{VMS}$  is not connected in the overdischarge status.

### **3.1 With power-down function**

Under the overdischarge status, when voltage difference between VDD pin and VM pin is 0.8 V typ. or lower, the power-down function works and the current consumption is reduced to the current consumption during power-down ( $I_{PDN}$ ). By connecting a battery charger, the power-down function is released when the VM pin voltage is 0.7 V typ. or lower.

- When a battery is not connected to a charger and the VM pin voltage  $\geq 0.7$  V typ., the S-82K1A Series maintains the overdischarge status even when the battery voltage reaches  $V_{DU}$  or higher.
- When a battery is connected to a charger and 0.7 V typ. > the VM pin voltage > 0 V typ., the battery voltage reaches  $V_{DU}$  or higher and the S-82K1A Series releases the overdischarge status.
- When a battery is connected to a charger and 0 V typ.  $\geq$  the VM pin voltage, the battery voltage reaches  $V_{DL}$  or higher and the S-82K1A Series releases the overdischarge status.

### **3.2 Without power-down function**

Under the overdischarge status, the power-down function does not work even when voltage difference between VDD pin and VM pin is 0.8 V typ. or lower.

- When a battery is not connected to a charger and the VM pin voltage  $\geq 0.7$  V typ., the battery voltage reaches  $V_{DU}$  or higher and the S-82K1A Series releases the overdischarge status.
- When a battery is connected to a charger and 0.7 V typ. > the VM pin voltage > 0 V typ., the battery voltage reaches  $V_{DU}$  or higher and the S-82K1A Series releases the overdischarge status.
- When a battery is connected to a charger and 0 V typ.  $\geq$  the VM pin voltage, the battery voltage reaches  $V_{DL}$  or higher and the S-82K1A Series releases the overdischarge status.

#### **4. Discharge overcurrent status (discharge overcurrent 1, discharge overcurrent 2, load short-circuiting, load short-circuiting 2)**

##### **4.1 Discharge overcurrent 1, discharge overcurrent 2, load short-circuiting**

When a battery in the normal status is in the status where the VINI pin voltage is equal to or higher than  $V_{DIOV1}$  because the discharge current is equal to or higher than the specified value and the status continues for the discharge overcurrent detection delay time ( $t_{DIOV1}$ ) or longer, the discharge control FET is turned off and discharging is stopped. This status is called the discharge overcurrent status.

Under the discharge overcurrent status, VM pin and VSS pin are shorted by  $R_{VMS}$  in the S-82K1A Series. However, the VM pin voltage is the VDD pin voltage due to the load as long as the load is connected. When the load is disconnected, VM pin voltage returns to the VSS pin voltage.

When the VM pin voltage returns to  $V_{RIOV}$  or lower, the S-82K1A Series releases the discharge overcurrent status.

$R_{VMD}$  is not connected in the discharge overcurrent status.

##### **4.2 Load short-circuiting 2**

When a battery in the normal status is in the status where a load causing discharge overcurrent is connected, and the VM pin voltage is equal to or higher than  $V_{SHORT2}$  and the status continues for the load short-circuiting detection delay time ( $t_{SHORT}$ ) or longer, the discharge control FET is turned off and discharging is stopped. This status is called the discharge overcurrent status.

The S-82K1A Series releases the discharge overcurrent status in the same way as in "**4.1 Discharge overcurrent 1, discharge overcurrent 2, load short-circuiting**".

##### **4.3 Discharge overcurrent status reset function by CTL pin**

###### **4.3.1 With discharge overcurrent status reset function by CTL pin**

Under the discharge overcurrent status, when the CTL pin is active and the condition continues for the charge-discharge inhibition delay time ( $t_{CTL}$ ) or longer, the charge control FET and the discharge control FET are turned off, and charging and discharging are stopped. The S-82K1A Series then becomes the charge-discharge inhibition status.

The S-82K1A Series returns to the normal status if the CTL pin is made inactive and the charge-discharge inhibition status is released.

###### **4.3.2 Without discharge overcurrent status reset function by CTL pin**

Under the discharge overcurrent status, even when the CTL pin is active and the condition continues for  $t_{CTL}$  or longer, the S-82K1A Series does not become the charge-discharge inhibition status and maintains the discharge overcurrent status.

The S-82K1A Series does not return to the normal status and maintains the discharge overcurrent status even if the CTL pin is made inactive.

#### **5. Charge overcurrent status**

When a battery in the normal status is in the status where the VINI pin voltage is equal to or lower than  $V_{CIOV}$  because the charge current is equal to or higher than the specified value and the status continues for the charge overcurrent detection delay time ( $t_{CIOV}$ ) or longer, the charge control FET is turned off and charging is stopped. This status is called the charge overcurrent status.

The S-82K1A Series releases the charge overcurrent status when the discharge current flows and the VM pin voltage is 0.35 V typ. or higher by removing the charger.

The charge overcurrent detection does not function in the overdischarge status.



## **6. Charge-discharge inhibition status**

### **6.1 CTL pin control logic active "H"**

When the CTL pin voltage is equal to or higher than CTL pin voltage "H" ( $V_{CTLH}$ ) and the status continues for the charge-discharge inhibition delay time ( $t_{CTL}$ ) or longer, the charge control FET and the discharge control FET are turned off, and charging and discharging are stopped. This status is called the charge-discharge inhibition status. The S-82K1A Series releases charge-discharge inhibition status when the CTL pin voltage is equal to or lower than CTL pin voltage "L" ( $V_{CTL L}$ ).

### **6.2 CTL pin control logic active "L"**

When the CTL pin voltage is equal to or lower than  $V_{CTL L}$  and the status continues for  $t_{CTL}$  or longer, the charge control FET and the discharge control FET are turned off, and charging and discharging are stopped. This status is called the charge-discharge inhibition status.

The S-82K1A Series releases charge-discharge inhibition status when the CTL pin voltage is equal to or higher than  $V_{CTLH}$ .

### **6.3 CTL pin internal resistance**

#### **6.3.1 CTL pin internal resistance "pull-up"**

The CTL pin is shorted to the VDD pin by the CTL pin internal resistance ( $R_{CTL}$ ).

#### **6.3.2 CTL pin internal resistance "pull-down"**

The CTL pin is shorted to the VSS pin by  $R_{CTL}$ .

When the S-82K1A Series becomes overdischarge status,  $R_{CTL}$  is disconnected, and the input current and the output current to the CTL pin are cut off.

The charge-discharge control by the CTL pin does not function in the overdischarge status.

**7. 0 V battery charge enabled**

This function is used to recharge a connected battery whose voltage is 0 V due to self-discharge. When the 0 V battery charge starting charger voltage ( $V_{0CHA}$ ) or a higher voltage is applied between the EB+ and EB- pins by connecting a charger, the charge control FET gate is fixed to the VDD pin voltage.

When the voltage between the gate and source of the charge control FET becomes equal to or higher than the threshold voltage due to the charger voltage, the charge control FET is turned on to start charging. At this time, the discharge control FET is off and the charging current flows through the internal parasitic diode in the discharge control FET. When the battery voltage becomes equal to or higher than  $V_{DL}$ , the S-82K1A Series returns to the normal status.

**Caution 1. Some battery providers do not recommend charging for a completely self-discharged lithium-ion rechargeable battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge.**

**2. The 0 V battery charge has higher priority than the charge overcurrent detection function. Consequently, a product in which use of the 0 V battery charge is enabled charges a battery forcibly and the charge overcurrent cannot be detected when the battery voltage is lower than  $V_{DL}$ .**

**8. 0 V battery charge inhibited**

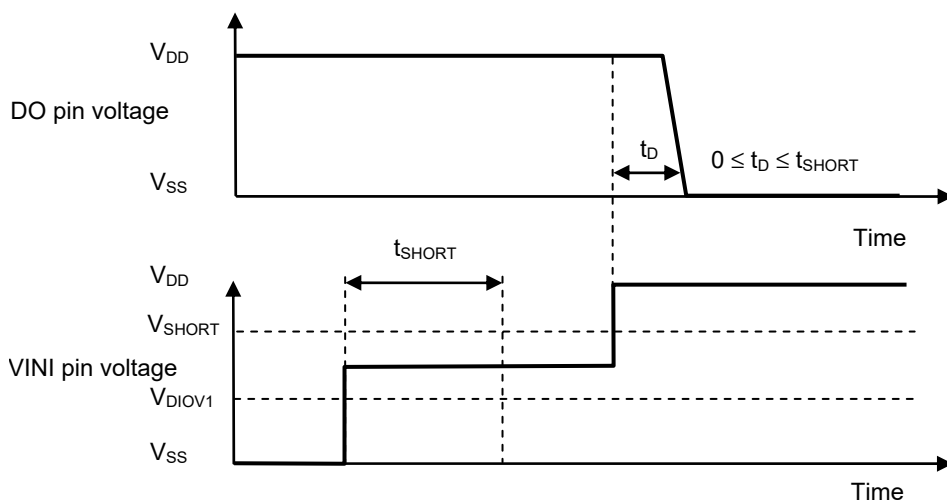
This function inhibits charging when a battery that is internally short-circuited (0 V battery) is connected. When the battery voltage is the 0 V battery charge inhibition battery voltage ( $V_{0INH}$ ) or lower, the charge control FET gate is fixed to the EB- pin voltage to inhibit charging. When the battery voltage is  $V_{0INH}$  or higher, charging can be performed.

**Caution Some battery providers do not recommend charging for a completely self-discharged lithium-ion rechargeable battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge.**

**9. Delay circuit**

The detection delay times are determined by dividing a clock of approximately 4 kHz by the counter.

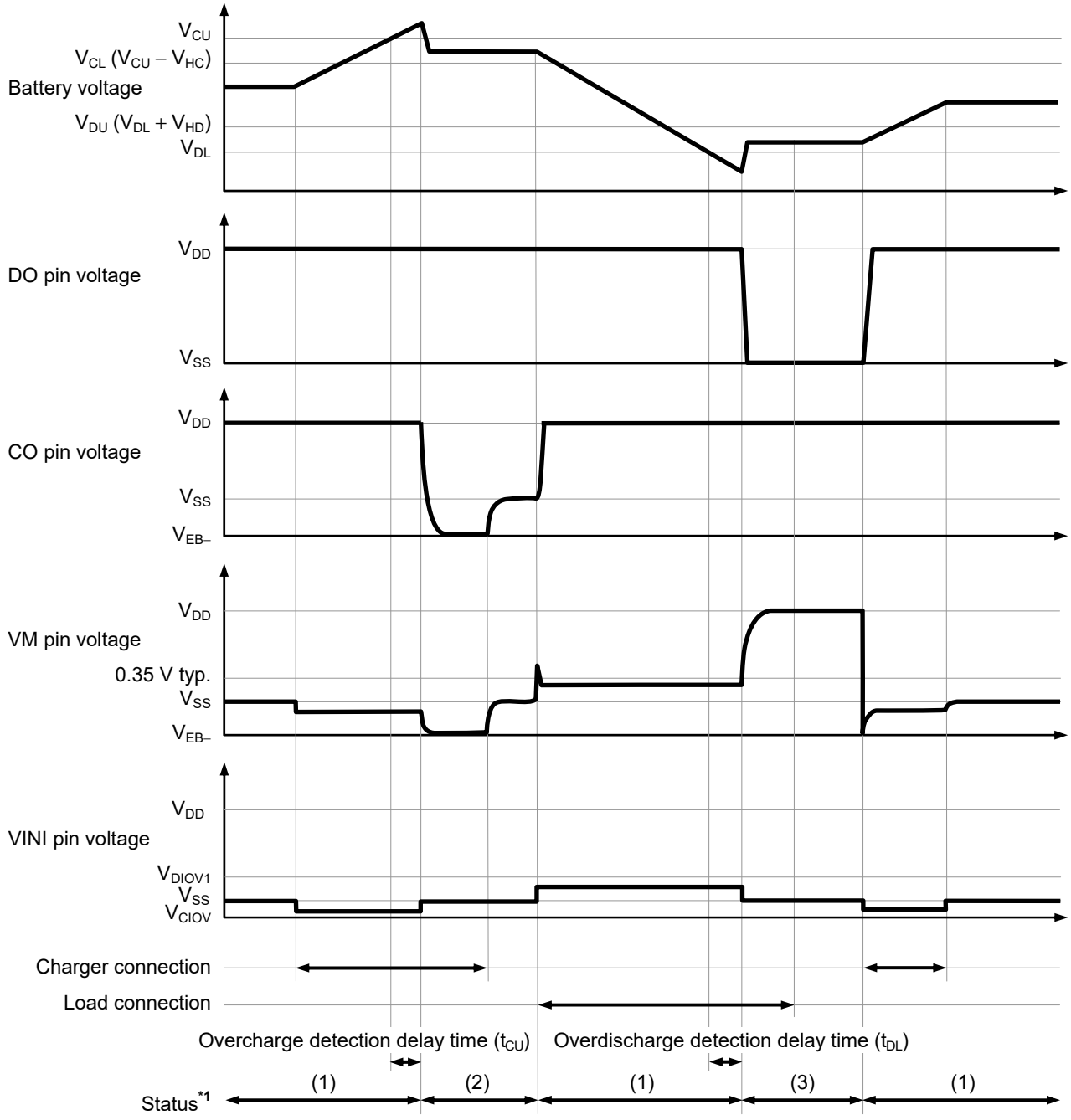
**Remark**  $t_{DIOV1}$ ,  $t_{DIOV2}$  and  $t_{SHORT}$  start when  $V_{DIOV1}$  is detected. When  $V_{DIOV2}$  or  $V_{SHORT}$  is detected over  $t_{DIOV2}$  or  $t_{SHORT}$  after the detection of  $V_{DIOV1}$ , the S-82K1A Series turns the discharge control FET off within  $t_{DIOV2}$  or  $t_{SHORT}$  of each detection.



**Figure 8**

■ Timing Charts

1. Overcharge detection, overdischarge detection

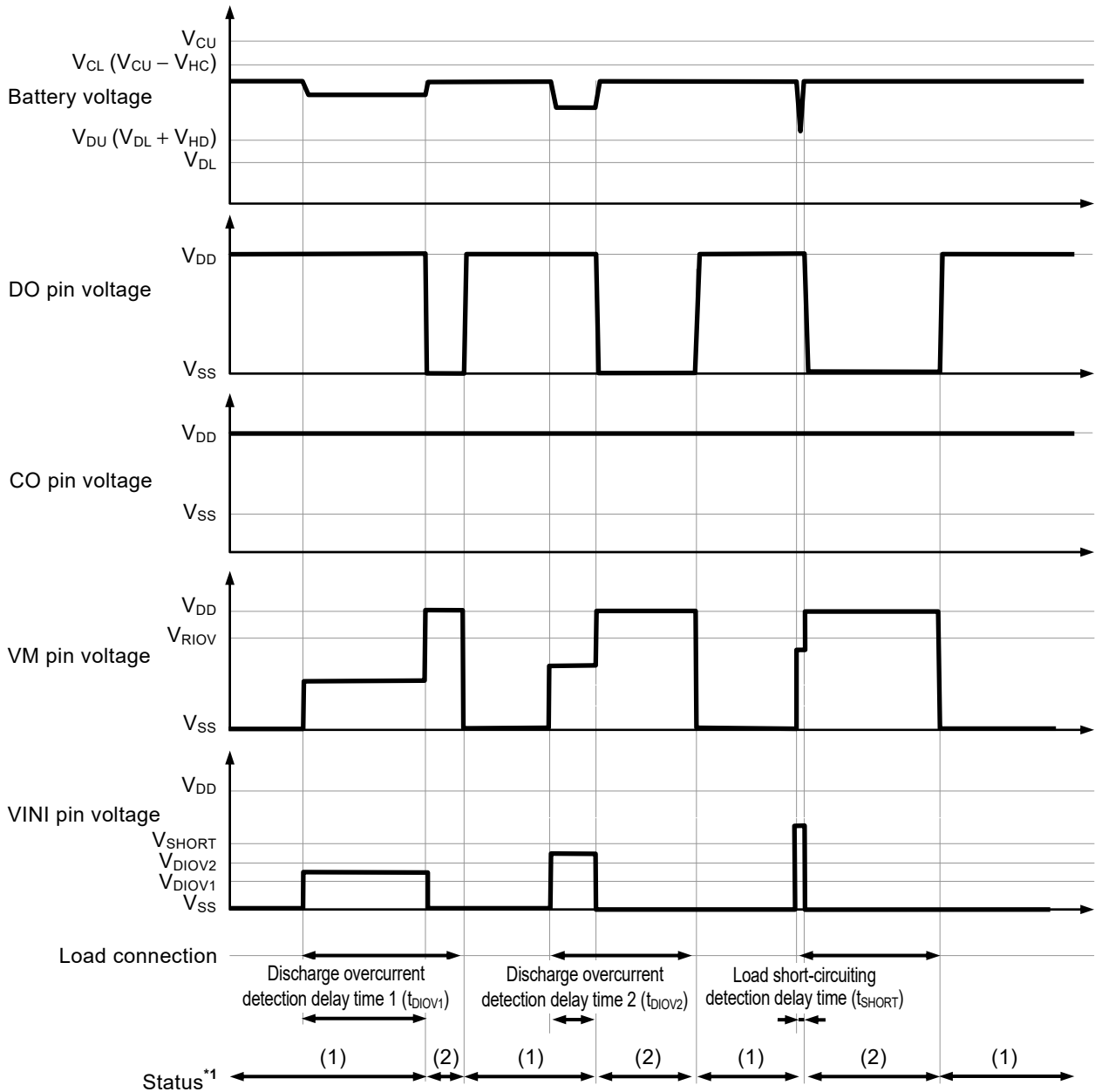


- \*1. (1): Normal status
- (2): Overcharge status
- (3): Overdischarge status

**Remark** The charger is assumed to charge with a constant current.

Figure 9

**2. Discharge overcurrent detection**

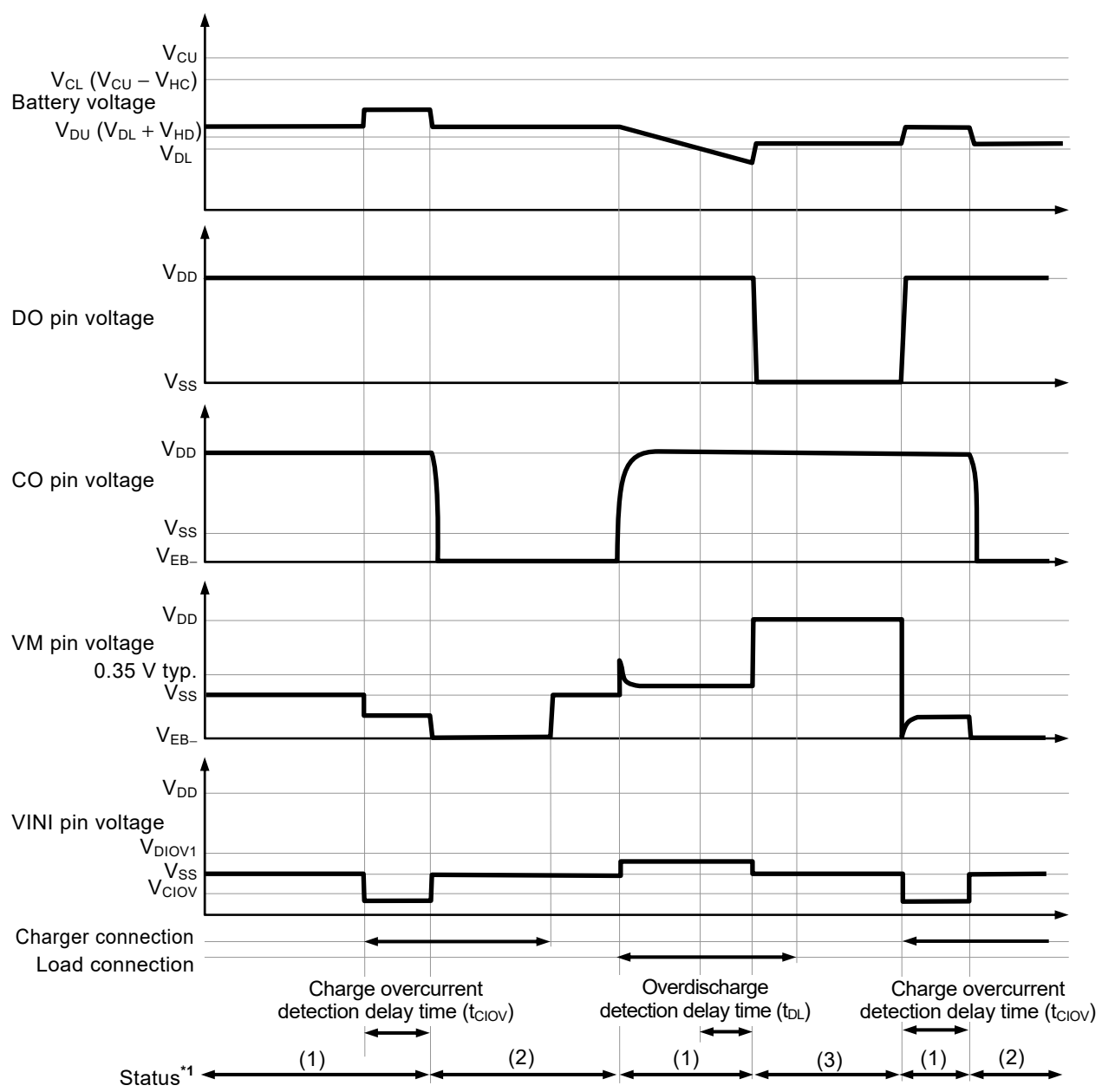


\*1. (1): Normal status  
 (2): Discharge overcurrent status

**Remark** The charger is assumed to charge with a constant current.

**Figure 10**

3. Charge overcurrent detection

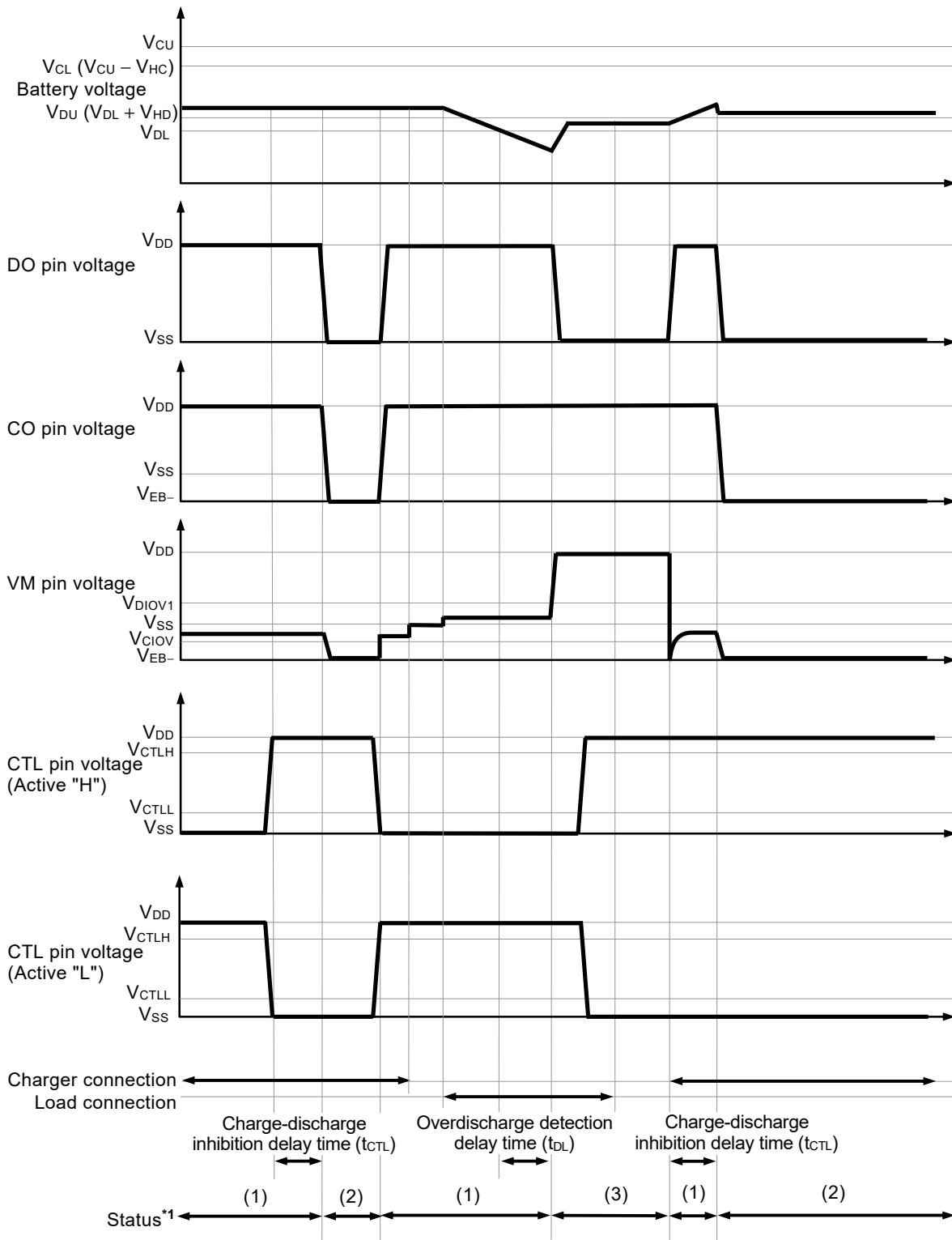


\*1. (1): Normal status  
 (2): Charge overcurrent status  
 (3): Overdischarge status

**Remark** The charger is assumed to charge with a constant current.

Figure 11

**4. Charge-discharge inhibition operation**



- \*1. (1): Normal status
- (2): Charge-discharge inhibition status
- (3): Overdischarge status

**Remark** The charger is assumed to charge with a constant current.

**Figure 12**

■ Battery Protection IC Connection Example

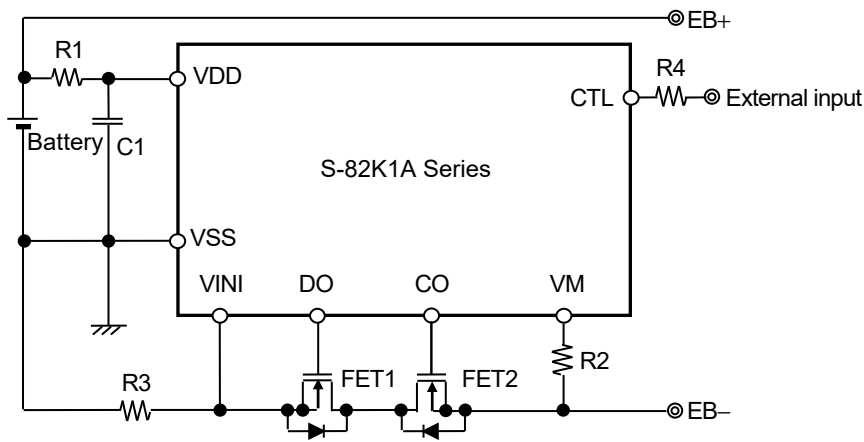


Figure 13

Table 8 Constants for External Components

| Symbol | Part              | Purpose  | Min.     | Typ.   | Max.     | Remark  |
|--------|-------------------|--|----------|--------|----------|---|
| FET1   | N-channel MOS FET | Discharge control  | -        | -      | -        | Threshold voltage ≤ Overdischarge detection voltage*1 |
| FET2   | N-channel MOS FET | Charge control   | -        | -      | -        | Threshold voltage ≤ Overdischarge detection voltage*1 |
| R1     | Resistor          | ESD protection, For power fluctuation                          | 270 Ω    | 330 Ω  | 1.2 kΩ*2 | -   |
| C1     | Capacitor         | For power fluctuation  | 0.068 μF | 0.1 μF | 2.2 μF   | -   |
| R2     | Resistor          | ESD protection, Protection for reverse connection of a charger | 300 Ω    | 470 Ω  | 1.5 kΩ   | -   |
| R3     | Resistor          | Overcurrent detection  | -        | 1.5 mΩ | -        | -   |
| R4     | Resistor          | CTL pin input protection                                       | -        | 1 kΩ   | -        | -   |

\*1. If a FET with a threshold voltage equal to or higher than the overdischarge detection voltage is used, discharging may be stopped before overdischarge is detected.

\*2. Accuracy of overcharge detection voltage is guaranteed by R1 = 330 Ω. Connecting resistors with other values will worsen the accuracy.

**Caution 1. The constants may be changed without notice.**

**2. It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.**

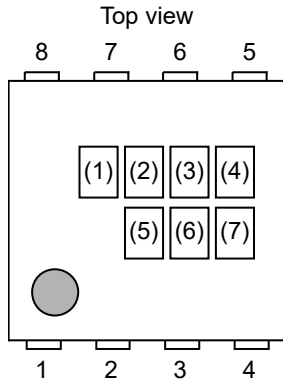
■ **Precautions**

- The application conditions for the input voltage, output voltage, and load current should not exceed the power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.



■ **Marking Specifications**

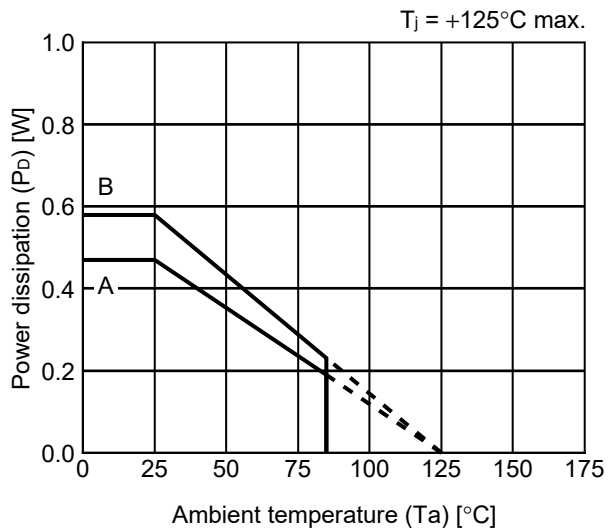
1. HSNT-8(1616)



- (1): Product code (Blank)
- (2) to (4): Product code
- (5) to (7): Lot number

■ Power Dissipation

HSNT-8(1616)

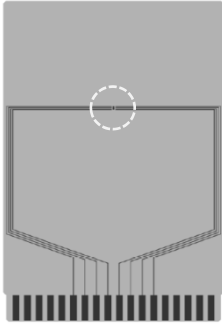


| Board | Power Dissipation (Pd) |
|-------|------------------------|
| A     | 0.47 W                 |
| B     | 0.58 W                 |
| C     | -                      |
| D     | -                      |
| E     | -                      |

# HSNT-8(1616) Test Board

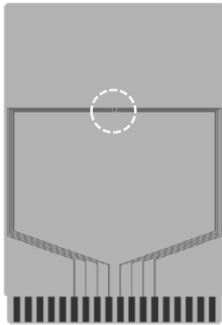
 IC Mount Area

(1) Board A



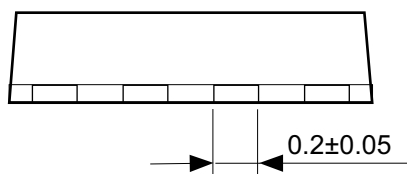
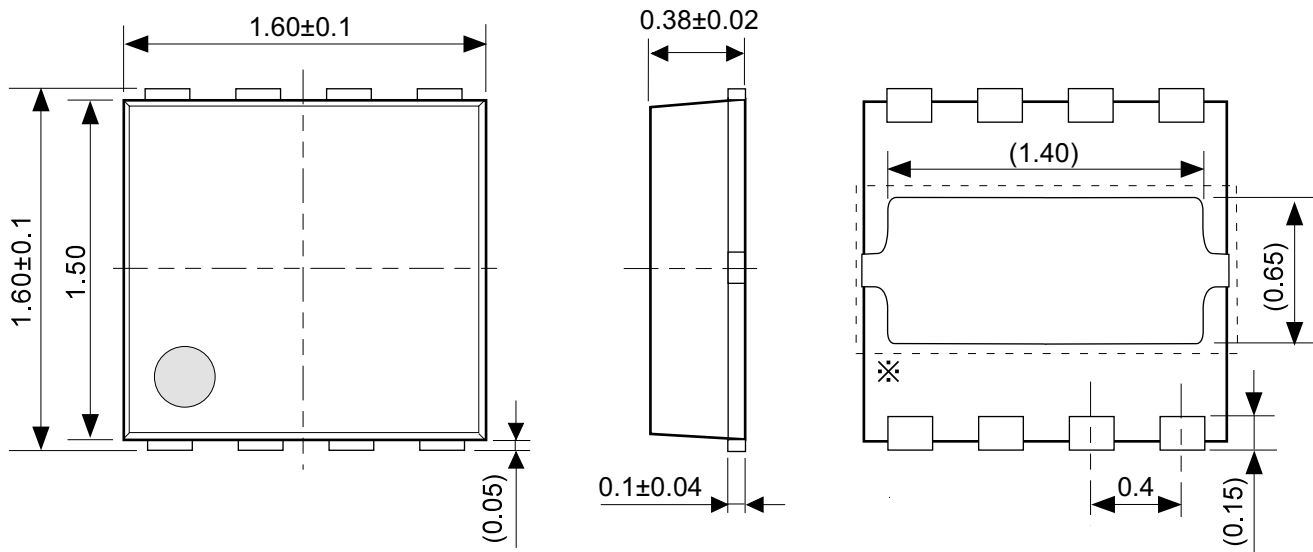
| Item                        | Specification       |   |
|-----------------------------|---------------------|---|
| Size [mm]                   | 114.3 x 76.2 x t1.6 |   |
| Material                    | FR-4                |   |
| Number of copper foil layer | 2                   |   |
| Copper foil layer [mm]      | 1                   | Land pattern and wiring for testing: t0.070 |
|                             | 2                   | -   |
|                             | 3                   | -   |
|                             | 4                   | 74.2 x 74.2 x t0.070                        |
| Thermal via                 | -                   |   |

(2) Board B



| Item                        | Specification       |   |
|-----------------------------|---------------------|---|
| Size [mm]                   | 114.3 x 76.2 x t1.6 |   |
| Material                    | FR-4                |   |
| Number of copper foil layer | 4                   |   |
| Copper foil layer [mm]      | 1                   | Land pattern and wiring for testing: t0.070 |
|                             | 2                   | 74.2 x 74.2 x t0.035                        |
|                             | 3                   | 74.2 x 74.2 x t0.035                        |
|                             | 4                   | 74.2 x 74.2 x t0.070                        |
| Thermal via                 | -                   |   |

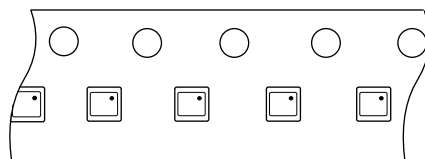
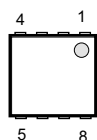
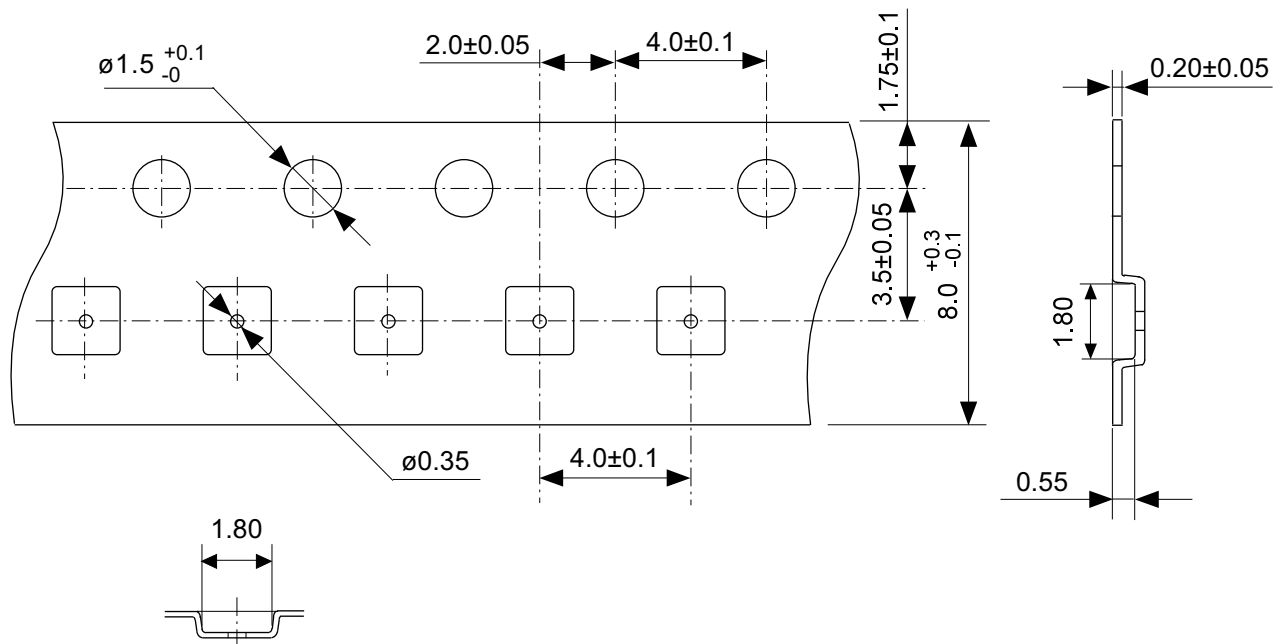
No. HSNT8-B-Board-SD-1.0



※ The heat sink of back side has different electric potential depending on the product.  
 Confirm specifications of each product.  
 Do not use it as the function of electrode.

No. PY008-A-P-SD-1.0

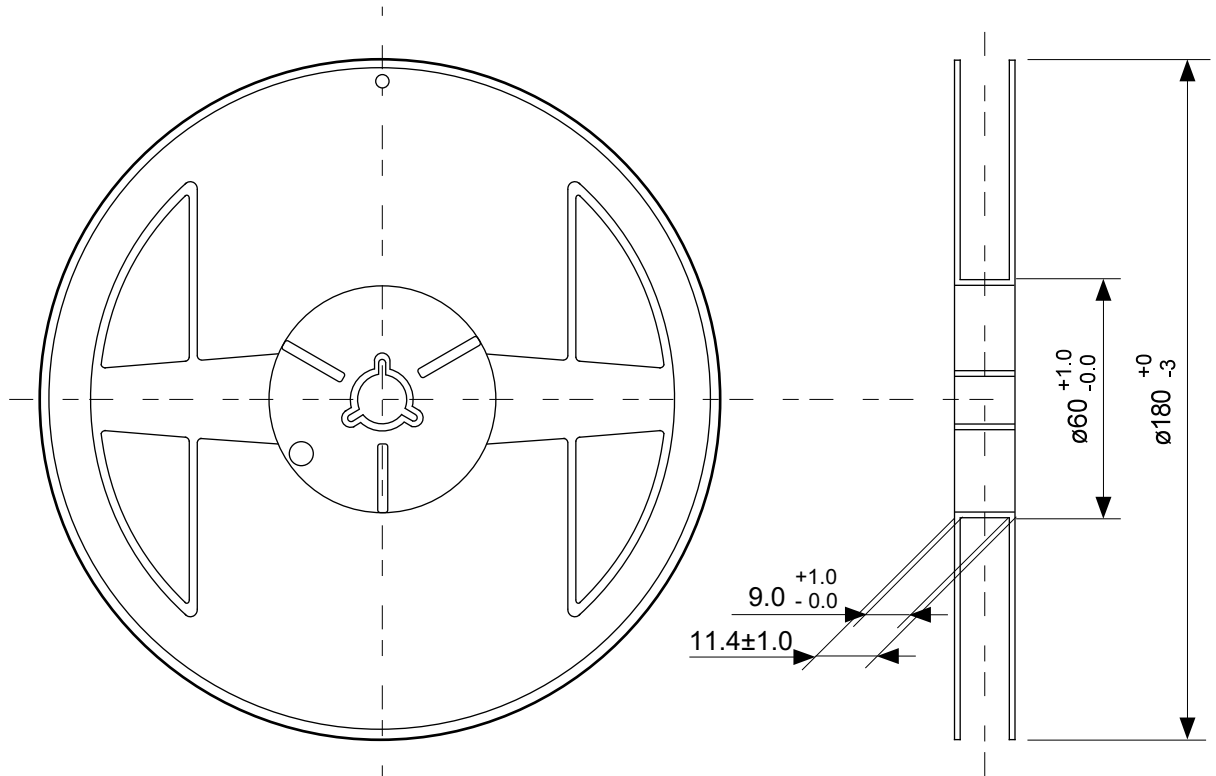
|                   |                         |
|-------------------|-------------------------|
| TITLE             | HSNT-8-B-PKG Dimensions |
| No.               | PY008-A-P-SD-1.0        |
| ANGLE             |                         |
| UNIT              | mm                      |
| <b>ABLIC Inc.</b> |                         |



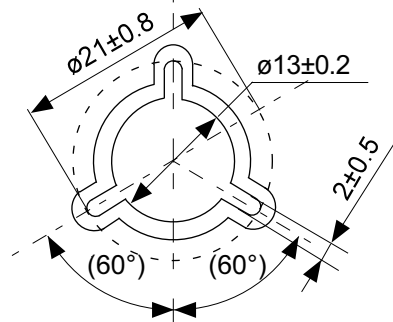
Feed direction →

No. PY008-A-C-SD-1.0

|                   |                       |
|-------------------|-----------------------|
| TITLE             | HSNT-8-B-Carrier Tape |
| No.               | PY008-A-C-SD-1.0      |
| ANGLE             |                       |
| UNIT              | mm                    |
|                   |                       |
| <b>ABLIC Inc.</b> |                       |



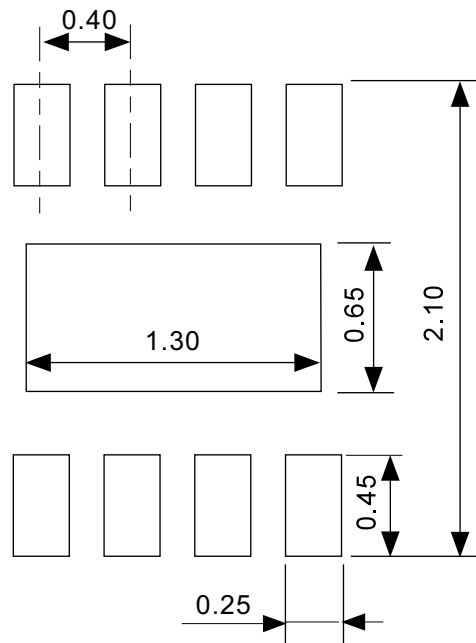
Enlarged drawing in the central part



No. PY008-A-R-SD-1.0

|                   |                  |      |       |
|-------------------|------------------|------|-------|
| TITLE             | HSNT-8-B-Reel    |      |       |
| No.               | PY008-A-R-SD-1.0 |      |       |
| ANGLE             |                  | QTY. | 5,000 |
| UNIT              | mm               |      |       |
|                   |                  |      |       |
| <b>ABLIC Inc.</b> |                  |      |       |

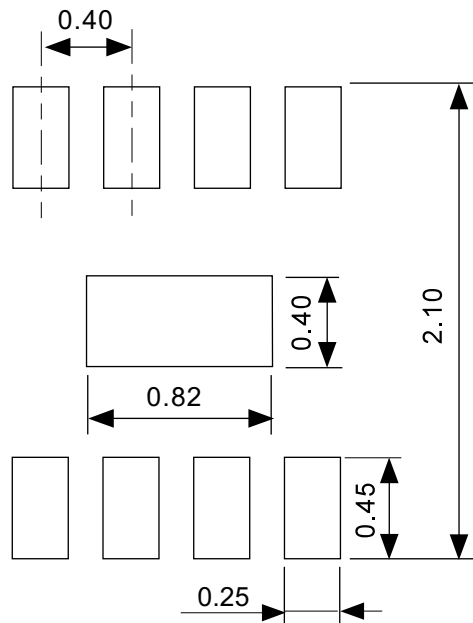
## Land Pattern



Caution It is recommended to solder the heat sink to a board in order to ensure the heat radiation.

注意 放熱性を確保する為に、PKGの裏面放熱板(ヒートシンク)を基板に半田付けする事を推奨いたします。

## Metal Mask Pattern



Caution ① Mask aperture ratio of the lead mounting part is 100%.  
 ② Mask aperture ratio of the heat sink mounting part is 40%.  
 ③ Mask thickness: t0.12 mm

注意 ①リード実装部のマスク開口率は100%です。  
 ②放熱板実装のマスク開口率は40%です。  
 ③マスク厚み : t0.12 mm

No. PY008-A-L-SD-1.0

|                   |                                  |
|-------------------|----------------------------------|
| TITLE             | HSNT-8-B<br>-Land Recommendation |
| No.               | PY008-A-L-SD-1.0                 |
| ANGLE             |                                  |
| UNIT              | mm                               |
|                   |                                  |
| <b>ABLIC Inc.</b> |                                  |

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2.4-2019.07