

General Description

- Trench Power MOSFET technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

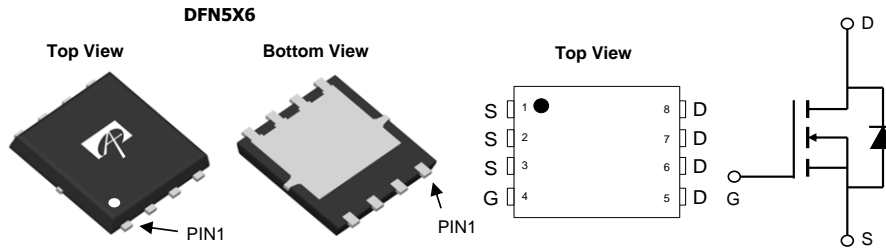
Applications

- DC/DC Converters in Computing, Servers, and POL
- Isolated DC/DC Converters in Telecom and Industrial
- See Note I

Product Summary

V_{DS}	30V
I_D (at $V_{GS}=10V$)	60A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 5.5m Ω
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 9.5m Ω

100% UIS Tested
 100% Rg Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONS36346	DFN 5x6	Tape & Reel	3000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	60
		$T_C=100^\circ\text{C}$	38
Pulsed Drain Current ^C	I_{DM}	100	A
Continuous Drain Current	I_{DSM}	$T_A=25^\circ\text{C}$	26.5
		$T_A=70^\circ\text{C}$	21
Avalanche Current ^C	I_{AS}	42	A
Avalanche energy	E_{AS}	9	mJ
V_{DS} Spike	V_{SPIKE}	36	V
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	31
		$T_C=100^\circ\text{C}$	12.5
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	6.2
		$T_A=70^\circ\text{C}$	4
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	15	20	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Ambient ^{A D}		Steady-State	40	50
Maximum Junction-to-Case	$R_{\theta JC}$	3.1	4	$^\circ\text{C}/\text{W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
STATIC PARAMETERS							
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V	
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA	
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.2	1.65	2.1	V	
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A		4.5	5.5	mΩ	
		T _J =125°C		6.6	8		
		V _{GS} =4.5V, I _D =20A		7.5	9.5	mΩ	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		54		S	
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V	
I _S	Maximum Body-Diode Continuous Current				40	A	
DYNAMIC PARAMETERS							
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		800		pF	
C _{oss}	Output Capacitance			240		pF	
C _{rss}	Reverse Transfer Capacitance			35		pF	
R _g	Gate resistance	f=1MHz	0.5	1	1.5	Ω	
SWITCHING PARAMETERS							
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A		10	20	nC	
Q _g (4.5V)	Total Gate Charge			5	10	nC	
Q _{gs}	Gate Source Charge			2		nC	
Q _{gd}	Gate Drain Charge			2		nC	
t _{D(on)}	Turn-On DelayTime				5		ns
t _r	Turn-On Rise Time	V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3Ω		2.5		ns	
t _{D(off)}	Turn-Off DelayTime				17		ns
t _f	Turn-Off Fall Time				2.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, di/dt=500A/μs		10		ns	
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, di/dt=500A/μs		13		nC	

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{D(SM)} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=150° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

I. For application requiring slow >1ms turn-on/turn-off, please consult AOS FAE for proper product selection.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

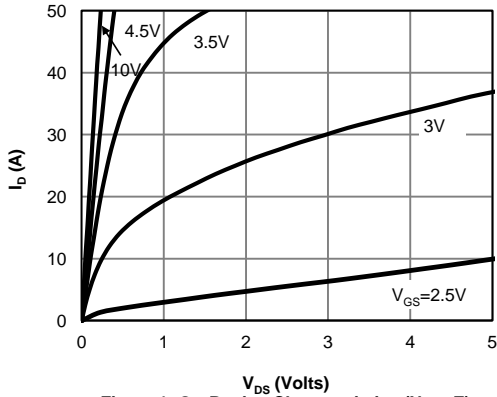


Figure 1: On-Region Characteristics (Note E)

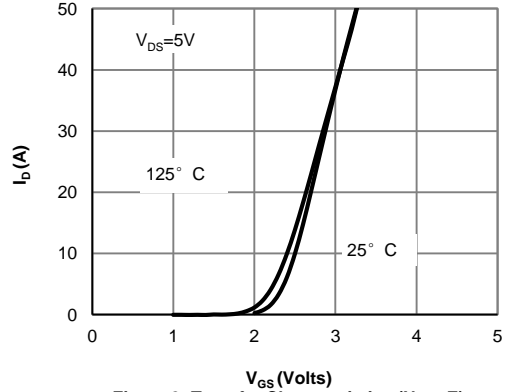


Figure 2: Transfer Characteristics (Note E)

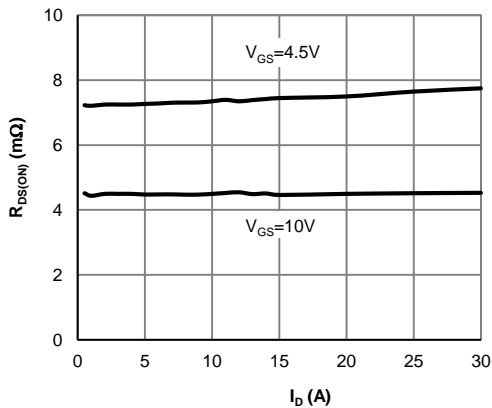


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

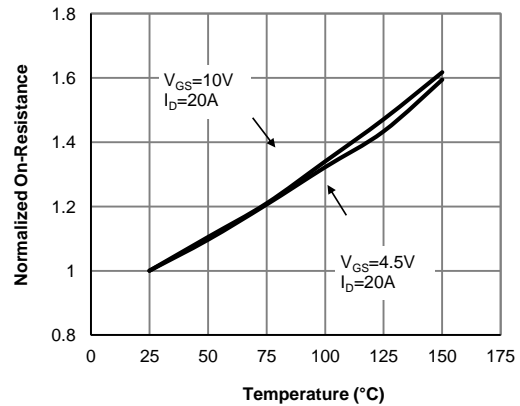


Figure 4: On-Resistance vs. Junction Temperature (Note E)

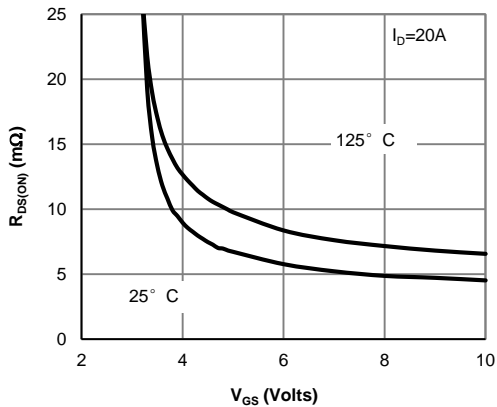


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

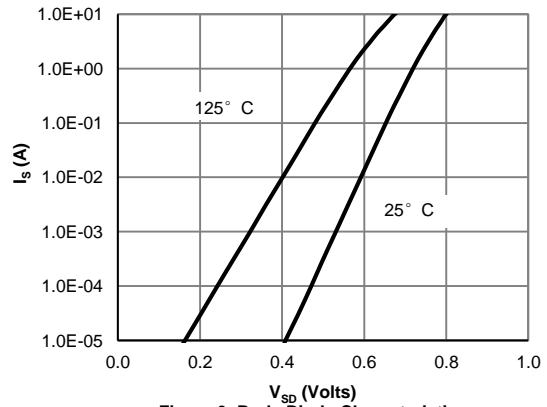


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

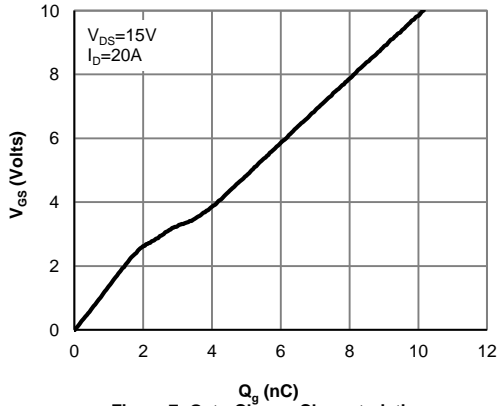


Figure 7: Gate-Charge Characteristics

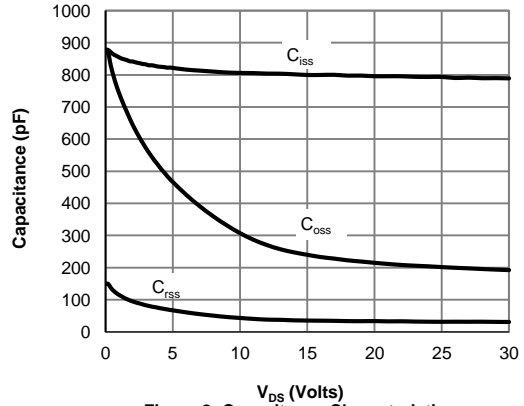


Figure 8: Capacitance Characteristics

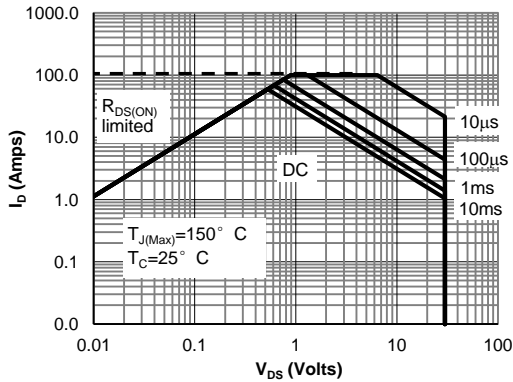


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

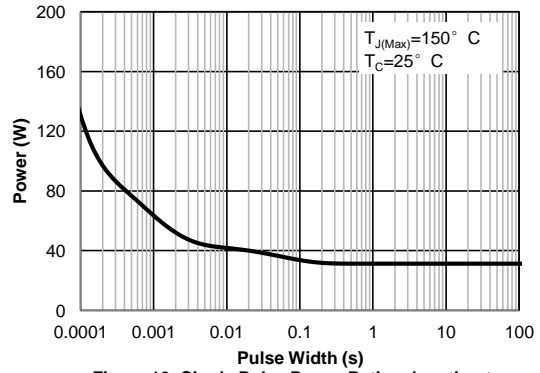


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

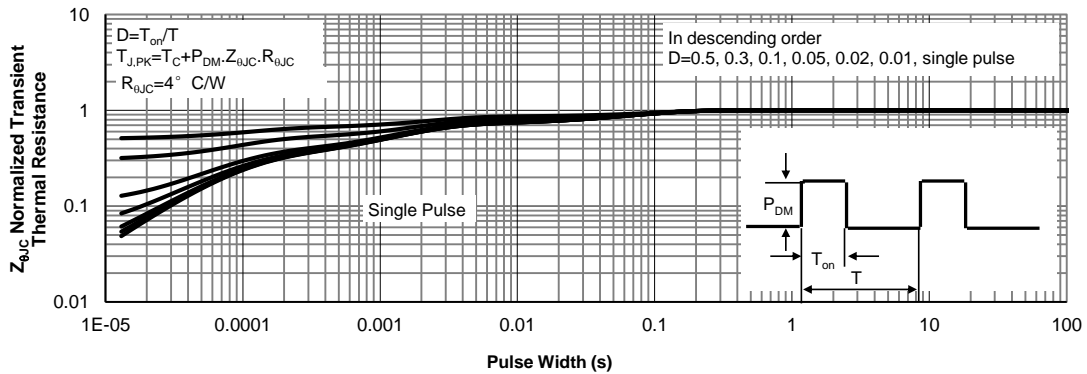


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

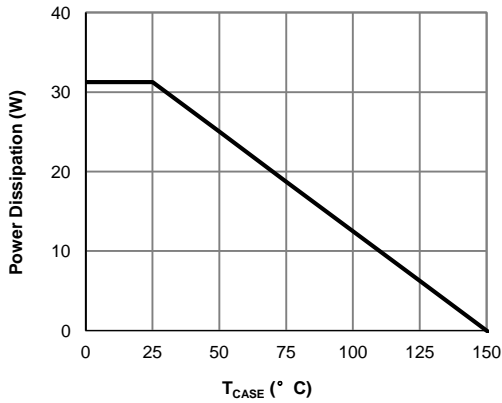


Figure 12: Power De-rating (Note F)

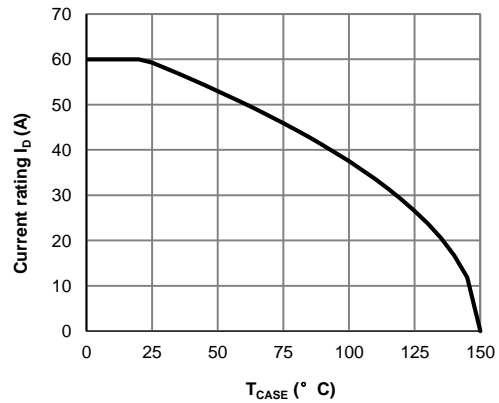


Figure 13: Current De-rating (Note F)

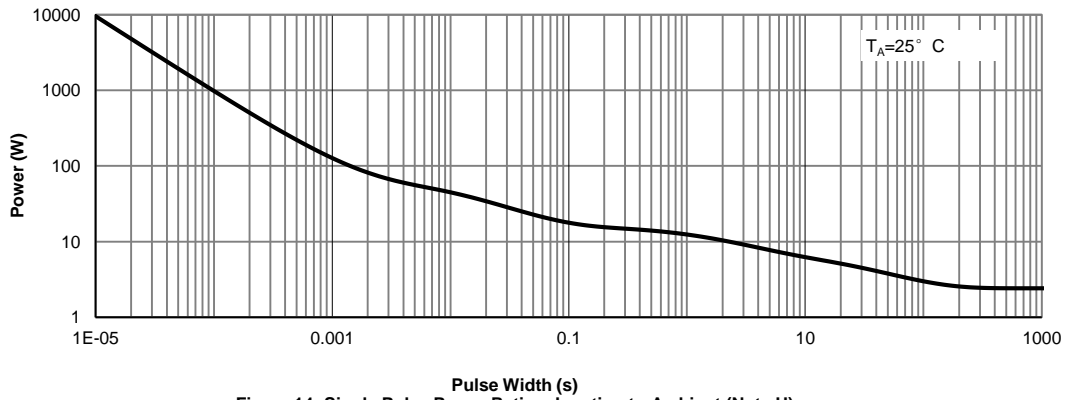


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

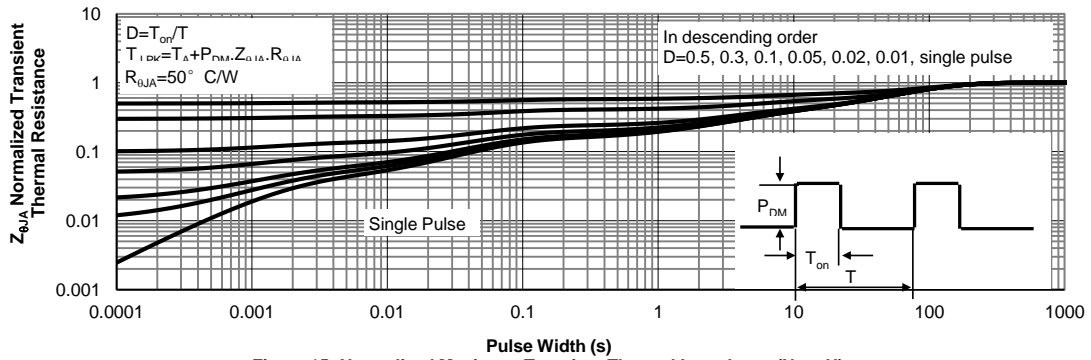


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

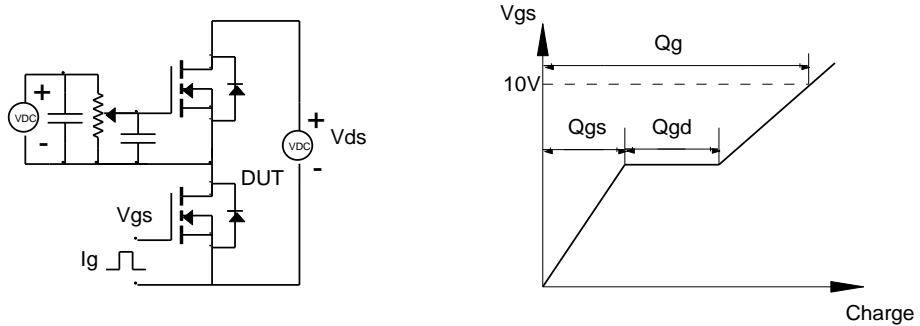


Figure B: Resistive Switching Test Circuit & Waveforms

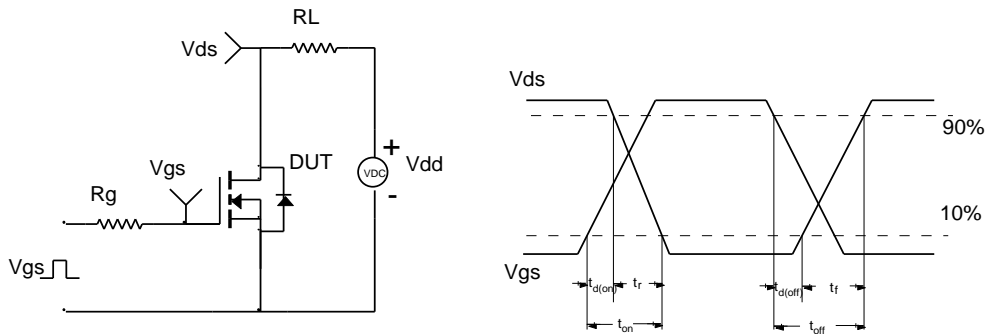


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

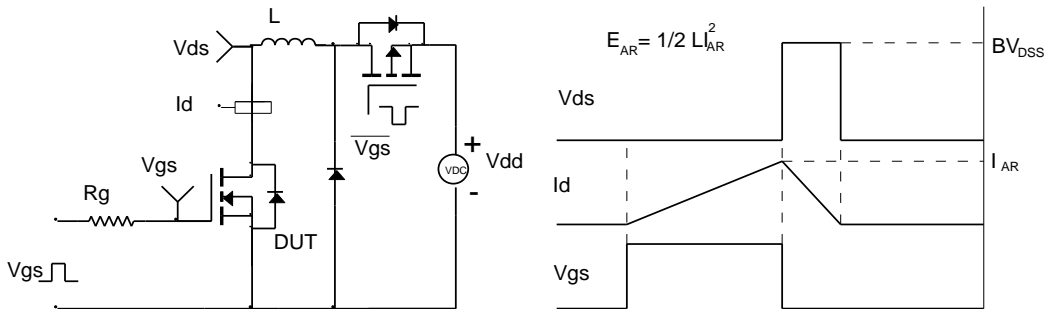


Figure D: Diode Recovery Test Circuit & Waveforms

