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FDP039N08B

N-Channel PowerTrench® MOSFET

80 V, 171 A, 3.9 mΩ

Features

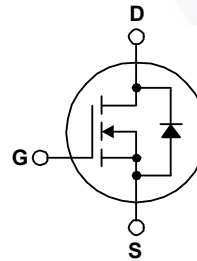
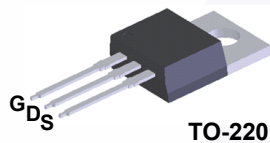
- $R_{DS(on)} = 3.16 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 100 \text{ A}$
- Low FOM $R_{DS(on)} * Q_G$
- Low Reverse-Recovery Charge, $Q_{rr} = 87.9 \text{ nC}$
- Soft Reverse-Recovery Body Diode
- Enables High Efficiency in Synchronous Rectification
- Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDP039N08B_F102	Unit
V_{DSS}	Drain to Source Voltage	80	V
V_{GSS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$, Silicon Limited)	171*
		- Continuous ($T_C = 100^\circ\text{C}$, Silicon Limited)	121*
		- Continuous ($T_C = 25^\circ\text{C}$, Package Limited)	120
I_{DM}	Drain Current	- Pulsed (Note 1)	684
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	547
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	6.0
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	214
		- Derate Above 25°C	1.43
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

* Package limitation current is 120A.

Thermal Characteristics

Symbol	Parameter	FDP039N08B_F102	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.7	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP039N08B_F102	FDP039N08B	TO-220	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	80	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	-	0.089	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 64 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 64 \text{ V}, T_C = 150^\circ\text{C}$	-	-	1 500	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	2.5	-	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 100 \text{ A}$	-	3.16	3.9	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 100 \text{ A}$	-	180	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$	-	7105	9450	pF
C_{oss}	Output Capacitance		-	1110	1475	pF
C_{rSS}	Reverse Transfer Capacitance		-	30	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$	-	1656	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 40 \text{ V}, I_D = 100 \text{ A},$ $V_{GS} = 10 \text{ V}$	-	102	133	nC
Q_{gs}	Gate to Source Gate Charge		-	39.9	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	22	-	nC
$V_{plateau}$	Gate Plateau Voltage		(Note 4)	-	5.6	-
Q_{sync}	Total Gate Charge Sync.	$V_{DS} = 0 \text{ V}, I_D = 50 \text{ A}$	-	87.4	-	nC
Q_{oss}	Output Charge	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$	-	99.2	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40 \text{ V}, I_D = 100 \text{ A},$ $V_{GS} = 10 \text{ V}, R_G = 4.7 \Omega$	-	36	82	ns
t_r	Turn-On Rise Time		-	49	108	ns
$t_{d(off)}$	Turn-Off Delay Time		-	71	152	ns
t_f	Turn-Off Fall Time		(Note 4)	-	29	68
ESR	Equivalent Series Resistance (G-S)	$f = 1 \text{ MHz}$	-	2.2	-	Ω

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	171*	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	684	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 100 \text{ A}$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, V_{DD} = 40 \text{ V}, I_{SD} = 100 \text{ A},$ $di_F/dt = 100 \text{ A}/\mu\text{s}$	-	70.1	-	ns
Q_{rr}	Reverse Recovery Charge		-	87.9	-	nC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $L = 3 \text{ mH}, I_{AS} = 19.1 \text{ A}$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 100 \text{ A}, di/dt \leq 200 \text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

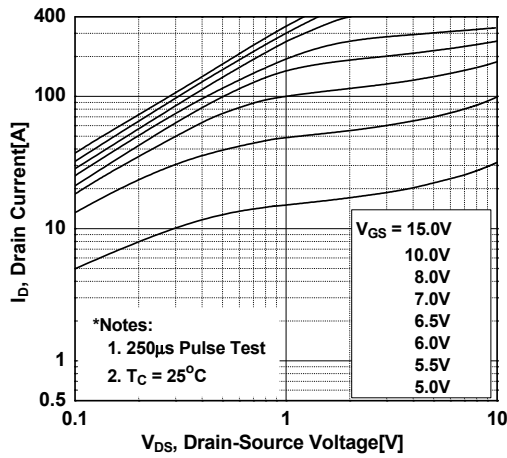


Figure 2. Transfer Characteristics

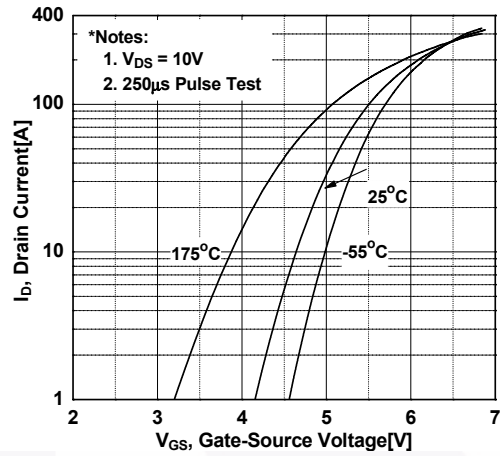


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

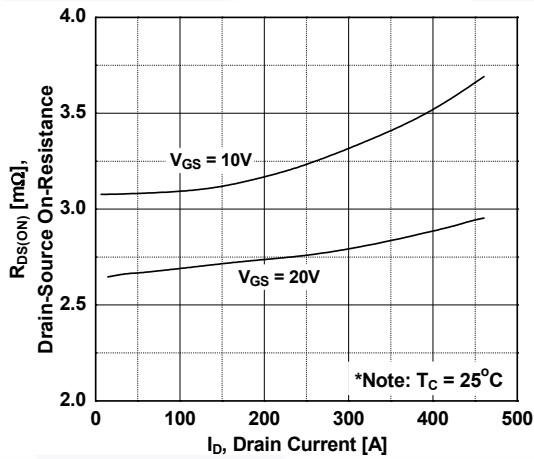


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

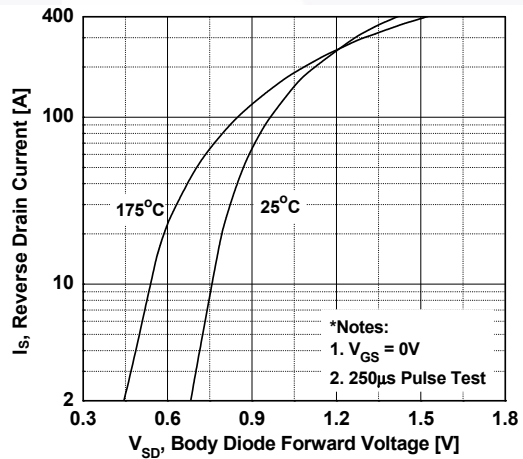


Figure 5. Capacitance Characteristics

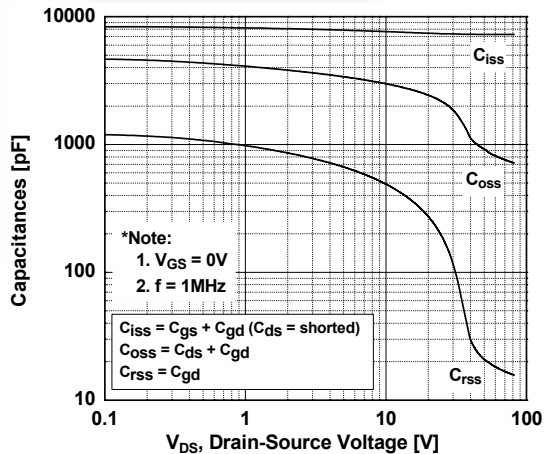
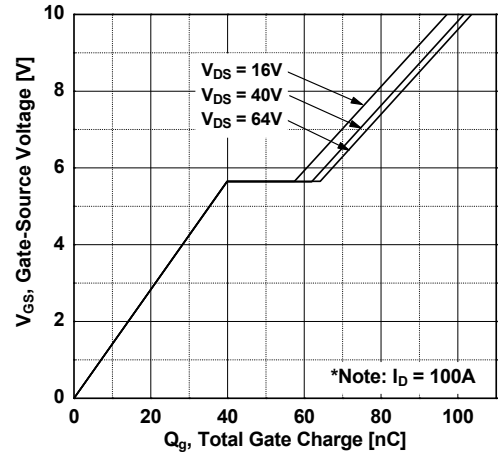


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

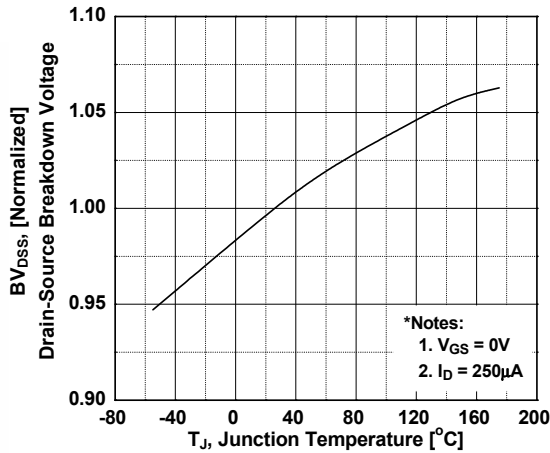


Figure 8. On-Resistance Variation vs. Temperature

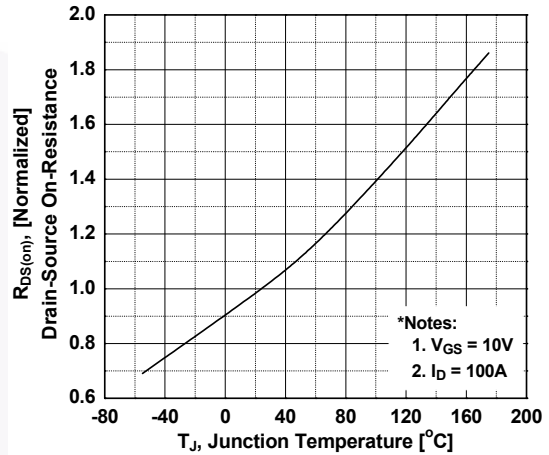


Figure 9. Maximum Safe Operating Area

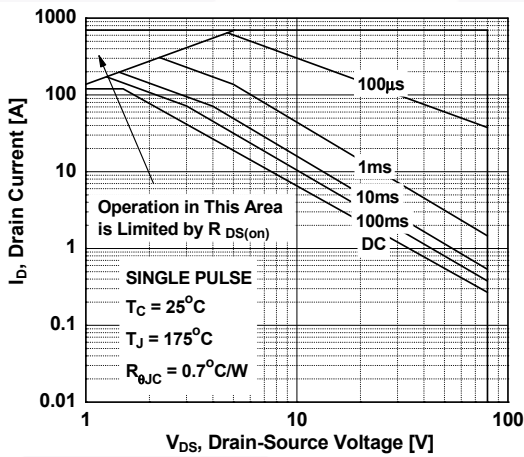


Figure 10. Maximum Drain Current vs. Case Temperature

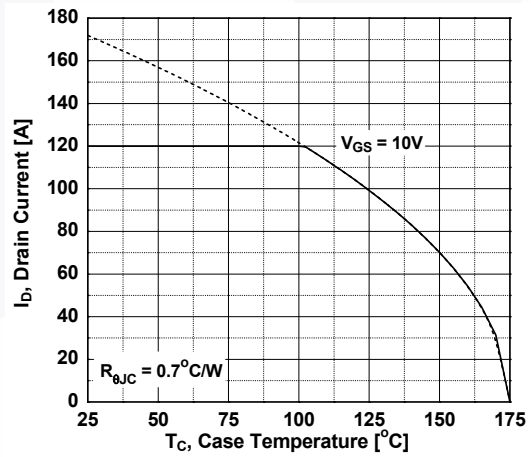


Figure 11. E_oss vs. Drain to Source Voltage

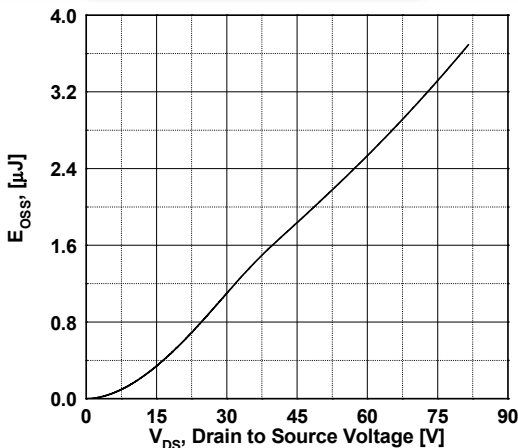
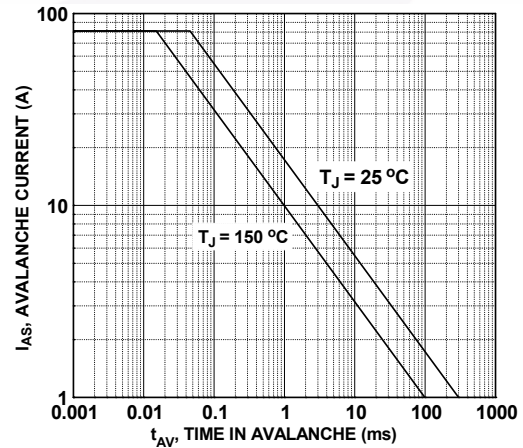
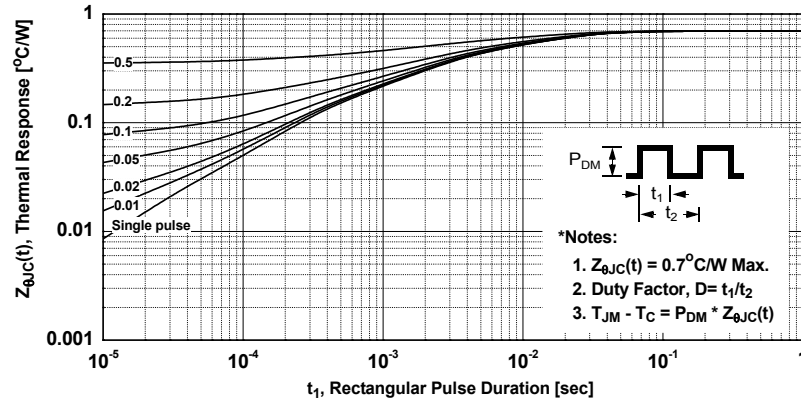


Figure 12. Unclamped Inductive Switching Capability



Typical Performance Characteristics (Continued)

Figure 13. Transient Thermal Response Curve



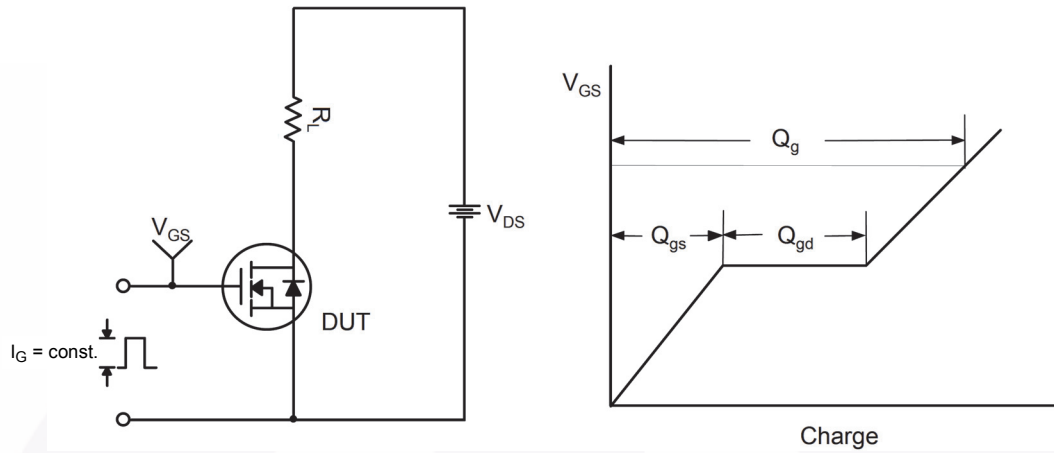


Figure 14. Gate Charge Test Circuit & Waveform



Figure 15. Resistive Switching Test Circuit & Waveforms



Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

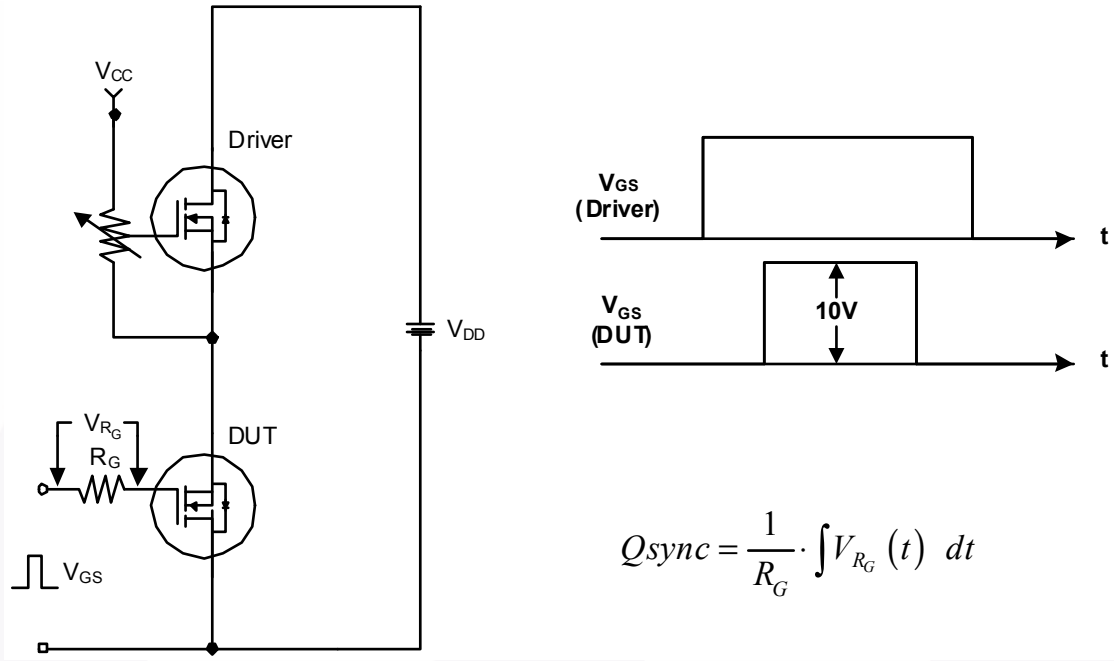


Figure 18. Total Gate Charge Q_{sync} . Test Circuit & Waveforms



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