

#### **Features**

- ESD Protection for 1 Line with Bi-directional.
- Provide ESD protection for each line to
   IEC 61000-4-2 (ESD) ±16kV (air / contact)
   IEC 61000-4-5 (Lightning) 4A (8/20µs)
- Ultra low capacitance: 0.5pF typical
- Suitable for, 5V and below, operating voltage applications
- 0201 small CSP package saves board space
- Protect one I/O line or one power line
- Fast turn-on and low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- Green part

## **Applications**

- Mobile Phones
- Hand Held Portable Applications
- Computer Interfaces Protection
- Microprocessors Protection
- Serial and Parallel Port Protection
- Control Signal Lines Protection
- Power Lines on PCB Protection
- Latchup Protection

## **Description**

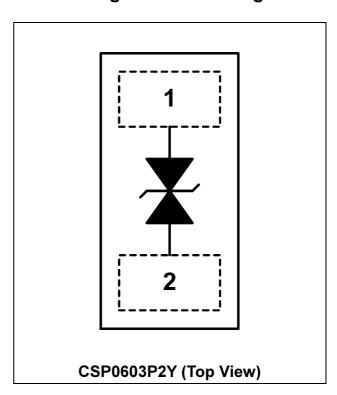
AZ5B85-01B is a design which includes a bi-directional ESD rated clamping cell to protect one power line, or one control line, or one high speed data line in an electronic system. The AZ5B85-01B has been specifically designed to protect sensitive components which are

connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD), Lightning, and Cable Discharge Event (CDE).

AZ5B85-01B is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ5B85-01B may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

## Circuit Diagram / Pin Configuration





## **SPECIFICATIONS**

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	RATING	UNITS	
Peak Pulse Current (tp =8/20μs)	$I_{PP}$	4	А	
Operating Supply Voltage (pin-1 to pin-2)	$V_{DC}$	±5.5	V	
Pin-1 to pin-2 ESD per IEC 61000-4-2 (Air)	V <sub>ESD-1</sub>	±16	kV	
Pin-1 to pin-2 ESD per IEC 61000-4-2 (Contact)	$V_{ESD-2}$	±16		
Lead Soldering Temperature	T <sub>SOL</sub>	260 (10 sec.)	°C	
Operating Temperature	T <sub>OP</sub>	-55 to +85	°C	
Storage Temperature	T <sub>STO</sub>	-55 to +150	°C	

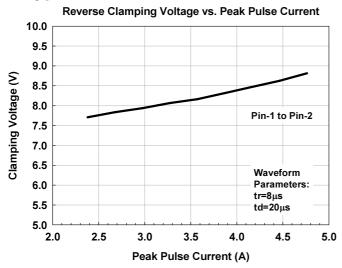
ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MINI	TYP	MAX	UNITS
Reverse						
Stand-Off	$V_{RWM}$	T=25 °C.	-5		5	V
Voltage						
Reverse		/			100	^
Leakage Current	l <sub>Leak</sub>	$V_{RWM} = \pm 5V$ , T=25 °C.			100	nA
Reverse						
Breakdown	$V_{BV}$	I <sub>BV</sub> = 1mA, T=25 °C.	6		9	V
Voltage						
ESD Clamping	\/	IEC 61000-4-2 +8kV (I <sub>TLP</sub> = 16A),		11		V
Voltage (Note 1)	$V_{\sf clamp}$	Contact mode, T=25 °C.		11		V
ESD Dynamic		IFC 64000 4 2 0 1912/ T=25 °C				
Turn-on	R <sub>dynamic</sub>	IEC 61000-4-2 0~+8kV, T=25 °C,		0.25		Ω
Resistance		Contact mode.				
Channel Input	C	V <sub>R</sub> = 2.5V, f = 1MHz, T=25 °C.		0.5	0.65	nE
Capacitance	C <sub>IN</sub>	V <sub>R</sub> - 2.5V, I - IIVIIIZ, I - 25 °C.		0.5	0.65	pF

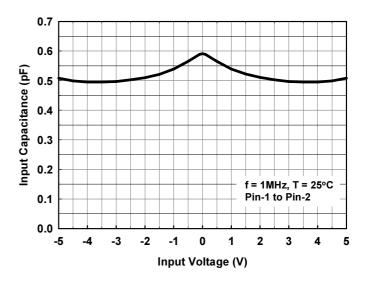
Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

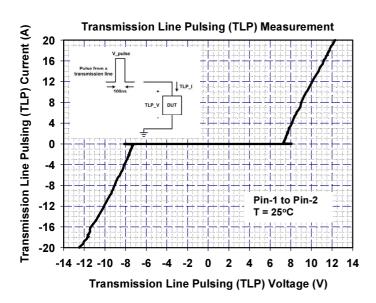
TLP conditions:  $Z_0$ = 50 $\Omega$ ,  $t_p$ = 100ns,  $t_r$ = 1ns.

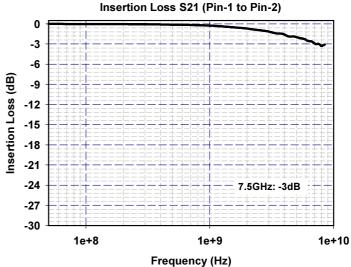


## **Typical Characteristics**











## **Applications Information**

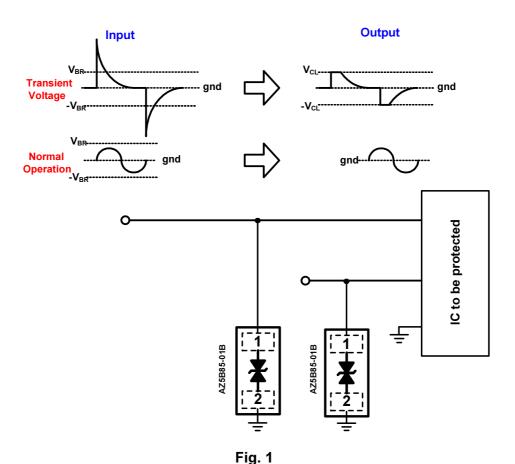
The AZ5B85-01B is designed to protect one line against System ESD/Lightning pulses by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ5B85-01B is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin 2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ5B85-01B should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ5B85-01B.
- Place the AZ5B85-01B near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.

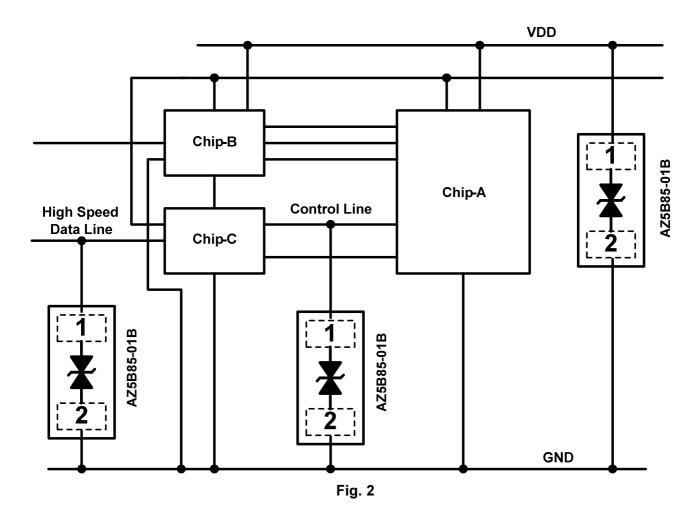
NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.



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Fig. 2 shows another simplified example of using AZ5B85-01B to protect the control line, high

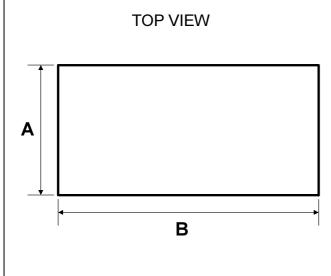
speed data line, and power line from ESD transient stress.



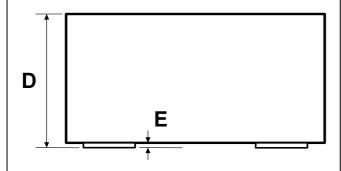
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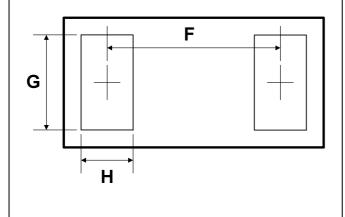
# Mechanical Details CSP0603P2Y PACKAGE DIAGRAMS







**BOTTOM VIEW** 

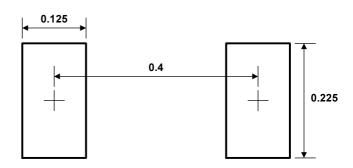


#### **PACKAGE DIMENSIONS**

Symbol	Millimeters			
	MIN.	TYP.	MAX.	
Α	0.275	0.300	0.325	
В	0.575	0.600	0.625	
D	0.256	0.276	0.296	
E		0.011		
F		0.400		
G	0.210	0.220	0.230	
Н	0.110	0.120	0.130	

### LAND LAYOUT

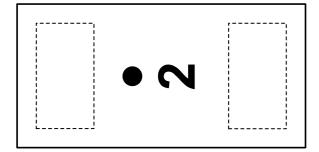
#### Unit: mm



#### Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

## **MARKING CODE**



Part Number	Marking Code		
AZ5B85-01B.R7G	2		
(Green Part)	۷		

Note: Green means Pb-free, RoHS, and Halogen free compliant.

2 = Device Code

# **Ordering Information**

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ5B85-01B.R7G	Green	T/R	7 inch	15,000/reel	4  reels = 60,000/box	6 boxes = 360,000/carton

# **Revision History**

Revision	Modification Description
Revision 2015/07/17	Preliminary Release.
Revision 2015/10/06	Update the maximum spec. of Leakage Current.
Revision 2016/03/16	Formal Release.