TEXAS INSTRUMENTS

TPA0172
Audio Power Amplifier Evaluation Module

User's Guide

February 2001

Mixed-Signal Products

SLOU103A

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Preface

How to Use This Manual

This document contains the following chapters:

- Chapter 1—Introduction
- Chapter 2—Operation

Related Documentation From Texas Instruments

- ***TI Plug-N-Play Audio Amplifier Evaluation Platform*** (literature number SLOU011) provides detailed information on the evaluation platform and its use with TI audio evaluation modules.
- ***TPA0172 2-W Stereo Audio Power Amplifier With I^2C Bus*** (literature number SLOS327) This is the data sheet for the TPA0172 audio amplifier integrated circuit.

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This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

Contents

Figures

Tables

Chapter 1

Introduction

This chapter provides an overview of the Texas Instruments (TI) TPA0172 audio amplifier evaluation module (SLOP211). It includes a list of EVM features, a brief description of the module illustrated with a pictorial diagram, and a list of EVM specifications.

Topic **Page**

1.1 Feature Highlights

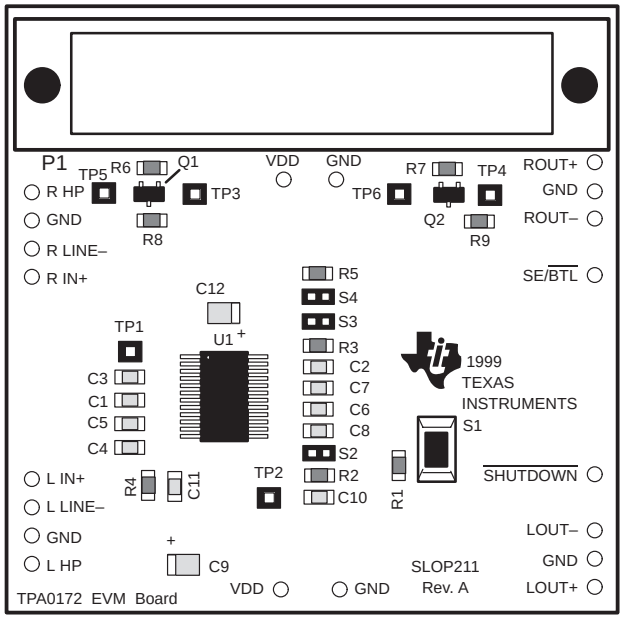
The TI TPA0172 audio amplifier evaluation module and the TI plug-n-play audio amplifier evaluation platform include the following features:

- TPA0172 Stereo 2-W Audio Power Amplifier Evaluation Module
  - I^2C Bus compatible
  - Internal depop circuitry to minimize transients in outputs
  - Powers up at mute volume level to avoid pop
  - Dual channel, bridge-tied load (BTL) or single-ended operation
  - 2 W per channel output power into 4 Ω at 5 V, BTL
  - Low current consumption in shutdown mode (15 μA)
  - Internal input MUX selects among two sets of stereo inputs
  - Digital volume control from +20 dB to –60 dB
  - Microprocessor mode volume control
  - Differential stereo inputs
  - PC beep input
- Quick and Easy Configuration with The TI Plug-N-Play Audio Amplifier Evaluation Platform
  - Evaluation module is designed to simply plug into the platform, automatically making all signal, control, and power connections
  - Platform provides flexible power options
  - Jumpers on the platform select power and module control options
  - Switches on the platform route signals
  - Platform provides quick and easy audio input and output connections
- Platform Power Options
  - External 5-V – 15-V DC V_{CC} supply inputs
  - External regulated V_{DD} supply input
  - Socket for onboard 5 V/3.3 V V_{DD} voltage regulator EVM
  - On-board overvoltage and reverse polarity power protection
- Platform Audio Input and Output Connections
  - Left and right RCA phono jack inputs
  - Miniature stereo phone jack input
  - Left and right RCA phono jack outputs
  - Left and right compression speaker terminal outputs
  - Miniature stereo headphone jack output

1.2 Description

The TPA0172 Stereo 2-W audio Ppower amplifier evaluation module is a complete, 2-Watt per channel stereo audio power amplifier. It consists of the TI TPA0172 Stereo 2-W audio power amplifier IC along with a small number of other parts and a D–25 connector mounted on a circuit board that measures approximately 2 1/4 inches by 2 1/4 inches (Figure 1–1).

Figure 1–1. The TI TPA0172 Audio Amplifier Evaluation Module



Single in-line header pins extend from the underside of the module circuit board to allow the EVM to be plugged into the TI plug-n-play audio amplifier evaluation platform, or to be wired directly into existing circuits and equipment when used stand-alone.

The platform has room for a single TPA0172 evaluation module and is a convenient vehicle for demonstrating TI's audio power amplifier and related evaluation modules. The EVMs simply plug into the platform, which automatically provides power to the modules, interconnects them correctly, and connects them to a versatile array of standard audio input and output jacks and connectors. Easy-to-use configuration controls allow the platform and EVMs to quickly model many possible end-equipment configurations.

There is nothing to build, nothing to solder, and nothing but the speakers included with the platform to *hook up*.

1.3 TPA0172 EVM Specifications

Supply voltage range, V_{DD}		4.5 V to 5.5 V
Supply current, I_{DD}		2 A max
Continuous output power per channel, P_O: 4-Ω BTL, V_{DD}=5 V		2 W
Audio input voltage, V_I:	HP input	5 Vpp max
	Line input	5 Vpp max
	PC Beep input	5 Vpp max
Minimum load impedance, R_L		3 Ω

Chapter 2

Operation

Quick start lists in this chapter contain steps that can be followed to quickly prepare the TI plug-n-play audio amplifier evaluation platform for use with the TPA0172 audio amplifier EVM, or to connect the TPA0172 audio amplifier EVM for stand-alone operation.

Using the TPA0172 audio amplifier evaluation module with the TI evaluation platform is a quick and easy way to connect power, signal and control inputs, and signal outputs to the EVM, using standard connectors.

The TPA0172 audio amplifier evaluation module can also be used stand-alone by making connections directly to the module pins, and it can be wired directly into existing circuits or equipment. A stand-alone connection diagram appears below.

A schematic, parts list, I^2C interface information, and PCB and layer illustrations for the EVM are included in the Reference section of this chapter.

Topic **Page**

2.1 Precautions

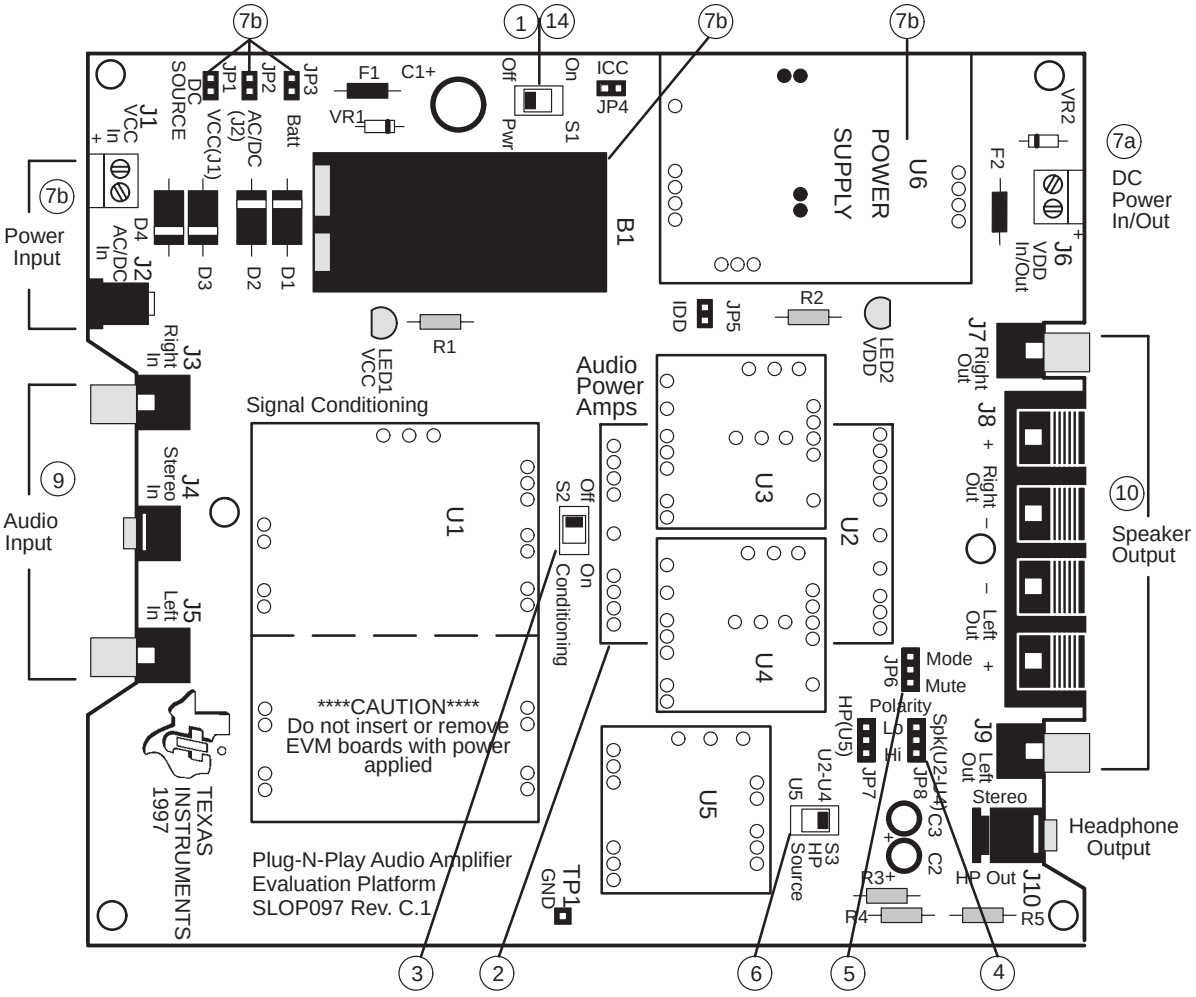
Power Supply Input Polarity and Maximum Voltage

Always ensure that the polarity and voltage of the external power connected to V_{CC} power input connector J1, J2, and/or V_{DD} power input connector J6 are correct. Overvoltage or reverse-polarity power applied to these terminals can open onboard soldered-in fuses and cause other damage to the platform, installed evaluation modules, and/or the power source.

Inserting or Removing EVM Boards

Do not insert or remove EVM boards with power applied—damage to the EVM board, the platform, or both may result.

Figure 2–1. Quick Start Platform Map



2.2 Quick Start List for Platform

Follow these steps when using the TPA0172 EVM with the TI plug-n-play audio amplifier evaluation platform (see the platform user's guide, SLOU011, for additional details). Typical platform switch and jumper settings are shown in Table 2–1 and typical EVM settings are shown in Table 2–2. Numbered callouts for selected steps are shown in Figure 2–1 and Figure 2–2.

❑ **Platform preparations**

Table 2–1. Platform Jumper and Switch Settings for the TPA0172

EVM	JP6	JP7	JP8	S2	S3
P-N-P Platform	Mode	X	Hi	Note 2	U2–U4

Notes: 1) X = Don't care
2) Set S2 to ***ON*** when signal conditioning board is installed in **U1**; set **S2** to *OFF* when no signal conditioning board is installed.

1) Ensure that all external power sources are set to *OFF* and that the platform power switch S1 is set to *OFF.*
2) Install a TPA0172 module in platform socket U2**,** taking care to align the module pins correctly.
3) Use switch S2 to select or bypass the signal conditioning EVM (U1).
4) Set control signal Polarity jumper JP8 to Hi**.**
5) Set jumper JP6 to select the *Mode* control input (causes the TPA0172 to switch to the single-ended output mode if a plug is inserted into platform headphone jack J10).
6) If the headphone Jack (J10) output will be used, set headphone source switch S3 to U2–U4.

❑ **Power supply**

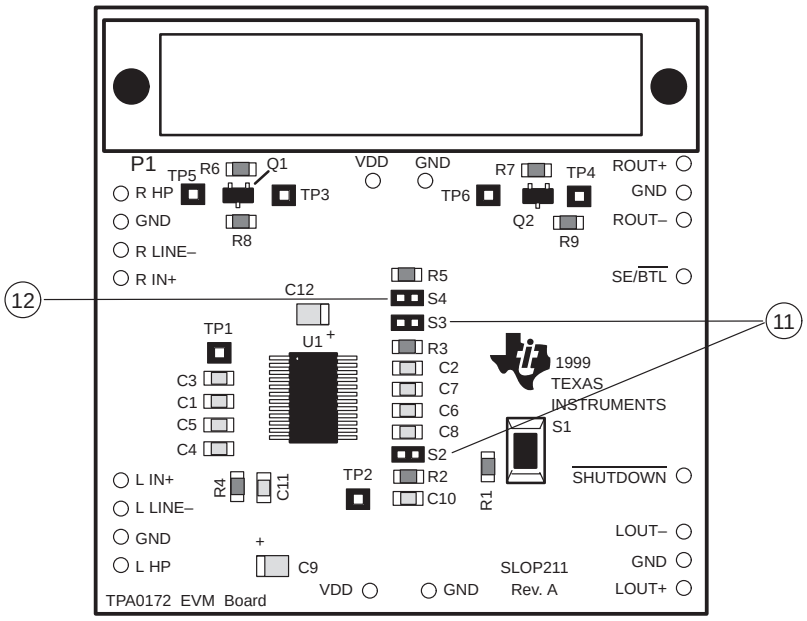
7) Select and connect the power supply (ensure power supply is set to *OFF*):
   a) Connect an external regulated power supply set to 5 V to platform V_{DD} power input connector J6 taking care to observe marked polarity, or
   b) Install a voltage regulator EVM (SLVP097 or equiv.) in platform socket U6. Connect a 7 V – 12 V power source to a platform V_{CC} power input J1 or J2 and jumper the appropriate power input (see platform user's guide).

❑ **Inputs and outputs**

8) Ensure that the audio signal source level is set to minimum.
9) Connect the audio source to left and right RCA phono jacks J3 and J5 or stereo miniature phone jack J4**.**
10) Connect speakers to left and right RCA jacks J7 and J9 or to stripped wire speaker connectors J8**.**

❑ Evaluation Module Preparations

Figure 2–2. Module Map



11) Jumpers S2 and S3 select the least significant bits of the EVM I^2C address. *See section 2.5.3 for details***.**

12) To allow the module SE/$\overline{\text{BTL}}$ control input to switch the amplifier IC between single ended (SE) and bridge-tied load (BTL) output modes, set output mode jumper S4 to *OFF*. To keep the module amplifier IC in the single-ended output mode regardless of the control input state, set jumper S4 to *ON*.

Table 2–2. Typical TPA0172 EVM Jumper Settings

EVM	S2	S3	S4
TPA0172	OFF	ON	ON

Note: ON = Shunt installed, OFF = Open

13) When the module powers up or comes out of shutdown, the gain is set at the –85 dB level. Gain settings can be adjusted through an I^2C interface, connecting to the EVM via connector P1 or through test point terminals TP3, TP4, TP5, and TP6 (Table 2–3). *See section 2.5.3 for details.*

Table 2–3. TPA0172 EVM Gain Control

CONNECTOR P1	TEST POINT TERMINAL	FUNCTION
Pin 1	TP6	SDA input
Pin 10	TP3	SCL output
Pin 14	TP5	SCL input
Pin 15	TP4	SDA output

❑ Power Up

14) Verify correct voltage and input polarity and set the external power supply to *ON*. If V_{CC} and an on-board regulator EVM are used to provide V_{DD}, set platform power switch S1 to *ON*.

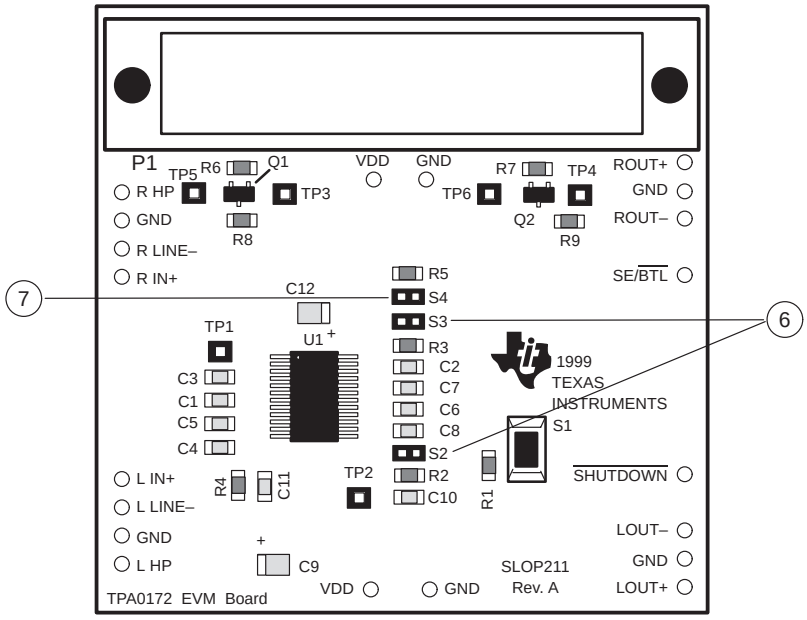
Platform LED2 should light indicating the presence of V_{DD}, and the evaluation modules installed on the platform should begin operation.

15) Adjust the signal source level as needed.

2.3 Quick Start List for Stand-Alone

Follow these steps to use the TPA0172 EVM stand-alone or when connecting it into existing circuits or equipment. Connections to the TPA0172 module header pins can be made via individual sockets, wire-wrapping, or soldering to the pins, either on the top or the bottom of the module circuit board. Typical EVM jumper settings are shown in Table 2–4. Numbered callouts for selected steps are shown in Figure 2–3.

Figure 2–3. Stand-Alone Module Map



❑ **Power supply**

1) Ensure that all external power sources are set to *OFF.*

2) Connect an external regulated power supply set to 5 V to the module VDD and GND pins taking care to observe marked polarity.

❑ **Inputs and outputs**

3) Ensure that audio signal source level adjustments are set to minimum.

4) Connect the right (left) positive lead of the audio source to the module R LINE– (L LINE–) pins and the negative lead to the R IN+ (L IN+) pins. If using the headphone inputs, connect the positive audio source to the module R HP (L HP) and the negative lead to R IN+ (L IN+)**.** The inputs can be used with a differential or single-ended audio source, but the headphone and line have common positive inputs.

5) Select output mode:

   a) For BTL output, connect a speaker to the module OUT+ and OUT– pins of each channel,
      or

   b) For single-ended output, connect a headphone or a speaker to the module OUT+ and GND pins of each channel through a 33 μF to 1000 μF output-coupling capacitor (Figure 3–10).

❑ **Evaluation Module Preparations**

6) Jumpers S2 and S3 select the least significant bits of the EVM I^2C address. *See section 2.5.3 for details***.**

7) To allow the module SE/$\overline{\text{BTL}}$ control input to switch the amplifier IC between single ended (SE) and bridge-tied load (BTL) output modes, set output mode jumper S4 to *OFF*. To keep the module amplifier IC in the single-ended output mode regardless of the control input state, set jumper S4 to *ON*.

Table 2–4. Typical TPA0172 EVM Jumper Settings

EVM	S2	S3	S4
TPA0172	OFF	ON	ON

Note: ON = Shunt installed, OFF = Open

8) When the module powers up or comes out of shutdown, the gain is set at the –85 dB level. Gain settings can be adjusted through an I^2C interface, connecting to the EVM via connector P1 or through test point terminals TP3, TP4, TP5, and TP6 (Table 2–5). To ensure a common ground path, connect a ground wire between a ground point on the I^2C transmitting device and GND on the EVM. *See section 2.5.3 for details.*

Table 2–5. TPA0172 EVM Gain Control

CONNECTOR P1	TEST POINT TERMINAL	FUNCTION
Pin 1	TP6	SDA input
Pin 10	TP3	SCL output
Pin 14	TP5	SCL input
Pin 15	TP4	SDA output

❑ **Control Inputs**

9) Connect control lines to the various module control input pins as needed:

   a) **SE/$\overline{\text{BTL}}$**: A high selects the single-ended (SE) output mode; a low or float selects the bridge-tied load (BTL) output mode.

   b) **$\overline{\text{SHUTDOWN}}$**: A low shuts down the amplifier IC on the module; a high or float allows normal operation.

❑ **Power-up**

10) Verify correct voltage and input polarity and set the external power supply to *ON***.**

The EVM should begin operation.

11) Adjust the signal source level as needed.

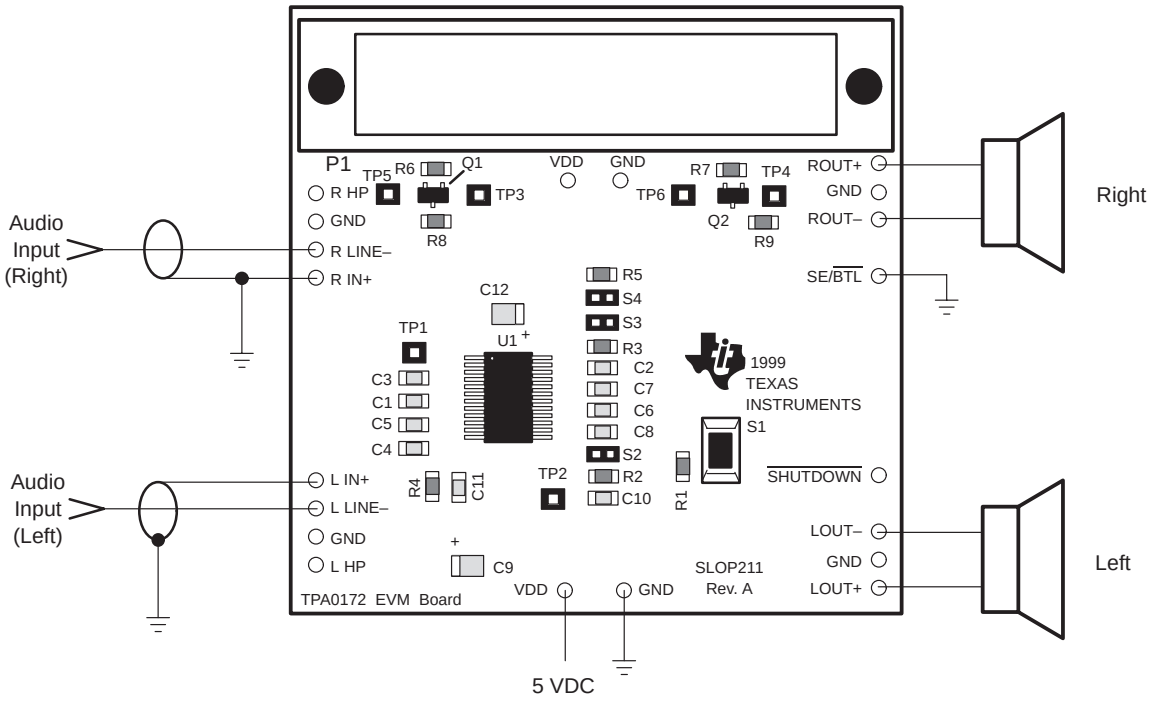
2.4 Stand-Alone Connection Diagram

The power supply range is 4.5 V to 5.5 V and isolated RO/MO+ and LO/MO– lines for BTL operation are required.

Note that the source of any shutdown signal applied to the EVM $\overline{\text{SHUTDOWN}}$ pin must be able to sink the current flowing through the pullup resistor on the module (100 kΩ) when the pin is held low.

Figure 2–4 shows a TPA0172 EVM connected for stereo BTL operation.

Figure 2–4. TPA0172 EVM Connected for Stereo BTL Output



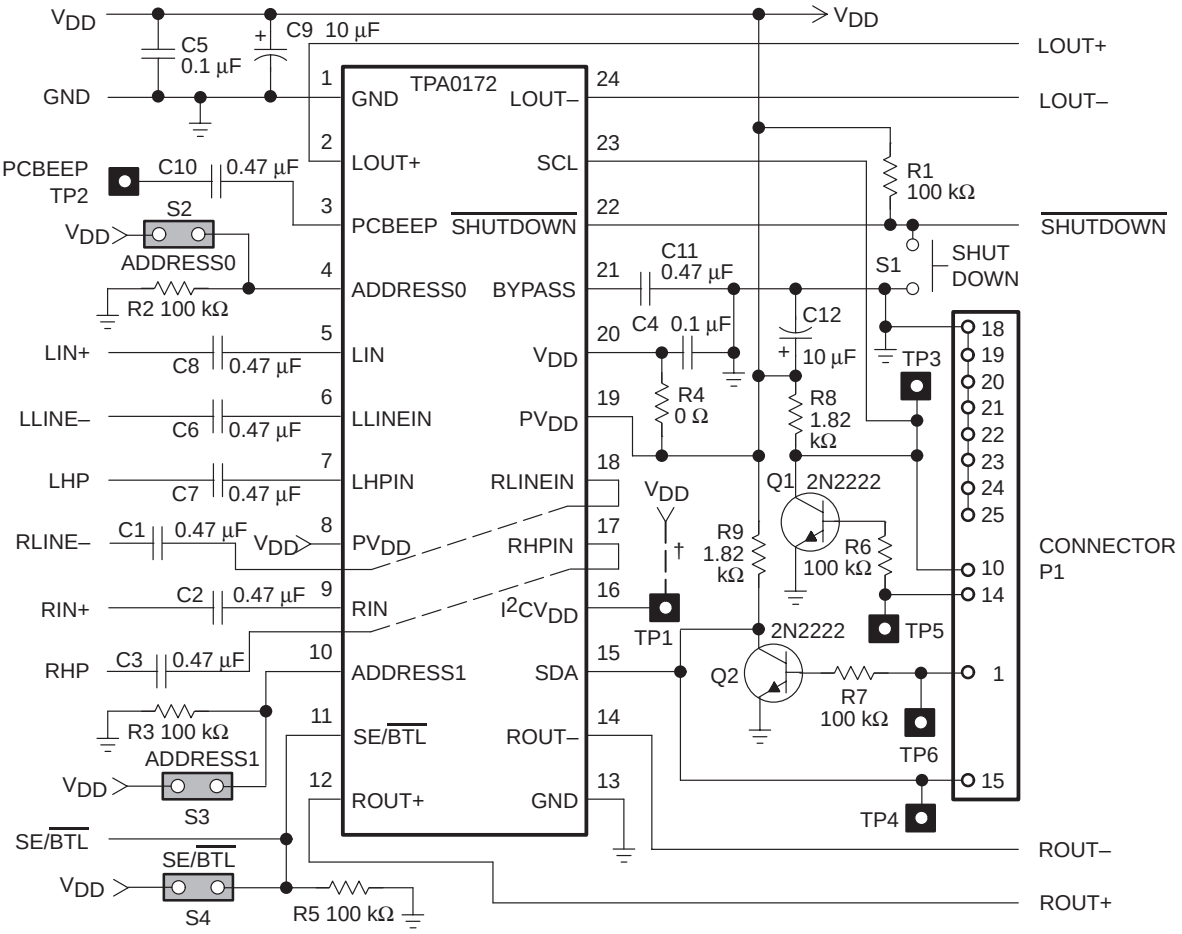
2.5 Reference

This section includes the TPA0172 EVM schematic, the EVM parts list, a discussion of the I²C interface, and the module PCB layers.

2.5.1 EVM Schematic

Figure 2–5 shows the TPA0172 EVM schematic.

Figure 2–5. TPA0172 EVM Schematic Diagram



† I^2CV_{DD} is connected to V_{DD} via a blue wire on the evaluation module. To use a different voltage for the I^2C interface, the wire must be disconnected and the I^2C power supply connected to TP1.

†

2.5.2 EVM Parts List

Table 2–6 is the TPA0172 EVM parts list.

Table 2–6. TPA0172 EVM Parts List

Ref.	Description	Size	EVM Qty.	Manufacturer/ Part Number	Vendor Number
C4, C5	Capacitor, 0.1 μF @ 25 V, 10%, nonpolarized	0805	2	Murata GRM40-X7R104K25	Arrow GRM40-X7R104K25
C1 – C3, C6 – C8, C10, C11	Capacitor, 0.47 μF @ 16 V +80%/–20%, nonpolarized	0805	8	Murata GRM40-Y5V474Z16	Arrow GRM40-Y5V474Z16
C9, C12	Capacitor, 10 μF @ 6.3 V	A	2	Panasonic ECS–TOJY106R	Digi-Key PCS1106CT–ND
R1 – R3, R5 – R7	Resistor, 100 kΩ, 1/10 W, 5%	0805	6	Panasonic ERJ-6GEYJ104V	Digi-Key P100KACT-ND
R8, R9	Resistor, 1.82 kΩ, 1/10 W, 1%	0805	2	Panasonic ERJ-6ENF1821V	Digi-Key P1.82KCTR-ND
R4	Resistor, 0 Ω, 1/10 W, 5%	0805	1	Phycomp 9C08052A0R00JLHFT	Digi–Key 311–0.0ATR–ND
S1	Switch, momentary	SMD	1	Panasonic P8050SCT–ND	Digi-Key P8050SCT-ND
TP1 – TP6	Test points, red		6	Farnell 240–345	
S2 – S4	Headers, 2 position	2 mm	3	Norcomp	Digi-Key 2163S–02–ND
P1	D-SUB connector, 25-pin, male, PCB mount		1	Norcomp 172–025–111–001	Digi-Key 525M–ND
Q1, Q2	Transistor, 2N2222	SOT–23	2	Rohm SST2222AT	Mouser 592–SST2222A
U1	IC, TPA0172 2-W, 2–channel audio amplifier	TSSOP-24	1	TI TPA0172PWP	

2.5.3 I²C Interface Information

The 8-bit I²C address of the TPA0172 is 11011a1a0(r/w). Bits 2 and 1, designated as a1 and a0, are set by the ADDRESS1 and ADDRESS0 pins, respectively. Bit 0, designated as (r/w), is the read/write bit where a 0 designates the write operation and a 1 designates the read operation.

The TPA0172 has six 8-bit registers with power-up/reset values and bit assignments as shown in Table 2–7.

Table 2–7. TPA0172 I²C Register Definitions

REGISTER NAME	POWER-UP/RESET VALUE (b7b6b5...b0)	BIT ASSIGNMENT
Right gain register 1 (BTL gain register)	0011 1111	0–5: Gain level
		6: Mute
		7: Mute
Left gain register 1 (BTL gain register)	0011 1111	0–5: Gain level
		6: Mute
		7: Mute
Right gain register 2 (SE gain register)	0011 1111	0–5: Gain level
		6: Mute
		7: Mute
Left gain register 2 (SE gain register)	0011 1111	0–5: Gain level
		6: Mute
		7: Mute
Mask register	1111 1111	0: Disable internal SHUTDOWN control
		1: Disable internal SE/BTL control
		2: Disable internal PCB enable control
		3–6: Unused
		7: Powering up indicator (read only)
Control register	0000 0000	0: SHUTDOWN
		1: HP/$\overline{\text{LINE}}$
		2: Reserved
		3: Mute
		4: Reserved
		5: SE/$\overline{\text{BTL}}$
		6: Gain register select
		7:PCBEEP

Data must be written to and read from these registers sequentially, in the order shown in the above table. This allows for a much shorter data stream, since the address for each register does not have to be sent/received and acknowledged before data can be written to or read from each register. For example, a typical write operation could be as follows:

1) 11011000 — Address of TPA0172 with write bit set
2) Acknowledge sent back by the TPA0172
3) 00000011 — Right gain register 1 set to 16.25 dB
4) Acknowledge sent back by the TPA0172
5) 00000011 — Left gain register 1 set to 16.25 dB
6) Acknowledge sent back by the TPA0172
7) 00000011 — Right gain register 2 set to 16.25 dB
8) Acknowledge sent back by the TPA0172
9) 00000011 — Left gain register 2 set to 16.25 dB
10) Acknowledge sent back by the TPA0172
11) 00000000 — Mask register — enable internal SHUTDOWN (bit 2), SE/$\overline{\text{BTL}}$ (bit 1), and PCB ENABLE (bit 0)
12) Acknowledge sent back by the TPA0172
13) 00001000 — Control register — disable PCBEEP input (bit 7), gain register 1 selected (bit 6), BTL mode (bit 5), reserved (bit 4), mute disabled (bit 3), reserved (bit 2), LINE inputs selected (bit 1), SHUTDOWN low for normal operation (bit 0)
14) Acknowledge sent back by the TPA0172

Each time the TPA0172 receives a write instruction from the I2C bus, all six registers must be sent an 8-bit number. Conversely, each time the TPA0172 receives a read instruction, the device sends the values stored in all six registers, in sequential order, to the I^2C bus starting with the gain right register 1 and ending with the control register.

2.5.3.1 ADDRESS1 and ADDRESS0 Operation

The ADDRESS1 and ADDRESS0 pins allow the specific I^2C address of the TPA0172 to be set, allowing up to four amplifiers to be controlled through the same I^2C bus. The 8-bit I^2C address of the TPA0172 is 11011a1a0(r/w), with bit 2 (a1) set by ADDRESS1, bit 1 (a0) set by ADDRESS0, and bit 0 (r/w) as the read/write bit. For example, pulling ADDRESS1 high and ADDRESS0 low would give an address of 1101110(r/w). Note that the high and low values are relative to V_{DD}, not I^2CV_{DD}. As a result, the trip point is approximately $V_{DD}/2$.

2.5.3.2 Gain Register Operation

The gain of the TPA0172 ranges from +20 dB to –60 dB in 64 1.25 dB steps. At power up, both the right and left channels are set at –60dB. The truth table shown in Table 2–8 gives examples of valid values that may be read from or written to the four gain setting registers. Note that the amplifier is muted if either bit 7 or bit 6 is set. Furthermore, to avoid any unwanted clicks or pops, the gain settings should not be changed until the amplifier has completed the power-up sequence, which can be determined by monitoring bit 7 of the mask register. When the bit goes to 0, the power-up sequence is complete

Table 2–8. TPA0172 Gain Settings Truth Table

GAIN (dB)	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
20	0	0	0	0	0	0	0	0
18.75	0	0	0	0	0	0	0	1
17.5	0	0	0	0	0	0	1	0
16.25	0	0	0	0	0	0	1	1
...	...	...	...	...	...	...	...	...
–57.5	0	0	1	1	1	1	0	1
–58.75	0	0	1	1	1	1	1	0
–60	0	0	1	1	1	1	1	1
–85 (mute)	1	1	X	X	X	X	X	X

2.5.3.3 Mask Register Operation

The mask register allows the user to select whether SHUTDOWN, SE/BTL, and PCBEEP are to be controlled by the external pins or by the internal control register. Since PCBEEP does not have an external control pin available, writing a 1 to this bit will disable all internal register control and place the PCBEEP in auto-detect mode. When a bit is set, the corresponding internal control register bit is masked or ignored, and the external pin controls the operating mode. Conversely, when a bit is set to 0, the corresponding external pin is disabled and the internal control register bit determines the operating mode. For example, writing XXXXX110 to the register allows a PCBEEP input to be automatically detected and the external pin to control SE/BTL, while allowing the control register to control SHUTDOWN.

The MSB of the mask register is read only. It is set when the TPA0172 is executing its power-up sequence and is set to 0 upon completion of the sequence and during normal operation. To avoid any unwanted clicks or pops, the gain registers should not be changed while this bit is set.

2.5.3.4 Control Register Operation

Each bit of the control register allows the user to control the operating mode of the TPA0172, as shown in Table 2–9.

Table 2–9. TPA0172 Control Register Operation

BIT	FUNCTION	VALUE	RESULT
0	SHUTDOWN	0	Normal operation
		1	Shutdown mode
1	HP/$\overline{\text{LINE}}$	0	Line inputs selected
		1	Headphone inputs selected
2	Reserved	0	Reserved
3	Mute	0	Normal operation
		1	Mute mode
4	Reserved	1	Reserved
5	SE/$\overline{\text{BTL}}$	0	BTL mode
		1	SE mode
6	Gain register select	0	Use gain register 1
		1	Use gain register 2
7	PCB ENABLE	0	Auto-detect PCBEEP
		1	PCBEEP always on

Bit 0 operates in the same manner as the external $\overline{\text{SHUTDOWN}}$ pin, only the logic is reversed (i.e., the device is active when the internal bit is low and is in shutdown when the internal bit is high).

Bit 1 allows the user to select the input source. If bit 1 of the mask register is set, however, the HP/$\overline{\text{LINE}}$ function is tied to the external SE/$\overline{\text{BTL}}$ pin.

Bit 2 This bit is reserved for future functionality. Always set this bit to 0.

Bit 3 performs the same mute function as setting either bit 6 or 7 in the gain registers.

Bit 4 This bit is reserved for future functionality. Always set this bit to 1.

Bit 5 operates in the same manner as the external SE/$\overline{\text{BTL}}$ pin.

Bit 6 allows the user to select which gain registers will determine the gain settings for each channel. For example, the amplifier may be configured to operate in SE mode with the gain settings taken from either register 1 or register 2. This function is tied to the SE/$\overline{\text{BTL}}$ pin if bit 1 of the mask register is set, which results in gain register 1 controlling the gain in SE mode and gain register 2 controlling the gain in BTL mode. It is important to remember that regardless of which gain register is selected, when the amplifier is in the single–ended mode of operation the gain will be 6 dB less than the setting stored in the register.

Bit 7 allows the user to either autodetect a signal at the PCBEEP input or manually override that input to be always on.

2.5.4 Module PCB Layers

The following illustrations depict the TPA0172 EVM PCB layers and silkscreen. These drawings are not to scale. Gerber plots can be obtained from any TI Sales Office.

Figure 2–6. TPA0172 EVM PCB

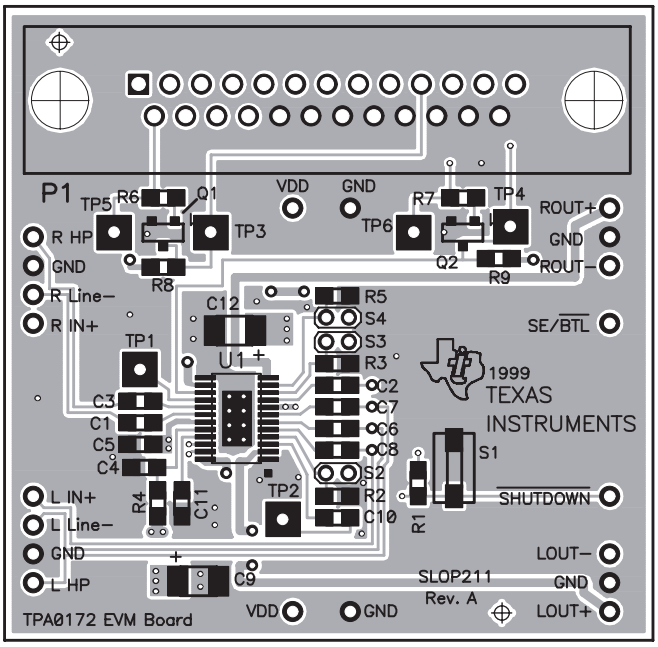


Figure 2–7. TPA0172 EVM Silkscreen

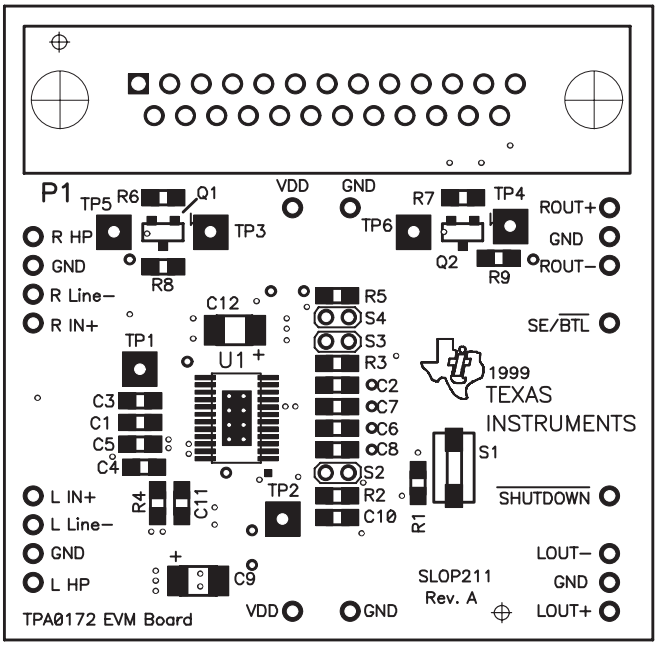


Figure 2–8. TPA0172 EVM Bottom Layer