User's Guide

TPS54350 Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide describes the characteristics, operation, and the use of the TPS54350EVM−235 evaluation module. It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram, and bill of materials are included.

WARNING

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments can cause interference with radio communications, in which case, the user at their own expense will be required to take whatever measures may be required to correct this interference.

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Table of Contents

1 Introduction

This chapter contains background information for the TPS54350 with support documentation for the TPS54350EVM-235 evaluation module (SLVP235). This user's guide contains the TPS54350EVM-235 performance specifications, schematic, and bill of material for the TPS54350EVM-235.

1.1 Background

The TPS54350 DC/DC converter is designed to provide up to 3-A output from a nominal 12-V (6-V to 18-V) input voltage source. Table 1-1 provides the rated input voltage and output current range. This evaluation module is designed to demonstrate the small PCB areas that can be achieved when designing with the TPS54350 regulator and does not reflect the high efficiencies that can be achieved when designing with this part. The switching frequency is set at a nominal 500 kHz, allowing the use of a relatively small footprint 10-mH output inductor. The high-side MOSFET is incorporated inside the TPS54350 package along with gate drive circuitry for an external synchronous FET. The low drain-to-source on resistance of the MOSFET allows the TPS54350 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are provided external to the IC, and allow for an adjustable output voltage and a customizable loop response. The TPS54350 is a full-featured device including:

- Programmable undervoltage lockout
- Bidirectional synchronization
- Adjustable switching frequency
- Enable and power good functions

Table 1-1. Input Voltage and Current Summary

EVM	INPUT VOLTAGE RANGE(1)	OUTPUT CURRENT RANGE
TPS54350EVM−235	6 V to 18 V	0 A to 3 A

(1) Operation assured to 4.0 V after initial start-up.

1.2 Performance Specification Summary

A summary of the TPS54350EVM-235 performance specifications is provided in Table 1-2. Specifications are given for an input voltage of 12 V and an output voltage of 3.3 V, unless otherwise specified. The ambient temperature is 250°C for all measurements, unless otherwise noted. The maximum input voltage for the TPS54350 is 4.5 V to 20 V. The EVM operates over this range but is designed and tested for 6-V to 18-V input range (12-V nominal).

Table 1-2. TPS54350EVM-235 Performance Specification Summary

SPECIFICATION		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage range			8.0	12.0	18	V
Output voltage set point				3.3		V
Output current range		V_I = 3 V to 5.5 V	0		3	A
Line regulation		I_O = 0–3 A, V_I = 6 V to 18 V		±1%		
Load regulation		V_I = 12 V, I_O = 0 A to 3 A		±0.05%		
Load transient	Voltage change	I_O = 0.75 A to 2.25 A		–10		mV_{PK}
	Recovery time			60		µs
	Voltage range	I_O = 2.25 A to 0.75 A		11		mV_{PK}
	Recovery time			60		µs
Loop bandwidth		V_I = 6 V		28		kHz
Phase margin		V_I = 6 V		70		°
Loop bandwidth		V_I = 18 V		32		kHz
Phase margin		V_I = 18 V		60		°
Input ripple voltage				400		mV_{PP}
Output ripple voltage				40		mV_{PP}
Output rise time				2.8		ms
Operating frequency				500		kHz

Table 1-2. TPS54350EVM-235 Performance Specification Summary (continued)

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Maximum efficiency	V_I = 6.0 V, V_O = 3.3 V, I_O = 1.0 A		87%		

1.3 Modifications

The TPS54350EVM−235 is designed to demonstrate the small size that can be attained when designing with the TPS54350, so many of the features, which allow for extensive modifications, have been omitted from this EVM.

1.3.1 Output Voltage Setpoint

Changing the value of R2 can change the output voltage in the range of 0.9 V to 5 V. The value of R2 for a specific output voltage can be calculated by using Equation 1. Table 1-3 list the values for R2 for some common output voltages.

Table 1-3. Output Voltage Programming

OUTPUT VOLTAGE (V)	R_2 VALUE (Q)
1.2	2.87 k
1.5	1.47 k
1.8	976
2.5	549
3.3	374
5.0	221

$$R_2 = 1\ k\Omega \times \frac{0.891\ V}{V_O - 0.891\ V} \quad (1)$$

The minimum output voltage is limited by the minimum controllable on time of the device, 125 ns, and is dependent upon the duty cycle and operating frequency. The approximate minimum output voltage can be calculated using Equation 2:

$$V_{O(min)} = 125\ \text{nsec} \times f\text{s} \times V_{I(max)} \quad (2)$$

1.3.2 Switching Frequency

The switching frequency can be trimmed to any value between 250 kHz and 700 kHz by changing the value of R4. The switching frequency can also be set to pre-programmed values of 250 kHz by shorting the RT pin to AGND, or 500 kHz by floating the RT pin. Decreasing the switching frequency results in increased output ripple unless the value of L1 is increased.

1.3.3 Input Filter

An on-board electrolytic input capacitor can be added at C1.

1.3.4 UVLO Programming

The TPS54350 is provided with an internal voltage divider from VIN to AGND. These start and stop thresholds are given in Table 1-4.

Table 1-4. Internal UVLO Setting

	START VOLTAGE THRESHOLD	STOP VOLTAGE THRESHOLD
VIN	4.4 V	3.7 V
UVLO	1.18 V	1.09 V

To set a different set of thresholds, R6 and R7 can be selected using Equation 3 and Equation 4.

$$R6 = \frac{V_{I(start)} \times R7}{UVLO(start)} - R7 \quad (3)$$

$$R6 = \frac{V_{I(stop)} \times R7}{UVLO(stop)} - R7 \quad (4)$$

1.3.5 Synchronization

The SYNC pin can be configured as an input or as an output, depending on the configuration of the RT pin. If the RT pin is open or tied to AGND, the SYNC pin functions as an output. When operating as an output, the falling edge of the signal is one half of the switching cycle and approximately 180° out of phase with the rising edge of the PH pins. Thus, two TPS54350 devices operating in a system can share an input capacitor and draw ripple current at twice the frequency of a single unit.

If the RT pin is programmed with a resistor to AGND, the SYNC pin functions as an input. When operating as an input, the SYNC pin is a falling-edge triggered signal, and the resistor at the RT pin should be set to provide a frequency equal to 90 percent of the SYNC input frequency.

1.3.6 Power Good

An internal circuit monitors the VSENSE input voltage to verify that it is within a guard band around the reference voltage. If these voltages are close to each other in value, and no other fault signals are present, the PWRGD pin presents a high impedance. A low on the PWRGD pin indicates a fault. The PWRGD pin has been designed to provide a weak pulldown and indicates a fault even when the device is unpowered. If the TPS54350 has power and has any fault flag set, the TPS54350 indicates the power is not good by driving the PWRGD pin low. The following events, alone or in combination, indicates power not good:

- VSENSE pin out of bounds
- Overcurrent
- Thermal shutdown
- UVLO undervoltage
- Input voltage not present (weak pulldown)
- Slow starting
- VBIAS voltage is low

The evaluation module provides an external pullup resistor of 10 kW (R8), a test point TP1 that can be tied to an external 3.3-V or 5-V source, and a test point TP2 to monitor the power-good signal.

1.3.7 Synchronous Low-Side FET

The TPS54350EVM-235 is provisioned with a external low-side FET for operation as a synchronous buck regulator. If desired, an external catch diode can be used in place of the FET. The pad for the diode is located on the back side of the PCB. Verify that the inductor is properly sized for operation without the low-side FET. The minimum value for the inductor when operating in this mode is given by Equation 5.

$$L(\min) = \frac{V_O\left(1 - \frac{V_O}{V_{I(max)}}\right)}{fs \times 0.6} \quad (5)$$

1.3.8 Optional Output Filtering

Optional pads are included on the EVM for additional output filter capacitors. One D4 location (C12) and one 0805 location (C5) are provided.

2 Test Setup and Results

This chapter describes how to properly connect, set up, and use the TPS54350EVM−235 evaluation module. The section also includes test results typical for the TPS54350EVM−235 and covers the following:

- Efficiency
- Output voltage regulation
- Load transients
- Loop response
- Output ripple
- Input ripple
- Start-up

2.1 Input/Output Connections

The TPS54350EVM−235 has the following two input/output connectors: VI(J1) and VO (J3). A diagram showing the connection points is shown in Figure 2-1. A power supply capable of supplying 5 A should be connected to J1 through a pair of 20 AWG wires. The load should be connected to J2 through a pair of 20 AWG wires. The maximum load current capability should be 3 A. Wire lengths should be minimized to reduce losses in the wires. Test point TP9 provides a place to easily connect an oscilloscope voltage probe to monitor the output voltage. The TPS54350 is intended to be used as a point of load regulator. In typical applications, it is usually located close to the input voltage source. When using the TPS54350EVM−235 with an external power supply as the source for VI, an additional bulk capacitor can be required, depending on the output impedance of the source and length of the hook-up wires. The test results presented are obtained using a 47-mF, 25-V additional input capacitor. Alternately, C1 can be populated with an input filter capacitor.

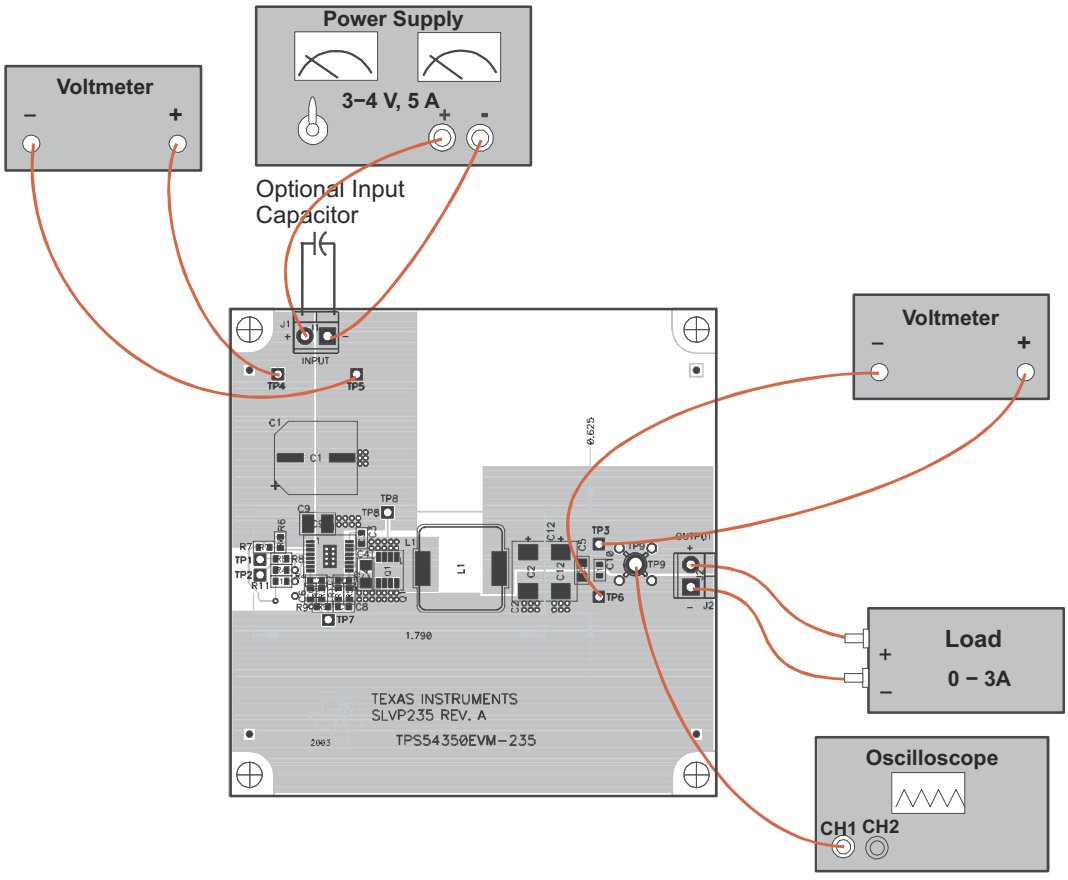

Figure 2-1. Connection Diagram

2.2 Efficiency

The TPS54350EVM−235 efficiency peaks at load current of approximately 1 A and V_I of 6 V, and then decreases as the load current increases towards full load. For higher input voltages, quiescent losses are greater and the efficiency peaks under full load conditions. It is important to consider that this design is optimized for small size and flexibility and does not reflect the high efficiencies that are possible for specific applications using the TPS54350. Figure 2-2 shows the efficiency for the TPS54350 at an ambient temperature of 250°C. The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs. The efficiency is slightly lower at 500 kHz than at lower switching frequencies due to the gate and switching losses in the MOSFETs.

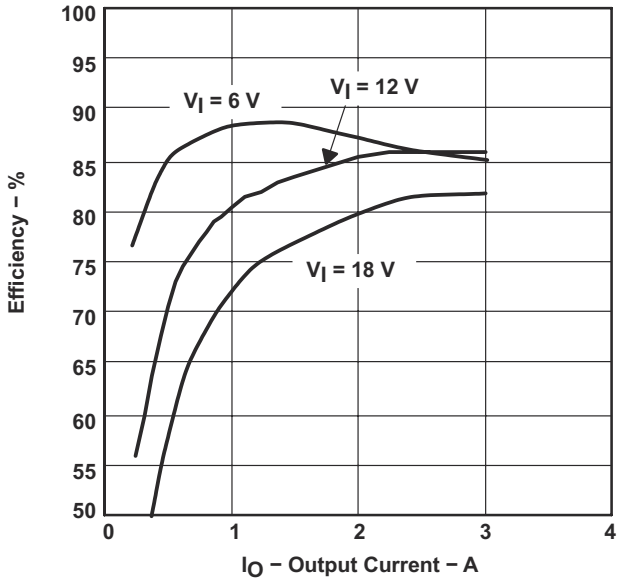

Figure 2-2. Measured Efficiency

2.3 Power Dissipation

The low junction-to-case thermal resistance of the PWP package, along with a good board layout, allows the TPS54350EVM−235 EVMs to output full-rated load current while maintaining safe junction temperatures. With a 12-V input source and a load approaching the current limit of 4.2 A, the junction temperature is approximately 47°C. The total circuit losses at 25°C are shown in Figure 2-3. Power dissipation is shown for input voltages of 6 V, 12 V, and 18 V. For additional information on the dissipation ratings of the devices, see the individual product data sheets.

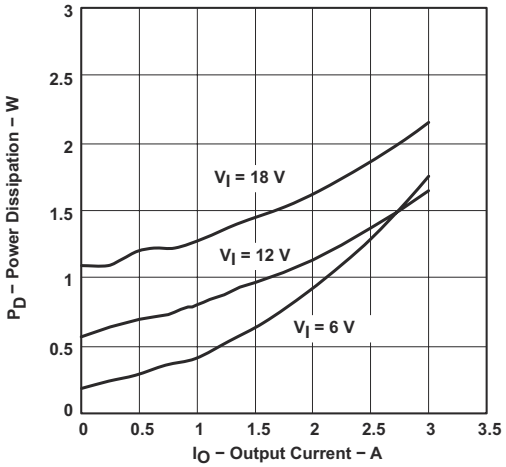

Figure 2-3. Measured Circuit Losses

2.4 Output Voltage Regulation

The output voltage load regulation of the TPS54350EVM−235 is shown in Figure 2-4, while the output voltage line regulation is shown in Figure 2-5. Measurements are given for an ambient temperature of 25°C.

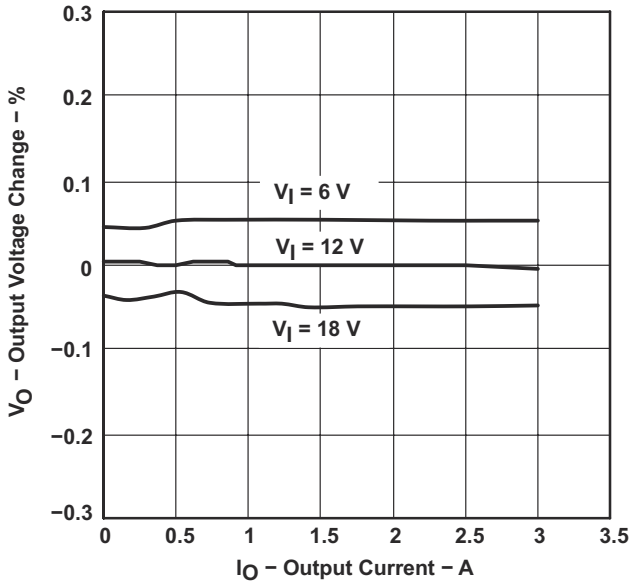

Figure 2-4. Load Regulation

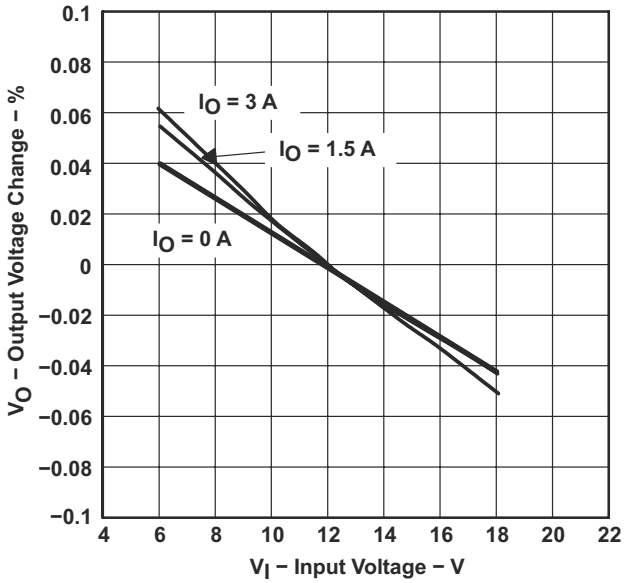

Figure 2-5. Line Regulation

2.5 Load Transients

The TPS54350EVM−235 response to load transients is shown in Figure 2-6. The current step is from 25% to 75% of maximum rated load. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

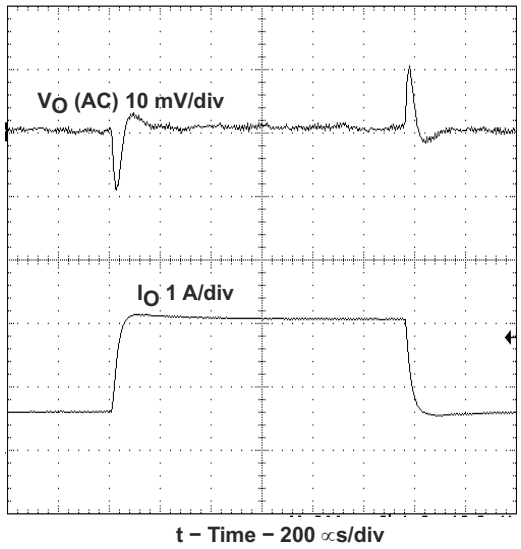

Figure 2-6. Load Transient Response, TPS54350

2.6 Loop Characteristic

The TPS54350EVM−235 loop response characteristics are shown in Figure 2-7 and Figure 2-8. Gain and phase plots are shown for each device at minimum and maximum operating voltage.

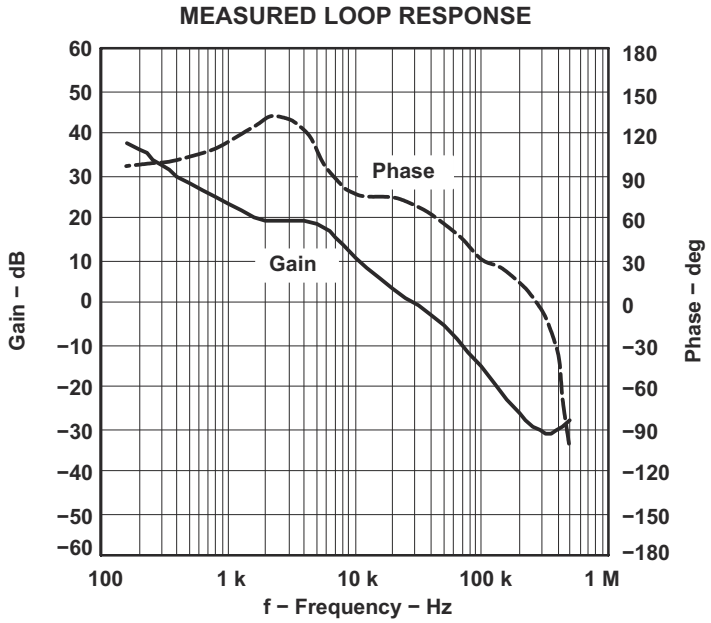

Figure 2-7. Measured Loop Response, TPS54350, V_I = 6 V

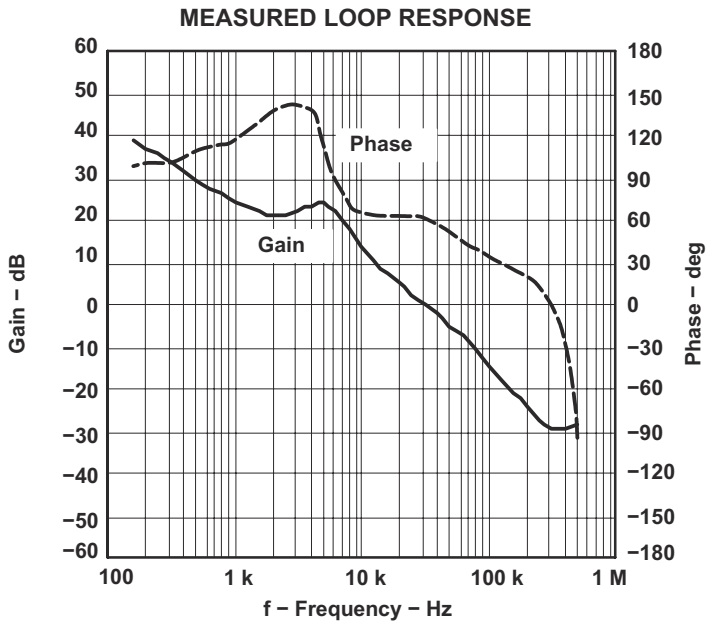

Figure 2-8. Measured Loop Response, TPS54350, V_I = 18 V

2.7 Output Voltage Ripple

The TPS54350EVM−235 output voltage ripple is shown in Figure 2-9. The input voltage is 3.3 V for the TPS54350. Output current is the rated full load of 3 A. Voltage is measured directly across output capacitors.

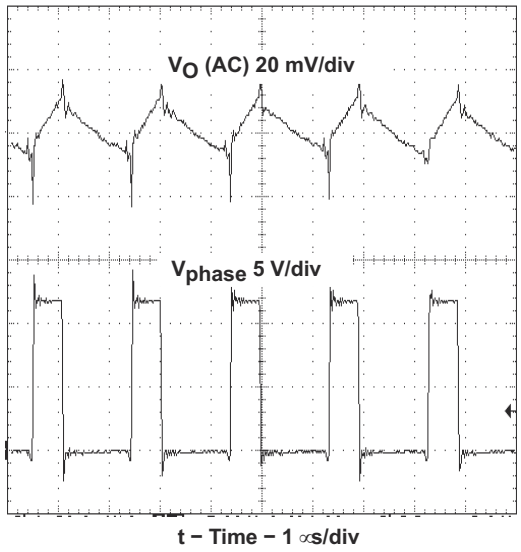

Figure 2-9. Measured Output Voltage Ripple, TPS54350

2.8 Input Voltage Ripple

The TPS54350EVM−235 output voltage ripple is shown in Figure 2-10. The input voltage is 3.3 V for the TPS54350. Output current for each device is rated full load of 3 A.

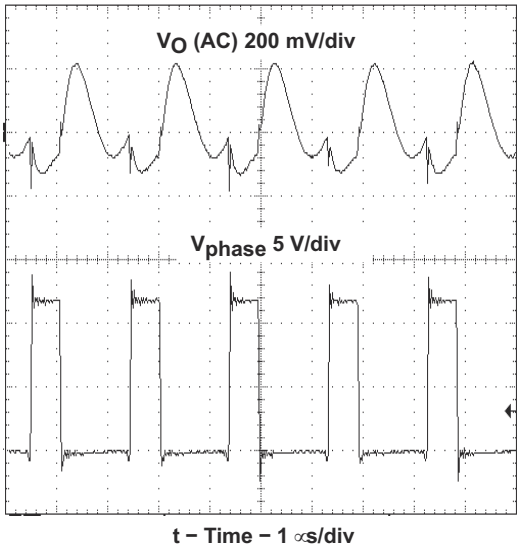

Figure 2-10. Input Voltage Ripple, TPS54350

2.9 Gate Drive

The TPS54350 provides the gate drive signal for a synchronous low-side FET. This gate drive signal and its relationship to the PHASE signal is shown in Figure 2-11.

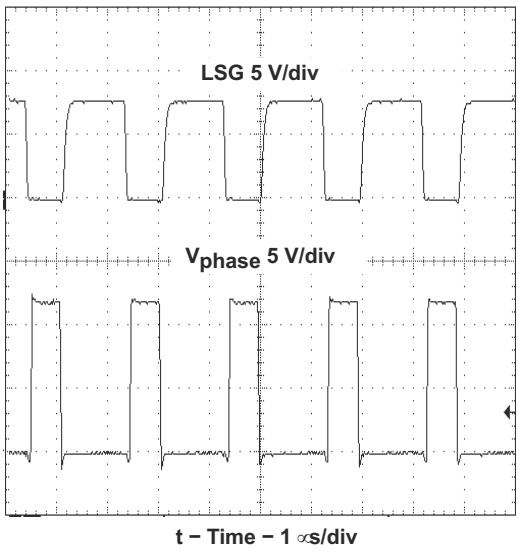

Figure 2-11. Gate Drive Signal, TPS54350

2.10 Powering Up and Down

The start-up voltage waveform of the TPS54350EVM−235 is shown in Figure 2-12. The waveform shows the nominal 12-V input voltage in Ch. 1, the 3.3-V output ramping up in Ch. 2, and the PWRGD signal in Ch. 3. Note that the PWRGD signal is pulled up externally to 3.3 V.

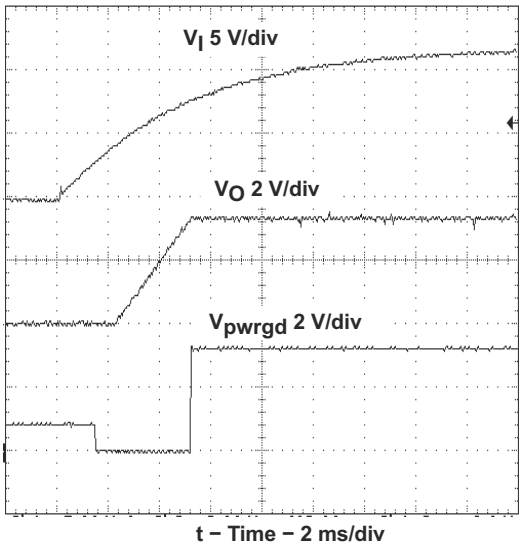

Figure 2-12. Powering Up

The corresponding power-down waveform is shown in Figure 2-13. The channel assignments are the same as in the power-up waveform in Figure 2-12.

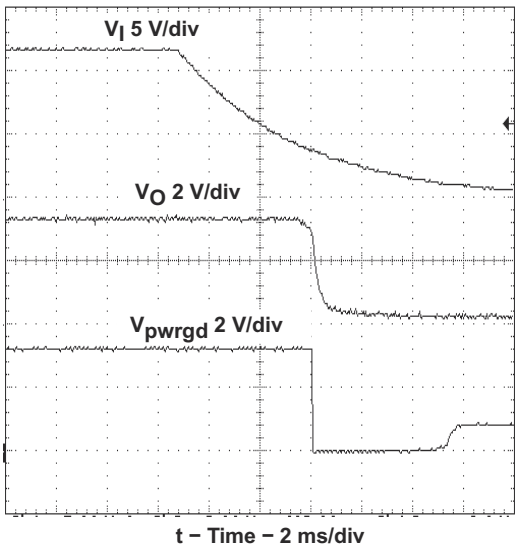

Figure 2-13. Powering Down

3 Board Layout

This section provides a description of the TPS54350EVM−235 board layout and layer illustrations.

3.1 Layout

Theboard layout for the TPS54350EVM−235 is shown in Figure 3−1 through Figure 3−4. The topside layer of the TPS54350EVM−235 is laid out in a manner typical of a user application that is optimized for small size. The top and bottom layers are 1.5 oz. copper.

The top layer contains the main power traces for VI, VO, and Vphase. Also, on thetop layer are connections for the remaining pins of the TPS54350 and a large area filled with ground. The bottom layer consists of a ground plane along with aVphase area and the Vsense trace. The bottom layer also has pads for placing snubber components (R10 and C11) and an optional catch diode (D1). The top and bottom ground traces are connected with multiple vias placed around the board including 8 directly under the TPS54350 device to provide a thermal path from the PowerPADä landto ground.

The input decoupling capacitor (C9), bias decoupling capacitor (C4), andbootstrap capacitor (C3) are all located as close to the IC as possible. In addition, the compensation components are also kept close to the IC. The compensation circuit ties to the output voltage at the point of regulation, at the positive output connection.

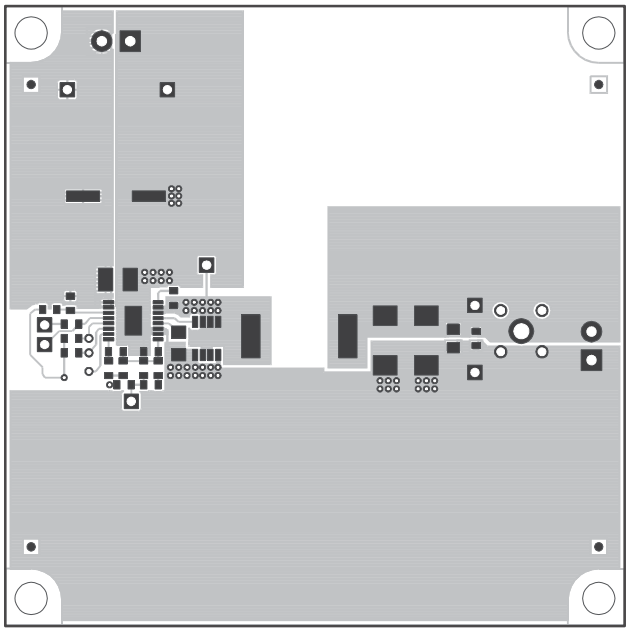

Figure 3-1. Top Side Layout

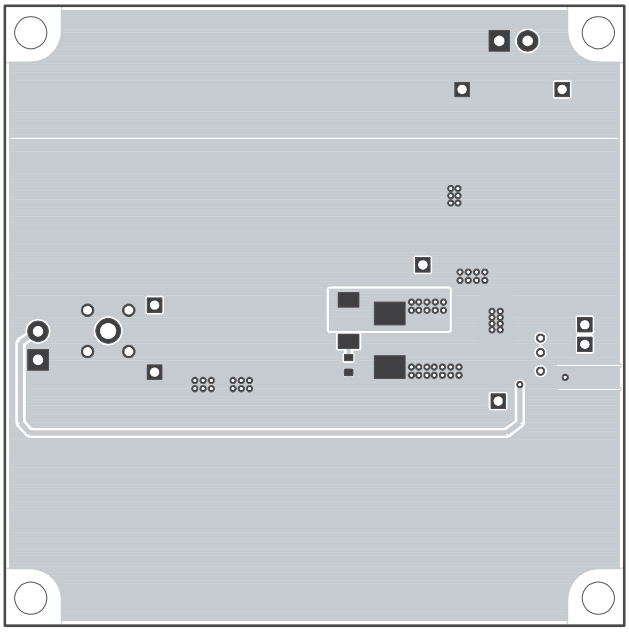

Figure 3-2. Bottom Side Layout

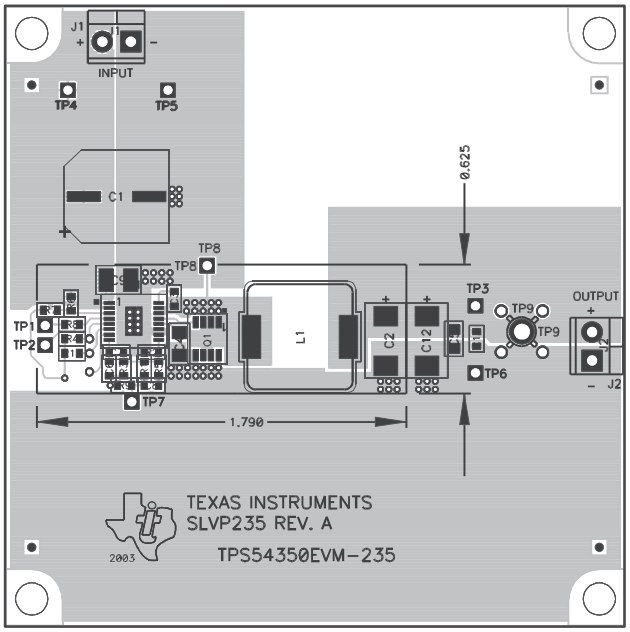

Figure 3-3. Top Side Assmebly

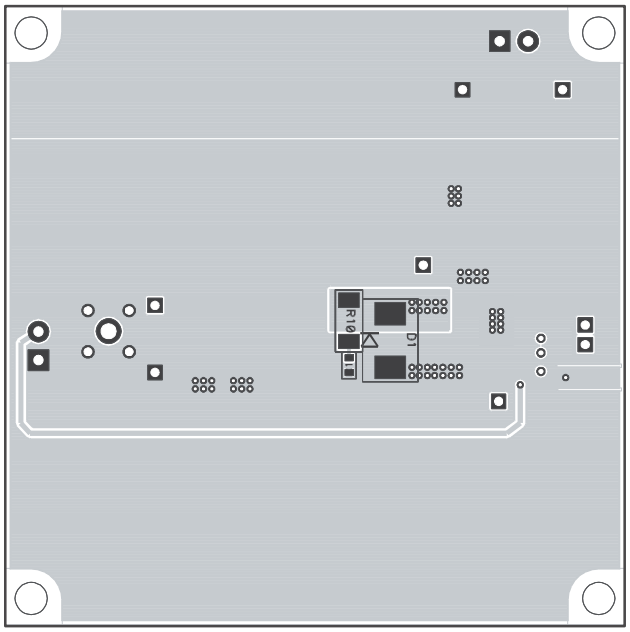

Figure 3-4. Bottom Side Assmebly

4 Schematic and Bill of Materials

The TPS54350EVM−235 schematic and bill of materials are presented in this section.

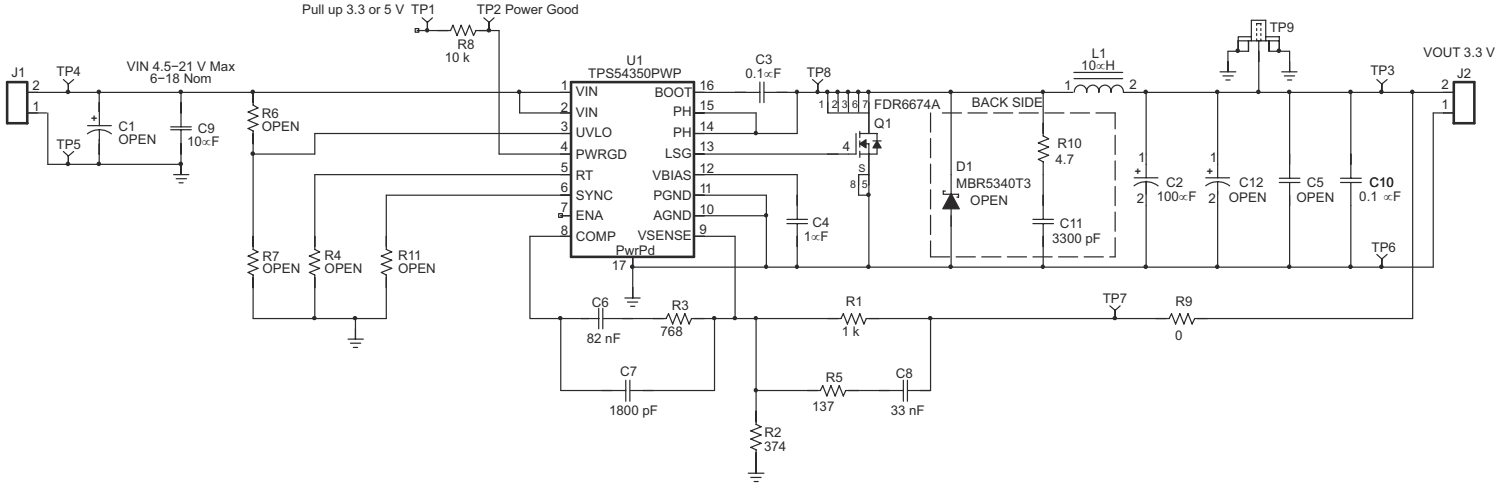

Figure 4-1. TPS54350EVM-235 Schematic

4.1 Bill of Materials

The bill of materials for the TPS54350EVM—235 is provided in Table 4-1.

Table 4-1. Bill of Materials

Count	RefDes	Description	Size	MFR	PartNumber
—	C1	Capacitor,aluminum, 100 mF, 35 V, 20%, FC Series	0.335x 0.374	Panasonic	EEVFC1V101P
1	C11	Capacitor,ceramic, 3300 pF, 50 V, X7R, 10%	603	std	std
—	C12	Capacitor, aluminum, xxx mF, × V, 20% (UE Series)	7343	std	std
—	C5	Capacitor,ceramic, xxx mF,vv V, [temp], [tol]	805	std	std
1	C2	Capacitor, POSCAP, 100 mF, 6.3 V, 45 mW, 20%	7343(D)	Sanyo	6TPC100M
2	C3,C10	Capacitor,ceramic, 0.1 mF,16 V, X7R, 10%	603	std	std
1	C4	Capacitor,ceramic, 1.0 mF,16 V, X7R, 10%	1206	std	std
1	C6	Capacitor,ceramic, 82 nF, 16 V, X7R, 10%	603	std	std
1	C7	Capacitor,ceramic, 1800 pF, 50 V, X7R, 10%	603	std	std
1	C8	Capacitor,ceramic, 33 nF, 50 V, X7R, 10%	603	std	std
1	C9	Capacitor,ceramic, 10 mF,25 V, X5R, 20%	1210	Taiyo Yuden	TMK325BJ106MN
—	D1	Diode,schottky, 3 A, 40 V	SMC	Motorola	MBRS340T3
2	J1,J2	Terminal block, 2 pin, 6 A, 3.5 mm	75525	OST	ED1514
1	L1	Inductor,SMT, 10 mH, 8 A, 20 mW	0.51 × 0.51	Vishay	IHLP—5050CZ
1	Q1	Transistor,MOSFET, Nch, 11.5 A, 30 V, 9.5 mW	0.160 × 0.130	Fairchild	FDR6674A
1	R1	Resistor,chip, 1.00 kW,1/16 W, 1%	603	std	std
1	R10	Resistor,chip, 4.7 W,1/2 W, 5%	2010	std	std
1	R2	Resistor,chip, 374 W,1/16 W, 1%	603	std	std
1	R3	Resistor,chip, 768 W,1/16 W, 1%	603	std	std
—	R4, R6,R7, R11	Resistor,chip, xx W,1/16 W, 1%	603	std	std
1	R5	Resistor,chip, 137 W,1/16 W, 1%	603	std	std
1	R8	Resistor,chip, 10.0 kW,1/16 W, 1%	603	std	std
1	R9	Resistor,chip, 0 W,1/16 W, 1%	603	std	std
4	TP1, TP3, TP4,TP8	Testpoint, red, 1 mm	0.038	Farnell	240–345
4	TP2, TP5, TP6,TP7	Testpoint, black, 1 mm	0.038	Farnell	240–333
1	TP9	Adaptor,3.5 mm probe clip (or 131–5031–00)	0.2	Tektronix	131–4244–00
1	U1	IC,dc/dc converter	PWP16	TI	TPS54350PWP
1	——	PCB,3 inch × 3 inch × 0.062 inch		Any	SLVP235

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2004) to Revision B (October 2021) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 2
- Updated the user's guide title..... 2

- Edited user's guide for clarity.....2

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