Si47xx Programming Guide

1. Introduction

This document provides an overview of the programming requirements for the Si4704/05/06/07/1x/2x/3x/4x/84/85 FM transmitter/AM/FM/SW/LW/WB receiver. The hardware control interface and software commands are detailed along with several examples of the required steps to configure the device for various modes of operation.

2. Overview

This family of products is programmed using commands and responses. To perform an action, the system controller writes a command byte and associated arguments, causing the device to execute the given command. The device will, in turn, provide a response depending on the type of command that was sent. Section "4. Commands and Responses" on page 6 and Section "5. Commands and Properties" on page 7 describe the procedures for using commands and responses and provide complete lists of commands, properties, and responses.

The device has a slave control interface that allows the system controller to send commands to and receive responses from the device using one of three serial protocols (or bus modes): 2-wire mode (I^2C and SMBUS compatible), 3-wire mode, or SPI mode.

Section "6. Control Interface" on page 223 describes the control interface in detail.

Section "7. Powerup" on page 231 describes options for the sequencing of VDD and VIO power supplies, selection of the desired bus mode, provision of the reference clock, RCLK, and sending of the POWER_UP command.

Section "8. Powerdown" on page 238 describes sending the POWER_DOWN command and removing VDD and VIO power supplies as necessary.

Section "9. Digital Audio Interface" on page 239 describes the digital audio format supported and how to operate the device in digital mode.

Section "10. Timing" on page 242 describes the CTS (Clear to Send) timing indicating when the command has been accepted and in most cases completed execution, and the STC (Seek/Tune Complete) timing indicating when the Seek/Tune commands have completed execution.

Section "11. FM Transmitter" on page 248 describes the audio dynamic range control, limiter, pre-emphasis, recommendations for maximizing audio volume for the FM transmitter.

Section "12. Programming Examples" on page 252 provides flowcharts and step-by-step procedures for programming the device.

Table 1. Product Family Function

Part Number	General Description	FM Transmitter	FM Receiver	AM Receiver	SW/LW Receiver	WB Receiver	RDS	High Performance RDS	RPS	SAME	Digital Input	Digital Output	Embedded FM antenna	AEC-Q100 Qualified	Package Size (mm)
Si4700	FM Receiver		✓												4x4
Si4701	FM Receiver with RDS		✓				✓								4x4
Si4702	FM Receiver		✓												3x3
Si4703	FM Receiver with RDS		✓				✓								3x3
Si4704	FM Receiver		✓									[1]	✓		3x3
Si4705	FM Receiver with RDS		✓				✓	[2]				✓	✓		3x3
Si4706[3]	High Performance RDS Receiver		✓				✓	✓				✓	✓		3x3
Si4707[3]	WB Receiver with SAME					✓				✓					3x3
Si4708	FM Receiver		✓												2.5x2.5
Si4709	FM Receiver with RDS		✓				✓								2.5x2.5
Si4710[4]	FM Transmitter	✓									✓		✓		3x3
Si4711	FM Transmitter with RDS	✓					✓				✓		✓		3x3
Si4712[4]	FM Transmitter with RPS	✓							✓		✓		✓		3x3
Si4713	FM Transmitter with RDS & RPS	✓					✓		✓		✓		✓		3x3
Si4720[4]	FM Transceiver	✓	✓						✓		✓		✓		3x3
Si4721	FM Transceiver with RDS	✓	✓				✓		✓		✓	✓	✓		3x3
Si4730	AM/FM Receiver		✓	✓											3x3
Si4731	AM/FM Receiver with RDS		✓	✓			✓	[2]				✓			3x3
Si4732[5]	AM/SW/LW/FM Receiver with RDS		✓	✓	✓		✓	✓				✓			SOIC16
Si4734	AM/SW/LW/FM Receiver		✓	✓	✓										3x3
Si4735	AM/SW/LW/FM Receiver with RDS		✓	✓	✓		✓	[2]				✓			3x3
Si4736	AM/FM/WB Receiver		✓	✓		✓									3x3

Notes:

1. Digital Output is available in Si4704-D60 and later.
2. High Performance RDS is available in Si4705/31/35/85-D50 and later, Si4732.
3. Si4706, Si4707, and Si474x are covered under NDA.
4. There is an errata for the digital audio input for Si4710-B30, Si4712-B30, and Si4720-B20. A patch is available to enable digital audio input for these devices. Please contact Skyworks Solutions to request a patch.
5. Si4732-A10 has the same firmware FMRX component and AM_SW_LW RX component as that of Si4735-D60, so Si4732-A10 is considered as the most recent revision as D60, and the Si4735-D60 related descriptions in Appendix A and Appendix B also apply to Si4732-A10 if not specified.

Table 1. Product Family Function (Continued)

Si4737	AM/FM/WB Receiver with RDS		✓	✓		✓	✓					✓			3x3
Si4738	FM/WB Receiver		✓			✓									3x3
Si4739	FM/WB Receiver with RDS		✓			✓	✓					✓			3x3
Si4740[3]	AM/FM Receiver		✓	✓										✓	4x4
Si4741[3]	AM/FM Receiver with RDS		✓	✓			✓	✓				✓		✓	4x4
Si4742[3]	AM/LW/SW/FM/WB Receiver		✓	✓	✓	✓								✓	4x4
Si4743[3]	AM/LW/SW/FM/WB Receiver with RDS		✓	✓	✓	✓	✓	✓				✓		✓	4x4
Si4744[3]	AM/LW/SW/FM Receiver		✓	✓	✓									✓	4x4
Si4745[3]	AM/LW/SW/FM Receiver with RDS		✓	✓	✓		✓	✓				✓		✓	4x4
Si4749[3]	High-Performance RDS Receiver						✓	✓						✓	4x4
Si4784	FM Receiver		✓									✓			3x3
Si4785	FM Receiver with RDS		✓				✓	2				✓			3x3

Notes:

1. Digital Output is available in Si4704-D60 and later.
2. High Performance RDS is available in Si4705/31/35/85-D50 and later, Si4732.
3. Si4706, Si4707, and Si474x are covered under NDA.
4. There is an errata for the digital audio input for Si4710-B30, Si4712-B30, and Si4720-B20. A patch is available to enable digital audio input for these devices. Please contact Skyworks Solutions to request a patch.
5. Si4732-A10 has the same firmware FMRX component and AM_SW_LW RX component as that of Si4735-D60, so Si4732-A10 is considered as the most recent revision as D60, and the Si4735-D60 related descriptions in Appendix A and Appendix B also apply to Si4732-A10 if not specified.

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3. Terminology

- $\overline{\text{SEN}}$—Serial enable pin, active low; used as device select in 3-wire and SPI operation and address selection in 2-wire operation.
- SDIO—Serial data in/data out pin.
- SCLK—Serial clock pin.
- $\overline{\text{RST}}$ or RSTb—Reset pin, active low
- RCLK—External reference clock
- GPO—General purpose output
- CTS—Clear to send
- STC—Seek/Tune Complete
- NVM—Non-volatile internal device memory
- Device—Refers to the FM Transmitter/AM/FM/SW/LW/WB Receiver
- System Controller—Refers to the system microcontroller
- CMD—Command byte
- COMMANDn—Command register (16-bit) in 3-Wire mode (n = 1 to 4)
- ARGn—Argument byte (n = 1 to 7)
- STATUS—Status byte
- RESPn—Response byte (n = 1 to 15)
- RESPONSEn—Response register (16-bit) in 3-Wire mode (n = 1 to 8)

4. Commands and Responses

Commands control actions, such as power up, power down, or tune to a frequency, and are one byte in size. Arguments are specific to a given command and are used to modify the command. For example, after the TX_TUNE_FREQ command, arguments are required to set the tune frequency. Arguments are one byte in size, and each command may require up to seven arguments. Responses provide the system controller status information and are returned after a command and its associated arguments are issued. All commands return a one byte status indicating interrupt state and clear-to-send the next command. Commands may return up to 15 additional response bytes. A complete list of commands is available in “5. Commands and Properties”.

Table 2 shows an example of tuning to a frequency using the TX_TUNE_FREQ command. This command requires that a command and three arguments be sent and returns one status byte. The table is broken into three columns. The first column lists the action taking place: command (CMD), argument (ARG), status (STATUS), or response (RESP). The second column lists the data byte or bytes in hexadecimal that are being sent or received. An arrow preceding the data indicates data being sent from the device to the system controller. The third column describes the action.

Table 2. Using the TX_TUNE_FREQ Command

Action	Data	Description
CMD	0x30	TX_TUNE_FREQ
ARG1	0x00	
ARG2	0x27	Set Station to 101.1 MHz
ARG3	0x7E	(0x277E = 10110 with 10 kHz step size)
STATUS	→0x80	Reply Status. Clear-to-send high.

Properties are special command arguments used to modify the default device operation and are generally configured immediately after power-up. Examples of properties are TX _PREEMPHASIS and REFCLK_FREQ. A complete list of properties is available in Section “5. Commands and Properties”.

Table 3 shows an example of setting the REFCLK frequency using the REFCLK_FREQ property by sending the SET_PROPERTY command and five argument bytes. ARG1 of the SET_PROPERTY command is always 0x00. ARG2 and ARG3 are used to select the property number, PROP (0x0201 in this example), and ARG4 and ARG5 are used to set the property value, PROPD (0x8000 or 32768 Hz in the example).

Table 3. Using the SET_PROPERTY Command

Action	Data	Description
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x02	REFCLK_FREQ
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0x80	32768 Hz
ARG5 (PROPD)	0x00	
STATUS	→0x80	Reply Status. Clear-to-send high.

The implementation of the command and response procedures in the system controller differs for each of the three bus modes. Section "6. Control Interface" on page 223 details the required bit transactions on the control bus for each of the bus modes.

5. Commands and Properties

There are four different components for these product families:

1. FM Transmitter component
2. FM Receiver component
3. AM/SW/LW component
4. WB component

The following four subsections list all the commands and properties used by each of the component.

5.1. Commands and Properties for the FM/RDS Transmitter (Si4710/11/12/13/20/21)

The following two tables are the summary of the commands and properties for the FM/RDS Transmitter component applicable to Si4710/11/12/13/20/21.

Table 4. FM/RDS Transmitter Command Summary

Cmd	Name	Description	Available In
0x01	POWER_UP	Power up device and mode selection. Modes include FM transmit and analog/digital audio interface configuration.	All
0x10	GET_REV	Returns revision information on the device.	All
0x11	POWER_DOWN	Power down device.	All
0x12	SET_PROPERTY	Sets the value of a property.	All
0x13	GET_PROPERTY	Retrieves a property's value.	All
0x14	GET_INT_STATUS	Read interrupt status bits.	All
0x15	PATCH_ARGS*	Reserved command used for patch file downloads.	All
0x16	PATCH_DATA*	Reserved command used for patch file downloads.	All
0x30	TX_TUNE_FREQ	Tunes to given transmit frequency.	All
0x31	TX_TUNE_POWER	Sets the output power level and tunes the antenna capacitor.	All
0x32	TX_TUNE_MEASURE	Measure the received noise level at the specified frequency.	Si4712/13/20/21
0x33	TX_TUNE_STATUS	Queries the status of a previously sent TX Tune Freq, TX Tune Power, or TX Tune Measure command.	All
0x34	TX_ASQ_STATUS	Queries the TX status and input audio signal metrics.	All
0x35	TX_RDS_BUFF	Queries the status of the RDS Group Buffer and loads new data into buffer.	Si4711/13/21
0x36	TX_RDS_PS	Set up default PS strings.	Si4711/13/21
0x80	GPIO_CTL	Configures GPO1, 2, and 3 as output or Hi-Z.	All except Si4710-A10
0x81	GPIO_SET	Sets GPO1, 2, and 3 output level (low or high).	All except Si4710-A10

***Note:** Commands PATCH_ARGS and PATCH_DATA are only used to patch firmware. For information on applying a patch file, see "7.2. Powerup from a Component Patch" on page 233.

Table 5. FM Transmitter Property Summary

Prop	Name	Description	Default	Available In
0x0001	GPO_IEN	Enables interrupt sources.	0x0000	All
0x0101	DIGITAL_INPUT _FORMAT[1]	Configures the digital input format.	0x0000	All except Si4710-A10
0x0103	DIGITAL_INPUT _SAMPLE_RATE[1]	Configures the digital input sample rate in 1 Hz steps. Default is 0.	0x0000	All except Si4710-A10
0x0201	REFCLK_FREQ	Sets frequency of the reference clock in Hz. The range is 31130 to 34406 Hz, or 0 to disable the AFC. Default is 32768 Hz.	0x8000	All
0x0202	REFCLK_PRESCALE	Sets the prescaler value for the reference clock.	0x0001	All
0x2100	TX_COMPONENT_ENABLE	Enable transmit multiplex signal components. Default has pilot and L-R enabled.	0x0003	All
0x2101	TX_AUDIO_DEVIATION	Configures audio frequency deviation level. Units are in 10 Hz increments. Default is 6825 (68.25 kHz).	0x1AA9	All
0x2102	TX_PILOT_DEVIATION	Configures pilot tone frequency deviation level. Units are in 10 Hz increments. Default is 675 (6.75 kHz)	0x02A3	All
0x2103	TX_RDS_DEVIATION[2]	Configures the RDS/RBDS frequency deviation level. Units are in 10 Hz increments. Default is 2 kHz.	0x00C8	Si4711/13/21
0x2104	TX_LINE_INPUT_LEVEL	Configures maximum analog line input level to the LIN/RIN pins to reach the maximum deviation level programmed into the audio deviation property TX Audio Deviation. Default is 636 mV_{PK}.	0x327C	All
0x2105	TX_LINE_INPUT_MUTE	Sets line input mute. L and R inputs may be independently muted. Default is not muted.	0x0000	All
0x2106	TX_PREEMPHASIS	Configures pre-emphasis time constant. Default is 0 (75 µs).	0x0000	All

Notes:

1. Digital Audio Input feature (property DIGITAL_INPUT_FORMAT and DIGITAL_INPUT_SAMPLE_RATE) is supported in FMTX component 2.0 or later.
2. RDS feature (command TX_RDS_BUFF, TX_RDS_PS and RDS properties 0x2103, 0x2C00 through 2C07) is supported in FMTX component 2.0 or later.
3. Limiter feature (LIMITEN bit in TX_ACOMP_ENABLE and property TX_LIMITER_RELEASE_TIME) is supported in FMTX component 2.0 or later.

Table 5. FM Transmitter Property Summary (Continued)

Prop	Name	Description	Default	Available In
0x2107	TX_PILOT_FREQUENCY	Configures the frequency of the stereo pilot. Default is 19000 Hz.	0x4A38	All
0x2200	TX_ACOMP_ENABLE[3]	Enables audio dynamic range control and limiter. Default is 2 (limiter is enabled, audio dynamic range control is disabled).	0x0002	All
0x2201	TX_ACOMP_THRESHOLD	Sets the threshold level for audio dynamic range control. Default is –40 dB.	0xFFD8	All
0x2202	TX_ACOMP_ATTACK_TIME	Sets the attack time for audio dynamic range control. Default is 0 (0.5 ms).	0x0000	All
0x2203	TX_ACOMP_RELEASE_TIME	Sets the release time for audio dynamic range control. Default is 4 (1000 ms).	0x0004	All
0x2204	TX_ACOMP_GAIN	Sets the gain for audio dynamic range control. Default is 15 dB.	0x000F	All
0x2205	TX_LIMITER_RELEASE_TIME[3]	Sets the limiter release time. Default is 102 (5.01 ms)	0x0066	All except Si4710-A10
0x2300	TX_ASQ_INTERRUPT_SOURCE	Configures measurements related to signal quality metrics. Default is none selected.	0x0000	All
0x2301	TX_ASQ_LEVEL_LOW	Configures low audio input level detection threshold. This threshold can be used to detect silence on the incoming audio.	0x0000	All
0x2302	TX_ASQ_DURATION_LOW	Configures the duration which the input audio level must be below the low threshold in order to detect a low audio condition.	0x0000	All
0x2303	TX_ASQ_LEVEL_HIGH	Configures high audio input level detection threshold. This threshold can be used to detect activity on the incoming audio.	0x0000	All

Notes:

1. Digital Audio Input feature (property DIGITAL_INPUT_FORMAT and DIGITAL_INPUT_SAMPLE_RATE) is supported in FMTX component 2.0 or later.
2. RDS feature (command TX_RDS_BUFF, TX_RDS_PS and RDS properties 0x2103, 0x2C00 through 2C07) is supported in FMTX component 2.0 or later.
3. Limiter feature (LIMITEN bit in TX_ACOMP_ENABLE and property TX_LIMITER_RELEASE_TIME) is supported in FMTX component 2.0 or later.

Table 5. FM Transmitter Property Summary (Continued)

Prop	Name	Description	Default	Available In
0x2304	TX_ASQ_DURATION_HIGH	Configures the duration which the input audio level must be above the high threshold in order to detect a high audio condition.	0x0000	All
0x2C00	TX_RDS_INTERRUPT_SOURCE[2]	Configure RDS interrupt sources. Default is none selected.	0x0000	Si4711/13/21
0x2C01	TX_RDS_PI[2]	Sets transmit RDS program identifier.	0x40A7	Si4711/13/21
0x2C02	TX_RDS_PS_MIX[2]	Configures mix of RDS PS Group with RDS Group Buffer.	0x0003	Si4711/13/21
0x2C03	TX_RDS_PS_MISC[2]	Miscellaneous bits to transmit along with RDS_PS Groups.	0x1008	Si4711/13/21
0x2C04	TX_RDS_PS_REPEAT_COUNT[2]	Number of times to repeat transmission of a PS message before transmitting the next PS message.	0x0003	Si4711/13/21
0x2C05	TX_RDS_PS_MESSAGE_COUNT[2]	Number of PS messages in use.	0x0001	Si4711/13/21
0x2C06	TX_RDS_PS_AF[2]	RDS Program Service Alternate Frequency. This provides the ability to inform the receiver of a single alternate frequency using AF Method A coding and is transmitted along with the RDS_PS Groups.	0xE0E0	Si4711/13/21
0x2C07	TX_RDS_FIFO_SIZE[2]	Number of blocks reserved for the FIFO. Note that the value written must be one larger than the desired FIFO size.	0x0000	Si4711/13/21

Notes:

1. Digital Audio Input feature (property DIGITAL_INPUT_FORMAT and DIGITAL_INPUT_SAMPLE_RATE) is supported in FMTX component 2.0 or later.
2. RDS feature (command TX_RDS_BUFF, TX_RDS_PS and RDS properties 0x2103, 0x2C00 through 2C07) is supported in FMTX component 2.0 or later.
3. Limiter feature (LIMITEN bit in TX_ACOMP_ENABLE and property TX_LIMITER_RELEASE_TIME) is supported in FMTX component 2.0 or later.

Table 6. Status Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	RDSINT	ASQINT	STCINT

Bit	Name	Function
7	CTS	**Clear to Send.** 0 = Wait before sending next command. 1 = Clear to send next command.
6	ERR	**Error.** 0 = No error 1 = Error
5:3	Reserved	Values may vary.
2	RDSINT	**RDS Interrupt.** 0 = RDS interrupt has not been triggered. 1 = RDS interrupt has been triggered.
1	ASQINT	**Signal Quality Interrupt.** 0 = Signal quality measurement has not been triggered. 1 = Signal quality measurement has been triggered.
0	STCINT	**Seek/Tune Complete Interrupt.** 0 = Tune complete has not been triggered. 1 = Tune complete has been triggered.

5.1.1. Commands and Properties for the FM/RDS Transmitter

Command 0x01. POWER_UP

Initiates the boot process to move the device from powerdown to powerup mode. The boot can occur from internal device memory or a system controller downloaded patch. To confirm that the patch is compatible with the internal device library revision, the library revision should be confirmed by issuing the POWER_UP command with Function = 15 (query library ID). The device will return the response, including the library revision, and then moves into powerdown mode. The device can then be placed in powerup mode by issuing the POWER_UP command with Function = 2 (transmit) and the patch may be applied. Only the STATUS byte will be returned in the response stream in transmit mode. The POWER_UP command configures the state of DIN (pin 13), DFS (pin 14), and RIN (pin 15) and LIN (pin 16) for analog or digital audio modes and GPO2/INT (pin 18) for interrupt operation. The command configures GPO2/INT interrupts (GPO2OEN) and CTS interrupts (CTSIEN). If both are enabled, GPO2/INT is driven high during normal operation and low for a minimum of 1 µs during the interrupt. The CTSIEN bit is duplicated in the GPO_IEN property. The command is complete when the CTS bit (and optional interrupt) is set.

Note: To change function (e.g., FM TX to FM RX), issue the POWER_DOWN command to stop the current function; then, issue POWER_UP to start the new function.

Note: Delay at least 500 ms between powerup command and first tune command to wait for the oscillator to stabilize if XOSCEN is set and crystal is used as the RCLK.

Available in: All

Command Arguments: Two

Response Bytes: None (FUNC = 2), Seven (FUNC = 15)

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	0	0	0	0	1
ARG1	CTSIEN	GPO2OEN	PATCH	XOSCEN	FUNC[3:0]			
ARG2	OPMODE[7:0]							

ARG	Bit	Name	Function
1	7	CTSIEN	**CTS Interrupt Enable.** 0 = CTS interrupt disabled. 1 = CTS interrupt enabled.
1	6	GPO2OEN	**GPO2 Output Enable.** 0 = GPO2 output disabled, (Hi-Z). 1 = GPO2 output enabled.
1	5	PATCH	**Patch Enable.** 0 = Boot normally 1 = Copy non-volatile memory to RAM, but do not boot. After CTS has been set, RAM may be patched
1	4	XOSCEN	**Crystal Oscillator Enable.** 0 = Use external RCLK (crystal oscillator disabled). 1 = Use crystal oscillator (RCLK and GPO3/DCLK with external 32.768 kHz crystal and OPMODE = 01010000). See Si47xx Data Sheet Application Schematic for external BOM details.

ARG	Bit	Name	Function
1	3:0	FUNC[3:0]	**Function.** 0–1, 3–14 = Reserved. 2 = Transmit. 15 = Query Library ID.
2	7:0	OPMODE[7:0]	**Application Setting** 01010000 = Analog audio inputs (LIN/RIN) 00001111 = Digital audio inputs (DIN/DFS/DCLK)

Response (to FUNC = 2, TX)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	RDSINT	ASQINT	STCINT

Response (to FUNC = 15, Query Library ID)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	RDSINT	ASQINT	STCINT
RESP1	PN[7:0]							
RESP2	FWMAJOR[7:0]							
RESP3	FWMINOR[7:0]							
RESP4	RESERVED[7:0]							
RESP5	RESERVED[7:0]							
RESP6	CHIPREV[7:0]							
RESP7	LIBRARYID[7:0]							

RESP	Bit	Name	Function
1	7:0	PN[7:0]	**Final 2 digits of part number.**
2	7:0	FWMAJOR[7:0]	**Firmware Major Revision.**
3	7:0	FWMINOR[7:0]	**Firmware Minor Revision.**
4	7:0	RESERVED[7:0]	**Reserved, various values.**
5	7:0	RESERVED[7:0]	**Reserved, various values.**
6	7:0	CHIPREV[7:0]	**Chip Revision.**
7	7:0	LIBRARYID[7:0]	**Library Revision.**

Command 0x10. GET_REV

Returns the part number, chip revision, firmware revision, patch revision and component revision numbers. The command is complete when the CTS bit (and optional interrupt) is set. This command may only be sent when in powerup mode.

Available in: All

Command arguments: None

Response bytes: Eight

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	0	0

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	RDSINT	ASQINT	STCINT
RESP1	PN[7:0]							
RESP2	FWMAJOR[7:0]							
RESP3	FWMINOR[7:0]							
RESP4	$PATCH_H$[7:0]							
RESP5	$PATCH_L$[7:0]							
RESP6	CMPMAJOR[7:0]							
RESP7	CMPMINOR[7:0]							
RESP8	CHIPREV[7:0]							

RESP	Bit	Name	Function
1	7:0	PN[7:0]	**Final 2 digits of Part Number**
2	7:0	FWMAJOR[7:0]	**Firmware Major Revision**
3	7:0	FWMINOR[7:0]	**Firmware Minor Revision**
4	7:0	$PATCH_H$[7:0]	**Patch ID High Byte**
5	7:0	$PATCH_L$[7:0]	**Patch ID Low Byte**
6	7:0	CMPMAJOR[7:0]	**Component Major Revision**
7	7:0	CMPMINOR[7:0]	**Component Minor Revision**
8	7:0	CHIPREV[7:0]	**Chip Revision**

Command 0x11. POWER_DOWN

Moves the device from powerup to powerdown mode. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode. Note that only the POWER_UP command is accepted in powerdown mode. **If the system controller writes a command other than POWER_UP when in powerdown mode, the device does not respond. The device will only respond when a POWER_UP command is written. GPO pins are powered down and not active during this state. For optimal power down current, GPO2 must be either internally driven low through GPIO_CTL command or externally driven low.**

Note: In FMTX component 1.0 and 2.0, a reset is required when the system controller writes a command other than POWER_UP when in powerdown mode.

Note: The following describes the state of all the pins when in powerdown mode:
GPIO1, GPIO2, and GPIO3 = 0
DIN, DFS, RIN, LIN = HiZ

Available in: All

Command arguments: None

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	0	1

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	RDSINT	ASQINT	STCINT

Command 0x12. SET_PROPERTY

Sets a property shown in Table 5, “FM Transmitter Property Summary,” on page 8. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode.

See Figure 30, “CTS and SET_PROPERTY Command Complete tCOMP Timing Model,” on page 243 and Table 49, “Command Timing Parameters for the FM Transmitter,” on page 244.

Available in: All

Command Arguments: Five

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	1	0
ARG1	0	0	0	0	0	0	0	0
ARG2	$PROP_H$[7:0]							
ARG3	$PROP_L$[7:0]							
ARG4	$PROPD_H$[7:0]							
ARG5	$PROPD_L$[7:0]							

ARG	Bit	Name	Function
1	7:0	Reserved	Always write to 0.
2	7:0	$PROP_H$[7:0]	**Property High Byte.** This byte in combination with $PROP_L$ is used to specify the property to modify. See Section "5.1.2. FM/RDS Transmitter Properties" on page 31.
3	7:0	$PROP_L$[7:0]	**Property Low Byte.** This byte in combination with $PROP_H$ is used to specify the property to modify. See Section "5.1.2. FM/RDS Transmitter Properties" on page 31.
4	7:0	$PROPD_H$[7:0]	**Property Value High Byte.** This byte in combination with $PROPV_L$ is used to set the property value. See Section "5.1.2. FM/RDS Transmitter Properties" on page 31.
5	7:0	$PROPD_L$[7:0]	**Property Value Low Byte.** This byte in combination with $PROPV_H$ is used to set the property value. See Section "5.1.2. FM/RDS Transmitter Properties" on page 31.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	RDSINT	ASQINT	STCINT

Command 0x13. GET_PROPERTY

Gets a property shown in Table 5, “FM Transmitter Property Summary,” on page 8. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode.

Available in: All

Command arguments: Three

Response bytes: Three

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	1	1
ARG1	0	0	0	0	0	0	0	0
ARG2	$PROP_H$[7:0]							
ARG3	$PROP_L$[7:0]							

ARG	Bit	Name	Function
1	7:0	Reserved	Always write to 0.
2	7:0	$PROP_H$[7:0]	**Property Get High Byte.** This byte in combination with $PROP_L$ is used to specify the property to get.
3	7:0	$PROP_L$[7:0]	**Property Get Low Byte.** This byte in combination with $PROP_H$ is used to specify the property to get.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	RDSINT	ASQINT	STCINT
RESP1	X	X	X	X	X	X	X	X
RESP2	$PROPD_H$[7:0]							
RESP3	$PROPD_L$[7:0]							

RESP	Bit	Name	Function
1	7:0	Reserved	Reserved, various values.
2	7:0	$PROPD_H$[7:0]	**Property Value High Byte.** This byte in combination with $PROPV_L$ will represent the requested property value.
3	7:0	$PROPD_L$[7:0]	**Property Value High Byte.** This byte in combination with $PROPV_H$ will represent the requested property value.

Command 0x14. GET_INT_STATUS

Updates bits 6:0 of the status byte. This command should be called after any command that sets the STCINT, ASQINT, or RDSINT bits. When polling this command should be periodically called to monitor the STATUS byte, and when using interrupts, this command should be called after the interrupt is set to update the STATUS byte. The command is complete when the CTS bit (and optional interrupt) is set. This command may only be sent when in powerup mode.

Available in: All

Command arguments: None

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	1	0	0

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	RDSINT	ASQINT	STCINT

Command 0x30. TX_TUNE_FREQ

Sets the state of the RF carrier and sets the tuning frequency between 76 and 108 MHz in 10 kHz units and steps of 50 kHz. For example 76.05 MHz = 7605 is valid because it follows the 50 kHz step requirement but 76.01 MHz = 7601 is not valid. The CTS bit (and optional interrupt) is set when it is safe to send the next command. The ERR bit (and optional interrupt) is set if an invalid argument is sent. Note that only a single interrupt occurs if both the CTS and ERR bits are set. The optional STC interrupt is set when the command completes. The STCINT bit is set only after the GET_INT_STATUS command is called. This command may only be sent when in powerup mode. The command clears the STC bit if it is already set. See Figure 29, “CTS and STC Timing Model,” on page 243 and Table 49, “Command Timing Parameters for the FM Transmitter,” on page 244.

Available in: All

Command arguments: Three

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	1	1	0	0	0	0
ARG1	0	0	0	0	0	0	0	0
ARG2	$FREQ_H$[7:0]							
ARG3	$FREQ_L$[7:0]							

ARG	Bit	Name	Function
1	7:0	Reserved	Always write to 0.
2	7:0	$FREQ_H$[7:0]	**Tune Frequency High Byte.** This byte in combination with $FREQ_L$ selects the tune frequency in units of 10 kHz. The valid range is from 7600 to 10800 (76–108 MHz). The frequency must be a multiple of 50 kHz.
3	7:0	$FREQ_L$[7:0]	**Tune Frequency Low Byte.** This byte in combination with $FREQ_H$ selects the tune frequency in units of 10 kHz. The valid range is from 7600 to 10800 (76–108 MHz). The frequency must be a multiple of 50 kHz.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	RDSINT	ASQINT	STCINT

Command 0x31. TX_TUNE_POWER

Sets the RF voltage level between 88 dBµV and 115 dBµV in 1 dB units. Power may be set as high as 120 dBµV; however, voltage accuracy is not guaranteed. A value of 0x00 indicates off. The command also sets the antenna tuning capacitance. A value of 0 indicates autotuning, and a value of 1–191 indicates a manual override. The CTS bit (and optional interrupt) is set when it is safe to send the next command. The ERR bit (and optional interrupt) is set if an invalid argument is sent. Note that only a single interrupt occurs if both the CTS and ERR bits are set. The optional STC interrupt is set when the command completes. The STCINT bit is set only after the GET_INT_STATUS command is called. This command may only be sent when in powerup mode. The command clears the STC bit if it is already set. See Figure 29, “CTS and STC Timing Model,” on page 243 and Table 49, “Command Timing Parameters for the FM Transmitter,” on page 244.

Available in: All

Command arguments: Four

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	1	1	0	0	0	1
ARG1	0	0	0	0	0	0	0	0
ARG2	0	0	0	0	0	0	0	0
ARG3	RFdBµV[7:0]							
ARG4	ANTCAP[7:0]							

ARG	Bit	Name	Function
1	7:0	Reserved	Always write to 0.
2	7:0	Reserved	Always write to 0.
3	7:0	RFdBµV[7:0]	**Tune Power Byte.** Sets the tune power in dBµV in 1 dB steps. The valid range is from 88–115 dBµV. Power may be set as high as 120 dBµV; however, voltage accuracy is not guaranteed.
4	7:0	ANTCAP[7:0]	**Antenna Tuning Capacitor.** This selects the value of the antenna tuning capacitor manually, or automatically if set to zero. The valid range is 0 to 191, which results in a tuning capacitance of 0.25 pF x ANTCAP.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	RDSINT	ASQINT	STCINT

Command 0x32. TX_TUNE_MEASURE

Enters receive mode (disables transmitter output power) and measures the received noise level (RNL) in units of dBµV on the selected frequency. The command sets the tuning frequency between 76 and 108 MHz in 10 kHz units and steps of 50 kHz. For example 76.05 MHz = 7605 is valid because it follows the 50 kHz step requirement but 76.01 MHz = 7601 is not valid. The command also sets the antenna tuning capacitance. A value of 0 indicates autotuning, and a value of 1–191 indicates a manual override. The CTS bit (and optional interrupt) is set when it is safe to send the next command. The ERR bit (and optional interrupt) is set if an invalid argument is sent. Note that only a single interrupt occurs if both the CTS and ERR bits are set. The optional STC interrupt is set when the command completes. The STCINT bit is set only after the GET_INT_STATUS command is called. This command may only be sent when in powerup mode. The command clears the STC bit if it is already set. See Figure 29, “CTS and STC Timing Model,” on page 243 and Table 49, “Command Timing Parameters for the FM Transmitter,” on page 244.

Available in: Si4712/13/20/21

Command arguments: Four

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	1	1	0	0	1	0
ARG1	0	0	0	0	0	0	0	0
ARG2	$FREQ_H$[7:0]							
ARG3	$FREQ_L$[7:0]							
ARG4	ANTCAP[7:0]							

ARG	Bit	Name	Function
1	7:0	Reserved	Always write to 0.
2	7:0	$FREQ_H$[7:0]	**Tune Frequency High Byte.** This byte in combination with $FREQ_L$ selects the tune frequency in units of 10 kHz. In FM mode the valid range is from 7600 to 10800 (76–108 MHz). The frequency must be a multiple of 50 kHz.
3	7:0	$FREQ_L$[7:0]	**Tune Frequency Low Byte.** This byte in combination with $FREQ_H$ selects the tune frequency in units of 10 kHz. In FM mode the valid range is from 7600 to 10800 (76–108 MHz). The frequency must be a multiple of 50 kHz.
4	7:0	ANTCAP[7:0]	**Antenna Tuning Capacitor.** This selects the value of the antenna tuning capacitor manually, or automatic if set to zero. The valid range is 0–191.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	RDSINT	ASQINT	STCINT

Command 0x33. TX_TUNE_STATUS

Returns the status of the TX_TUNE_FREQ, TX_TUNE_MEASURE, or TX_TUNE_POWER commands. The command returns the current frequency, output voltage in dBµV (if applicable), the antenna tuning capacitance value (0–191) and the received noise level (if applicable). The command clears the STCINT interrupt bit when INTACK bit of ARG1 is set. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode.

Available in: All

Command arguments: One

Response bytes: Seven

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	1	1	0	0	1	1
ARG1	0	0	0	0	0	0	0	INTACK

ARG	Bit	Name	Function
1	7:1	Reserved	Always write to 0.
1	0	INTACK	**Seek/Tune Interrupt Clear.** If set this bit clears the seek/tune complete interrupt status indicator.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	RDSINT	ASQINT	STCINT
RESP1	X	X	X	X	X	X	X	X
RESP2	$READFREQ_H$[7:0]							
RESP3	$READFREQ_L$[7:0]							
RESP4	X	X	X	X	X	X	X	X
RESP5	READRFdBµV[7:0]							
RESP6	READANTCAP[7:0]							
RESP7	RNL[7:0]							

RESP	Bit	Name	Function
1	7:0	Reserved	Returns various data.
2	7:0	$READFREQ_H$[7:0]	**Read Frequency High Byte.** This byte in combination with $READFREQ_L$ returns frequency being tuned.
3	7:0	$READFREQ_L$[7:0]	**Read Frequency Low Byte.** This byte in combination with $READFREQ_H$ returns frequency being tuned.
4	7:0	Reserved	Returns various data.
5	7:0	READRFdBµV[7:0]	**Read Power.** Returns the transmit output voltage setting.
6	7:0	READANTCAP [7:0]	**Read Antenna Tuning Capacitor.** This byte will contain the current antenna tuning capacitor value.
7	7:0	RNL[7:0]	**Read Received Noise Level (Si4712/13 Only).** This byte will contain the receive level as the response to a TX Tune Measure command. The returned value will be the last RNL measurement (or 0 if no measurement has been performed) for the TX Tune Freq and TX Tune Power commands.

Command 0x34. TX_ASQ_STATUS

Returns status information about the audio signal quality and current FM transmit frequency. This command can be used to check if the input audio stream is below a low threshold as reported by the IALL bit, or above a high threshold as reported by the IALH bit. The thresholds can be configured to detect a silence condition or an activity condition which can then be used by the host to take an appropriate action such as turning off the carrier in the case of prolonged silence. The thresholds are set using the TX_ASQ_LEVEL_LOW and TX_ASQ_LEVEL_HIGH properties. The audio must be above or below the threshold for greater than the amount of time specified in the TX_ASQ_DURATION_LOW and TX_ASQ_DURATION_HIGH properties for the status to be detected. Additionally the command can be used to determine if an overmodulation condition has occurred or the limiter has engaged, as reported by the OVERMOD bit, in which case the host could reduce the audio level to the part. If any of the OVERMOD, IALH, or IALL bits are set, the ASQINT bit will also be set. The ASQINT bit can be routed to a hardware interrupt via the GPO_IEN property.

Clearing the IALH or IALL interrupts will result in the TX_ASQ_DURATION_LOW or TX_ASQ_DURATION_HIGH counters being rearmed, respectively, to start another detection interval measurement. The command clears the ASQINT interrupt bit and OVERMOD, IALH, and IALL bits when the INTACK bit of ARG1 is set. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode.

Note that the TX_ASQ_DURATION_LOW and TX_ASQ_DURATION_HIGH counters start and the TX_ASQ_STATUS command will only return valid data after a call to TX_TUNE_FREQ, TX_TUNE_POWER, or TX_TUNE_MEASURE.

Available in: All

Command arguments: One

Response bytes: Four

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	1	1	0	1	0	0
ARG1	0	0	0	0	0	0	0	INTACK

ARG	Bit	Name	Function
1	0	INTACK	**Interrupt Acknowledge.** 0 = Interrupt status preserved. 1 = Clears ASQINT, OVERMOD, IALDH, and IALDL.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	RDSINT	ASQINT	STCINT
RESP1	X	X	X	X	X	OVERMOD	IALH	IALL
RESP2	X	X	X	X	X	X	X	X
RESP3	X	X	X	X	X	X	X	X
RESP4	INLEVEL[7:0]							

RESP	Bit	Name	Function
1	2	OVERMOD	**Overmodulation Detection.** 0 = Output signal is below requested modulation level. 1 = Output signal is above requested modulation level.
1	1	IALH	**Input Audio Level Threshold Detect High.** 0 = Input audio level high threshold not exceeded. 1 = Input audio level high threshold exceeded.
1	0	IALL	**Input Audio Level Threshold Detect Low.** 0 = Input audio level low threshold not exceeded. 1 = Input audio level low threshold exceeded.
2	7:0	Reserved	**Returns various values.**
3	7:0	Reserved	**Returns various values.**
4	7:0	INLEVEL[7:0]	**Input Audio Level.** The current audio input level measured in dBfs (2s complement notation).

Command 0x35. TX_RDS_BUFF

Loads or clears the RDS group buffer FIFO or circular buffer and returns the FIFO status. The buffer can be allocated between the circular buffer and FIFO with the TX_RDS_FIFO_SIZE property. A common use case for the circular buffer is to broadcast group 2A radio text, and a common use case for the FIFO is to broadcast group 4A real time clock. The command clears the INTACK interrupt bit when the INTACK bit of ARG1 is set. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode.

Note: TX_RDS_BUFF is supported in FMTX component 2.0 or later.

Available in: Si4711/13/21

Command arguments: Seven

Response bytes: Five

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	1	1	0	1	0	1
ARG1	FIFO	0	0	0	0	LDBUFF	MTBUFF	INTACK
ARG2	$RDSB_H$[7:0]							
ARG3	$RDSB_L$[7:0]							
ARG4	$RDSC_H$[7:0]							
ARG5	$RDSC_L$[7:0]							
ARG6	$RDSD_H$[7:0]							
ARG7	$RDSD_L$[7:0]							

ARG	Bit	Name	Function
1	7	FIFO	**Operate on FIFO.** If set, the command operates on the FIFO buffer. If cleared, the command operates on the circular buffer.
1	6:3	Reserved	Always write to 0.
1	2	LDBUFF	**Load RDS Group Buffer.** If set, loads the RDS group buffer with RDSB, RDSC, and RDSD. Block A data is generated from the RDS_TX_PI property when the buffer is transmitted.
1	1	MTBUFF	**Empty RDS Group Buffer.** If set, empties the RDS group buffer.
1	0	INTACK	**Clear RDS Group buffer interrupt.** If set this bit clears the RDS group buffer interrupt indicator.
2	7:0	$RDSB_H$[7:0]	**RDS Block B High Byte.** This byte in combination with $RDSB_L$ sets the RDS block B data.
3	7:0	$RDSB_L$[7:0]	**RDS Block B Low Byte.** This byte in combination with $RDSB_H$ sets the RDS block B data.

ARG	Bit	Name	Function
4	7:0	$RDSC_H$[7:0]	**RDS Block C High Byte.** This byte in combination with $RDSC_L$ sets the RDS block C data.
5	7:0	$RDSC_L$[7:0]	**RDS Block C Low Byte.** This byte in combination with $RDSC_H$ sets the RDS block C data.
6	7:0	$RDSD_H$[7:0]	**RDS Block D High Byte.** This byte in combination with $RDSD_L$ sets the RDS block D data.
7	7:0	$RDSD_L$[7:0]	**RDS Block D Low Byte.** This byte in combination with $RDSD_H$ sets the RDS block D data.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	RDSINT	ASQINT	STCINT
RESP1	X	X	X	RDSPSXMIT	CBUFXMIT	FIFOXMIT	CBUFWRAP	FIFOMT
RESP2	CBAVAIL[7:0]							
RESP3	CBUSED[7:0]							
RESP4	FIFOAVAIL[7:0]							
RESP5	FIFOUSED[7:0]							

RESP	Bit	Name	Function
1	7:5	Reserved	Values may vary.
1	4	RDSPSXMIT	Interrupt source: RDS PS Group has been transmitted.
1	3	CBUFXMIT	Interrupt source: RDS Group has been transmitted from the FIFO buffer.
1	2	FIFOXMIT	Interrupt source: RDS Group has been transmitted from the circular buffer.
1	1	CBUFWRAP	Interrupt source: RDS Group Circular Buffer has wrapped.
1	0	FIFOMT	Interrupt source: RDS Group FIFO Buffer is empty.
2	7:0	CBAVAIL[7:0]	Returns the number of available Circular Buffer blocks.
3	7:0	CBUSED[7:0]	Returns the number of used Circular Buffer blocks.
4	7:0	FIFOAVAIL[7:0]	Returns the number of available FIFO blocks.
5	7:0	FIFOUSED[7:0]	Returns the number of used FIFO blocks.

Command 0x36. TX_RDS_PS

Loads or clears the program service buffer. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode.

Note: TX_RDS_PS is supported in FMTX component 2.0 or later.

Available in: Si4711/13/21

Command arguments: Five

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	1	1	0	1	1	0
ARG1	0	0	0	PSID[4:0]				
ARG2	PSCHAR0 [7:0]							
ARG3	PSCHAR1 [7:0]							
ARG4	PSCHAR2 [7:0]							
ARG5	PSCHAR3 [7:0]							

ARG	Bit	Name	Function
1	7:5	Reserved	Always write to 0.
1	4:0	PSID[4:0]	Selects which PS data to load (0–23) 0 = First 4 characters of PS0. 1 = Last 4 characters of PS0. 2 = First 4 characters of PS1. 3 = Last 4 characters of PS1. . . 22 = First 4 characters of PS11. 23 = Last 4 characters of PS11.
2	7:0	PSCHAR0[7:0]	**RDS PSID CHAR0.** First character of selected PSID.
3	7:0	PSCHAR1[7:0]	**RDS PSID CHAR1.** Second character of selected PSID.
4	7:0	PSCHAR2[7:0]	**RDS PSID CHAR2.** Third character of selected PSID.
5	7:0	PSCHAR3[7:0]	**RDS PSID CHAR3.** Fourth character of selected PSID.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	RDSINT	ASQINT	STCINT

Command 0x80. GPIO_CTL

Enables output for GPO1, 2, and 3. GPO1, 2, and 3 can be configured for output (Hi-Z or active drive) by setting the GPO1OEN, GPO2OEN, and GPO3OEN bit. The state (high or low) of GPO1, 2, and 3 is set with the GPIO_SET command. To avoid excessive current consumption due to oscillation, GPO pins should not be left in a high impedance state. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode. The default is all GPO pins set for high impedance.

Notes:

1. GPIO_CTL is fully supported in FMTX component 3.0 or later. Only bit GPO3OEN is supported in FMTX comp 2.0.
2. The use of GPO2 as an interrupt pin and/or the use of GPO3 as DCLK digital clock input will override this GPIO_CTL function for GPO2 and/or GPO3 respectively.

Available in: All except Si4710-A10

Command arguments: One

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	1	0	0	0	0	0	0	0
ARG1	0	0	0	0	GPO3OEN	GPO2OEN	GPO1OEN	0

ARG	Bit	Name	Function
1	7:4	Reserved	Always write 0.
1	3	GPO3OEN	**GPO3 Output Enable.** 0 = Output Disabled (Hi-Z) (default). 1 = Output Enabled.
1	2	GPO2OEN	**GPO2 Output Enable.** 0 = Output Disabled (Hi-Z) (default). 1 = Output Enabled.
1	1	GPO1OEN	**GPO1 Output Enable.** 0 = Output Disabled (Hi-Z) (default). 1 = Output Enabled.
1	0	Reserved	Always write 0.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	RDSINT	ASQINT	STCINT

Command 0x81. GPIO_SET

Sets the output level (high or low) for GPO1, 2, and 3. GPO1, 2, and 3 can be configured for output by setting the GPO1OEN, GPO2OEN, and GPO3OEN bit in the GPIO_CTL command. To avoid excessive current consumption due to oscillation, GPO pins should not be left in a high impedance state. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is all GPO pins set for high impedance.

Note: GPIO_SET is fully-supported in FMTX comp 3.0 or later. Only bit GPO3LEVEL is supported in FMTX comp 2.0.

Available in: All except Si4710-A10

Command arguments: One

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	1	0	0	0	0	0	0	1
ARG1	0	0	0	0	GPO3LEVEL	GPO2LEVEL	GPO1LEVEL	0

ARG	Bit	Name	Function
1	7:4	Reserved	Always write 0.
1	3	GPO3LEVEL	**GPO3 Output Level.** 0 = Output low (default). 1 = Output high.
1	2	GPO2LEVEL	**GPO3 Output Level.** 0 = Output low (default). 1 = Output high.
1	1	GPO1LEVEL	**GPO3 Output Level.** 0 = Output low (default). 1 = Output high.
1	0	Reserved	Always write 0.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	RDSINT	ASQINT	STCINT

5.1.2. FM/RDS Transmitter Properties

Property 0x0001. GPO_IEN

Configures the sources for the GPO2/INT interrupt pin. Valid sources are the lower 8 bits of the STATUS byte, including CTS, ERR, RDSINT, ASQINT, and STCINT bits. The corresponding bit is set before the interrupt occurs. The CTS bit (and optional interrupt) is set when it is safe to send the next command. The CTS interrupt enable (CTSIEN) can be set with this property and the POWER_UP command. The state of the CTSIEN bit set during the POWER_UP command can be read by reading the this property and modified by writing this property. This property may only be set or read when in powerup mode. The default is no interrupts enabled.

Available in: All

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	RDSREP	ASQREP	STCREP	CTSIEN	ERRIEN	0	0	0	RDSIEN	ASQIEN	STCIEN

Bit	Name	Function
15:11	Reserved	Always write to 0.
10	RDSREP	**RDS Interrupt Repeat. (Si4711/13/21 Only)** 0 = No interrupt generated when RDSINT is already set (default). 1 = Interrupt generated even if RDSINT is already set.
9	ASQREP	**ASQ Interrupt Repeat.** 0 = No interrupt generated when ASQREP is already set (default). 1 = Interrupt generated even if ASQREP is already set.
8	STCREP	**STC Interrupt Repeat.** 0 = No interrupt generated when STCREP is already set (default). 1 = Interrupt generated even if STCREP is already set.
7	CTSIEN	**CTS Interrupt Enable.** 0 = No interrupt generated when CTS is set (default). 1 = Interrupt generated when CTS is set. After PowerUp, this bit will reflect the CTSIEN bit in ARG1 of PowerUp Command.
6	ERRIEN	**ERR Interrupt Enable.** 0 = No interrupt generated when ERR is set (default). 1 = Interrupt generated when ERR is set.
5:3	Reserved	Always write to 0.
2	RDSIEN	**RDS Interrupt Enable (Si4711/13/21 Only).** 0 = No interrupt generated when RDSINT is set (default). 1 = Interrupt generated when RDSINT is set.
1	ASQIEN	**Audio Signal Quality Interrupt Enable.** 0 = No interrupt generated when ASQINT is set (default). 1 = Interrupt generated when ASQINT is set.
0	STCIEN	**Seek/Tune Complete Interrupt Enable.** 0 = No interrupt generated when STCINT is set (default). 1 = Interrupt generated when STCINT is set.

Property 0x0101. DIGITAL_INPUT_FORMAT

Configures the digital input format. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode.

Note: DIGITAL_INPUT_FORMAT is supported in FMTX component 2.0 or later.

Available in: All except Si4710-A10

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	IFALL	IMODE[3:0]				IMONO	ISIZE[1:0]	

Bit	Name	Function
15:8	Reserved	Always write to 0.
7	IFALL	**DCLK Falling Edge.** 0 = Sample on DCLK rising edge (default). 1 = Sample on DCLK falling edge.
6:3	IMODE[3:0]	**Digital Mode.** 0000 = default 0001 = I^2S Mode. 0111 = Left-justified mode. 1101 = MSB at 1^{st} DCLK rising edge after DFS Pulse. 1001 = MSB at 2^{nd} DCLK rising edge after DFS Pulse.
2	IMONO	**Mono Audio Mode.** 0 = Stereo audio mode (default). 1 = Mono audio mode.
1:0	ISIZE[1:0]	**Digital Audio Sample Precision.** 00 = 6 bits (default) 01 = 20 bits 10 = 24 bits 11 = 8 bits

Property 0x0103. DIGITAL_INPUT_SAMPLE_RATE

Configures the digital input sample rate in 1 Hz units. The input sample rate must be set to 0 before removing the DCLK input or reducing the DCLK frequency below 2 MHz. If this guideline is not followed, a device reset will be required. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. TX_TUNE_FREQ command must be sent after the POWER_UP command to start the internal clocking before setting this property.

Note: DIGITAL_INPUT_SAMPLE_RATE is supported in FMTX component 2.0 or later.

Available in: All except Si4710-A10

Default: 0x0000

Units: 1 Hz

Step: 1 Hz

Range: 0, 32000-48000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DISR[15:0]															

Bit	Name	Function
15:0	DISR	**Digital Input Sample Rate.** 0 = Disabled. Required before removing DCLK or reducing DCLK frequency below 2 MHz. The range is 32000–48000 Hz.

Property 0x0201. REFCLK_FREQ

Sets the frequency of the REFCLK from the output of the prescaler. (Figure 1 shows the relation between RCLK and REFCLK.) The REFCLK range is 31130 to 34406 Hz (32768 ±5% Hz) in 1 Hz steps, or 0 (to disable AFC). For example, an RCLK of 13 MHz would require a prescaler value of 400 to divide it to 32500 Hz REFCLK. The reference clock frequency property would then need to be set to 32500 Hz. RCLK frequencies between 31130 Hz and 40 MHz are supported, however, there are gaps in frequency coverage for prescaler values ranging from 1 to 10, or frequencies up to 311300 Hz. Table 7 summarizes these RCLK gaps.

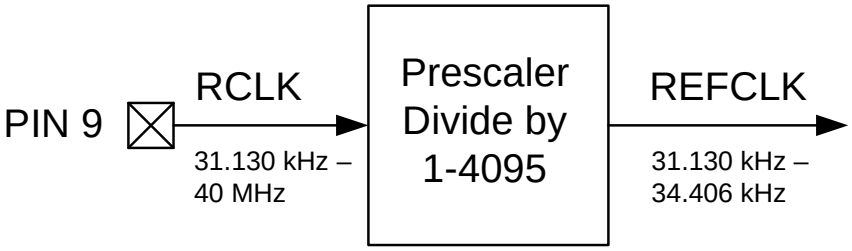


Figure 1. REFCLK Prescaler

Table 7. RCLK Gaps

Prescaler	RCLK Low (Hz)	RCLK High (Hz)
1	31130	34406
2	62260	68812
3	93390	103218
4	124520	137624
5	155650	172030
6	186780	206436
7	217910	240842
8	249040	275248
9	280170	309654
10	311300	344060

The RCLK must be valid 10 ns before and 10 ns after sending the TX_TUNE_MEASURE, TX_TUNE_FREQ, or TX_TUNE_POWER commands. In addition, the RCLK must be valid at all times when the carrier is enabled for proper AFC operation. The RCLK may be removed or reconfigured at other times. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 32768 Hz.

Available in: All

Default: 0x8000 (32768)

Units: 1 Hz

Step: 1 Hz

Range: 31130–34406

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	REFCLKF[15:0]															

Bit	Name	Function
15:0	REFCLKF[15:0]	**Frequency of Reference Clock in Hz.** The allowed REFCLK frequency range is between 31130 and 34406 Hz (32768 ±5%), or 0 (to disable AFC).

Property 0x0202. REFCLK_PRESCALE

Sets the number used by the prescaler to divide the external RCLK down to the internal REFCLK. The range may be between 1 and 4095 in 1 unit steps. For example, an RCLK of 13 MHz would require a prescaler value of 400 to divide it to 32500 Hz. The reference clock frequency property would then need to be set to 32500 Hz. The RCLK must be valid 10 ns before and 10 ns after sending the TX_TUNE_MEASURE, TX_TUNE_FREQ, or TX_TUNE_POWER commands. In addition, the RCLK must be valid at all times when the carrier is enabled for proper AFC operation. The RCLK may be removed or reconfigured at other times. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 1.

Available in: All

Default: 0x0001

Step: 1

Range: 1–4095

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	RCLKSEL	RCLKP[11:0]											

Bit	Name	Function
15:13	Reserved	Always write to 0.
12	RCLKSEL	**RCLKSEL.** 0 = RCLK pin is clock source. 1 = DCLK pin is clock source.
11:0	REFCLKP[11:0]	**Prescaler for Reference Clock.** Integer number used to divide the RCLK frequency down to REFCLK frequency. The allowed REFCLK frequency range is between 31130 and 34406 Hz (32768 ±5%), or 0 (to disable AFC).

Property 0x2100. TX_COMPONENT_ENABLE

Individually enables the stereo pilot, left minus right stereo and RDS components. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is stereo pilot and left minus right stereo components enabled.

Available in: All

Default: 0x0003

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	RDS	LMR	PILOT

Bit	Name	Function
15:3	Reserved	Always write 0.
2	RDS	**RDS Enable (Si4711/13/21 Only).** 0 = Disables RDS (default). 1 = Enables RDS to be transmitted.
1	LMR	**Left Minus Right.** 0 = Disables Left Minus Right. 1 = Enables Left minus Right (Stereo) to be transmitted (default).
0	PILOT	**Pilot Tone.** 0 = Disables Pilot. 1 = Enables the Pilot tone to be transmitted (default).

Property 0x2101. TX_AUDIO_DEVIATION

Sets the transmit audio deviation from 0 to 90 kHz in 10 Hz units. The sum of the audio deviation, pilot deviation and RDS deviation should not exceed regulatory requirements, typically 75 kHz. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 6825, or 68.25 kHz.

Available in: All

Default: 0x1AA9 (6825)

Units: 10 Hz

Step: 10 Hz

Range: 0–9000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXADEV[15:0]															

Bit	Name	Function
15:0	TXADEV[15:0]	**Transmit Audio Frequency Deviation.** Audio frequency deviation is programmable from 0 Hz to 90 kHz in 10 Hz units. Default is 6825 (68.25 kHz). Note that the total deviation of the audio, pilot, and RDS must be less than 75 kHz to meet regulatory requirements.

Property 0x2102. TX_PILOT_DEVIATION

Sets the transmit pilot deviation from 0 to 90 kHz in 10 Hz units. The sum of the audio deviation, pilot deviation and RDS deviation should not exceed regulatory requirements, typically 75 kHz. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 675, or 6.75 kHz.

Available in: All

Default: 0x02A3 (675)

Units: 10 Hz

Step: 10 Hz

Range: 0–9000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXPDEV[15:0]															

Bit	Name	Function
15:0	TXPDEV[15:0]	**Transmit Pilot Frequency Deviation.** Pilot tone frequency deviation is programmable from 0 Hz to 90 kHz in 10 Hz units. Default is 675 (6.75 kHz). Note that the total deviation of the audio, pilot, and RDS must be less than 75 kHz to meet regulatory requirements.

Property 0x2103. TX_RDS_DEVIATION

Sets the RDS deviation from 0 to 7.5 kHz in 10 Hz units. The sum of the audio deviation, pilot deviation and RDS deviation should not exceed regulatory requirements, typically 75 kHz. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 200, or 2 kHz.

Available in: Si4711/13/21

Default: 0x00C8 (200)

Units: 10 Hz

Step: 10 Hz

Range: 0–9000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXRDEV[15:0]															

Bit	Name	Function
15:0	TXRDEV[15:0]	**Transmit RDS Frequency Deviation.** RDS frequency deviation is programmable from 0 Hz to 90 kHz in 10 Hz units. Default is 200 (2 kHz). Note that the total deviation of the audio, pilot, and RDS must be less than 75 kHz to meet regulatory requirements.

Property 0x2104. TX_LINE_INPUT_LEVEL

Sets the input resistance and maximum audio input level for the LIN/RIN pins. An application providing a 150 mV_{PK} input to the device on RIN/LIN would set Line Attenuation = 00, resulting in a maximum permissible input level of 190 mV_{PK} on LIN/RIN and an input resistance of 396 kΩ. The Line Level would be set to 150 mV to correspond to the TX audio deviation level set by the TX_AUDIO_DEVIATION property. An application providing a 1 V_{PK} input to the device on RIN/LIN would set Line Attenuation = 11, resulting in a maximum permissible input level of 636 mV_{PK} on LIN/RIN and an input resistance of 60 kΩ. An external series resistor on LIN and RIN inputs of 40 kΩ would create a resistive voltage divider that would keep the maximum line level on RIN/LIN below 636 mV_{PK}. The Line Level would be set to 636 mV_{PK} to correspond to the TX audio deviation level set by the TX_AUDIO_DEVIATION property. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default input level and peak line level is 636 mV_{PK} with an input impedance of 60 kΩ.

Available in: All

Default: 0x327C

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	LIATTEN[1:0]		0	0	LILEVEL[9:0]									

Bit	Name	Function
15:14	Reserved	Always write to 0.
13:12	LIATTEN[1:0]	**Line Attenuation.** 00 = Max input level = 190 mV_{PK}; input resistance = 396 kΩ 01 = Max input level = 301 mV_{PK}; input resistance = 100 kΩ 10 = Max input level = 416 mV_{PK}; input resistance = 74 kΩ 11 = Max input level = 636 mV_{PK}; input resistance = 60 kΩ (default)
11:10	Reserved	Always write to 0.
9:0	LILEVEL[9:0]	**Line Level.** Maximum line amplitude level on the LIN/RIN pins in mV_{PK}. The default is 0x27C or 636 mV_{PK}.

Property 0x2105. TX_LINE_INPUT_MUTE

Selectively mutes the left and right audio inputs. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode.

Available in: All

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LIMUTE	RIMUTE

Bit	Name	Function
15:2	Reserved	Always write to 0.
1	LIMUTE	Mutes L Line Input. 0 = No mute (default) 1 = Mute
0	RIMUTE	Mutes R Line Input. 0 = No mute (default) 1 = Mute

Property 0x2106. TX_PREEMPHASIS

Sets the transmit pre-emphasis to 50 µs, 75 µs or off. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 75 µs.

Available in: All

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FMPE[1:0]	

Bit	Name	Function
15:2	Reserved	Always write to 0.
1:0	FMPE[1:0]	**FM Pre-Emphasis.** 00 = 75 µs. Used in USA (default) 01 = 50 µs. Used in Europe, Australia, Japan 10 = Disabled 11 = Reserved

Property 0x2107. TX_PILOT_FREQUENCY

This property is used to set the frequency of the stereo pilot in 1 Hz steps. The stereo pilot is nominally set to 19 kHz for stereo operation, however the pilot can be set to any frequency from 0 Hz to 19 kHz to support the generation of an audible test tone. The pilot tone is enabled by setting the PILOT bit (D0) of the TX_COMPONENT_ENABLE property. When using the stereo pilot as an audible test generator it is recommended that the RDS bit (D2) be disabled. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode.

Available in: All

Default: 0x4A38 (19000)

Units: 1 Hz

Step: 1 Hz

Range: 0–19000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	FREQ[15:0]															

Bit	Name	Function
15:0	FREQ	**Stereo Pilot Frequency** Sets the frequency of the stereo pilot in 1 Hz steps. Range 0 Hz–19000 Hz (default is 0x4A38 or 19 kHz).

Property 0x2200. TX_ACOMP_ENABLE

Selectively enables the audio dynamic range control and limiter. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is limiter enabled and audio dynamic range control disabled.

Note: LIMITEN bit is supported in FMTX component 2.0 or later. Reset this bit to 0 in FMTX component 1.0.

Available in: All

Default: 0x0002

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LIMITEN	ACEN

Bit	Name	Function
15:2	Reserved	Always write to 0.
1	LIMITEN	**Audio Limiter.** 0 = Disable 1 = Enable (default)
0	ACEN	**Transmit Audio Dynamic Range Control Enable.** 0 = Audio dynamic range control disabled (default) 1 = Audio dynamic range control enabled

Property 0x2201. TX_ACOMP_THRESHOLD

Sets the threshold for audio dynamic range control from 0 dBFS to –40 dBFS in 1 dB units in 2's complement notation. For example, a setting of –40 dB would be 65536 – 40 = 65496 = 0xFFD8. The threshold is the level below which the device applies the gain set by the TX_ACOMP_GAIN property, and above which the device applies the compression defined by (gain + threshold) / threshold. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 0xFFD8, or –40 dBFS.

Available in: All

Default: 0xFFD8 (–40)

Units: 1 dB

Step: 1 dB

Range: –40 to 0

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	THRESHOLD[15:0]															

Bit	Name	Function
15:0	THRESHOLD[15:0]	**Transmit Audio Dynamic Range Control Threshold.** Range is from –40 to 0 dBFS in 1 dB steps (0xFFD8–0x0). Default is 0xFFD8 (–40 dBFS).

Property 0x2202. TX_ACOMP_ATTACK_TIME

Sets the time required for the device to respond to audio level transitions from below the threshold in the gain region to above the threshold in the compression region. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 0.5 ms, or 0.

Available in: All

Default: 0x0000

Range: 0–9

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	ATTACK[3:0]			

Bit	Name	Function
15:4	Reserved	Always write to 0.
3:0	ATTACK[3:0]	**Transmit Audio Dynamic Range Control Attack Time.** 0 = 0.5 ms (default) 1 = 1.0 ms 2 = 1.5 ms 3 = 2.0 ms 4 = 2.5 ms 5 = 3.0 ms 6 = 3.5 ms 7 = 4.0 ms 8 = 4.5 ms 9 = 5.0 ms

Property 0x2203. TX_ACOMP_RELEASE_TIME

Sets the time required for the device to respond to audio level transitions from above the threshold in the compression region to below the threshold in the gain region. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 1000 ms, or 4.

Available in: All

Default: 0x0004

Range: 0–4

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	RELEASE[2:0]		

Bit	Name	Function
15:3	Reserved	Always write to 0.
2:0	RELEASE[2:0]	**Transmit Audio Dynamic Range Control Release Time.** 0 = 100 ms 1 = 200 ms 2 = 350 ms 3 = 525 ms 4 = 1000 ms (default)

Property 0x2204. TX_ACOMP_GAIN

Sets the gain for audio dynamic range control from 0 to 20 dB in 1 dB units. For example, a setting of 15 dB would be 15 = 0xF. The gain is applied to the audio below the threshold set by the TX_ACOMP_THRESHOLD property. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 15 dB or 0xF.

Available in: All

Default: 0x000F (15)

Units: 1 dB

Step: 1 dB

Range: 0–20

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name											GAIN[5:0]					

Bit	Name	Function
15:6	Reserved	Always write to 0.
5:0	GAIN[5:0]	**Transmit Audio Dynamic Range Control Gain.** Range is from 0 to 20 dB in 1 dB steps. Default is 15.

Property 0x2205. TX_LIMITER_RELEASE_TIME

Sets the time required for the device to respond to audio level transitions from above the limiter threshold to below the limiter threshold. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 5.01 ms, or 102.

Note: TX_LIMITER_RELEASE_TIME is supported in FMTX component 2.0 or later.

Available in: All except Si4710-A10

Default 0x0066 (102)

Step: 1

Range: 5–2000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	LIMITERTC[15:0]															

Bit	Name	Function
15:0	LMITERTC[15:0]	**Sets the limiter release time.** 5 = 102.39 ms 6 = 85.33 ms 7 = 73.14 ms 8 = 63.99 ms 10 = 51.19 ms 13 = 39.38 ms 17 = 30.11 ms 25 = 20.47 ms 51 = 10.03 ms 57 = 8.97 ms 64 = 7.99 ms 73 = 7.01 ms 85 = 6.02 ms 102 = 5.01 ms (default) 127 = 4.02 ms 170 = 3.00 ms 255 = 2.00 ms 510 = 1.00 ms 1000 = 0.50 ms 2000 = 0.25 ms

Property 0x2300. TX_ASQ_INTERRUPT_SELECT

This property is used to enable which Audio Signal Quality (ASQ) measurements trigger ASQ_INT bit in the TX_ASQ_STATUS command. OVERMODIEN bit enables ASQ interrupt by the OVERMOD bit, which turns on with overmodulation of the FM output signal due to excessive input signal level. IALHIEN and IALLIEN bits enable ASQ interrupt by the IALH and IALL bits, which report high or low input audio condition. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode.

Available in: All

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	OVERMODIEN	IALHIEN	IALLIEN

Bit	Name	Function
15:3	Reserved	Always write to 0.
2	OVERMODIEN	**Overmodulation Detection Enable.** 0 = OVERMOD detect disabled (default). 1 = OVERMOD detect enabled.
1	IALHIEN	**Input Audio Level Detection High Threshold Enable.** 0 = IALH detect disabled (default). 1 = IALH detect enabled.
0	IALLIEN	**Input Audio Level Detection Low Threshold Enable.** 0 = IALL detect disabled (default). 1 = IALL detect enabled.

Property 0x2301. TX_ASQ_LEVEL_LOW

This property sets the low audio level threshold relative to 0 dBFS in 1 dB increments, which is used to trigger the IALL bit. This threshold can be set to detect a silence condition in the input audio allowing the host to take an appropriate action such as disabling the RF carrier or powering down the chip. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 0x0000 and the range is 0 to –70.

Available in: All

Default: 0x0000

Units: 1 dB

Step: 1 dB

Range: –70 to 0

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	IALLTH[7:0]							

Bit	Name	Function
15:8	Reserved	Always write to 0.
7:0	IALLTH[7:0]	**Input Audio Level Low Threshold**. Threshold which input audio level must be below in order to detect a low audio condition. Specified in units of dBFS in 1 dB steps (–70 .. 0). Default is 0.

Property 0x2302. TX_ASQ_DURATION_LOW

This property is used to determine the duration (in 1 ms increments) that the input signal must be below the TX_ASQ_LEVEL_LOW threshold in order for an IALL condition to be generated. The range is 0 ms to 65535 ms, and the default is 0 ms. Note that the TX_ASQ_DURATION_LOW and TX_ASQ_DURATION_HIGH counters start and the TX_ASQ_STATUS command will only return valid data after a call to TX_TUNE_FREQ, TX_TUNE_POWER, or TX_TUNE_MEASURE. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode.

Available in: All

Default: 0x0000

Units: 1 ms

Step: 1 ms

Range: 0–65535

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	IALLDUR[15:0]															

Bit	Name	Function
15:0	IALLDUR[15:0]	**Input Audio Level Duration Low.** Required duration the input audio level must fall below IALLTH to trigger an IALL interrupt. Specified in 1mS increments (0–65535 ms). Default is 0.

Property 0x2303. TX_ASQ_LEVEL_HIGH

This property sets the high audio level threshold relative to 0 dBFS in 1 dB increments, which is used to trigger the IALH bit. This threshold can be set to detect an activity condition in the input audio allowing the host to take an appropriate action such as enabling the RF carrier after an extended silent period. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 0x0000 and the range is 0 to –70.

Available in: All

Default: 0x0000

Units: 1 dB

Step: 1 dB

Range: –70 to 0

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	IALHTH[7:0]							

Bit	Name	Function
15:8	Reserved	Always write to 0.
7:0	IALHTH[7:0]	**Input Audio Level High Threshold** Threshold which input audio level must be above in order to detect a high audio condition. Specified in units of dBFS in 1 dB steps (–70 .. 0). Default is 0.

Property 0x2304. TX_ASQ_DURATION_HIGH

This property is used to determine the duration (in 1 ms increments) that the input signal must be above the TX_ASQ_LEVEL_HIGH threshold in order for a IALH condition to be generated. The range is 0 to 65535 ms, and the default is 0 ms. Note that the TX_ASQ_DURATION_LOW and TX_ASQ_DURATION_HIGH counters start and the TX_ASQ_STATUS command will only return valid data after a call to TX_TUNE_FREQ, TX_TUNE_POWER, or TX_TUNE_MEASURE. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode.

Available in: All

Default: 0x0000

Units: 1 ms

Step: 1 ms

Range: 0–65535

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	IALHDUR[15:0]															

Bit	Name	Function
15:0	IALHDUR[15:0]	**Input Audio Level Duration High.** Required duration the input audio level must exceed IALHTH to trigger an IALH interrupt. Specified in 1 ms increments (0 – 65535 ms). Default is 0.

Property 0x2C00. TX_RDS_INTERRUPT_SOURCE

Configures the RDS interrupt sources. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode.

Note: TX_RDS_INTERRUPT_SOURCE is supported in FMTX component 2.0 or later.

Available in: Si4711/13/21

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	RDS PSXMIT	RDS CBUFXMIT	RDS-FIFOXMIT	RDS CBUFWRAP	RDS-FIFOMT

Bit	Name	Function
4	RDSPSXMIT	0 = Do not interrupt (default). 1 = Interrupt when a RDS PS Group has been transmitted. The interrupt occurs when a PS group begins transmission.
3	RDSCBUFXMIT	0 = Do not interrupt (default). 1 = Interrupt when a RDS Group has been transmitted from the Circular Buffer. The interrupt occurs when a group is fetched from the buffer.
2	RDSFIFOXMIT	0 = Do not interrupt (default). 1 = Interrupt when a RDS Group has been transmitted from the FIFO Buffer. The interrupt occurs when a group is fetched from the buffer.
1	RDSCBUFWRAP	0 = Do not interrupt (default). 1 = Interrupt when the RDS Group Circular Buffer has wrapped. The interrupt occurs when the last group is fetched from the buffer.
0	RDSFIFOMT	0 = Do not interrupt (default). 1 = Interrupt when the RDS Group FIFO Buffer is empty. The interrupt occurs when the last group is fetched from the FIFO.

Property 0x2C01. TX_RDS_PI

Sets the RDS PI code to be transmitted in block A and block C (for type B groups). The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode.

Note: TX_RDS_PI is supported in FMTX component 2.0 or later.

Available in: Si4711/13/21

Default: 0x40A7

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDSPI[15:0]															

Bit	Name	Function
15:0	RDSPI[15:0]	**Transmit RDS Program Identifier.** RDS program identifier data.

Property 0x2C02. TX_RDS_PS_MIX

Sets the ratio of RDS PS (group 0A) and circular buffer/FIFO groups. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode.

Note: TX_RDS_PS_MIX is supported in FMTX component 2.0 or later.

Available in: Si4711/13/21

Default: 0x0003

Range: 0–6

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	RDSPSMIX[2:0]		

Bit	Name	Function
15:3	Reserved	Always write to 0.
2:0	RDSPSMIX[2:0]	**Transmit RDS Mix.** 000 = Only send RDS PS if RDS Group Buffer is empty 001 = Send RDS PS 12.5% of the time 010 = Send RDS PS 25% of the time 011 = Send RDS PS 50% of the time (default) 100 = Send RDS PS 75% of the time 101 = Send RDS PS 87.5% of the time 110 = Send RDS PS 100% of the time

Property 0x2C03. TX_RDS_PS_MISC

Configures miscellaneous RDS flags. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode.

Note: TX_RDS_PS_MISC is supported in FMTX component 2.0 or later.

Available in: Si4711/13/21

Default: 0x1008

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDSD3	RDSD2	RDSD1	RDSD0	FORCEB	RDSTP	RDSPTY[4:0]					RDSTA	RDSMS	0	0	0

Bit	Name	Function
15	RDSD3	**Dynamic PTY code.** 0 = Static PTY (default). 1 = Indicates that the PTY code is dynamically switched.
14	RDSD2	**Compressed code.** 0 = Not compressed (default). 1 = Compressed.
13	RDSD1	**Artificial Head code.** 0 = Not artificial head (default). 1 = Artificial head.
12	RDSD0	**Mono/Stereo code.** 0 = Mono. 1 = Stereo (default).
11	FORCEB	**Use the PTY and TP set here in all block B data.** 0 = FIFO and BUFFER use PTY and TP as when written (default). 1 = FIFO and BUFFER force PTY and TP to be the settings in this property.
10	RDSTP	**Traffic Program Code (default = 0).**
9:5	RDSPTY[4:0]	**Program Type Code (default = 0).**
4	RDSTA	**Traffic Announcement Code (default = 0).**
3	RDSMS	**Music/Speech Switch Code.** 0 = Speech. 1 = Music (default).
2:0	Reserved	Always write to 0.

Property 0x2C04. TX_RDS_PS_REPEAT_COUNT

Sets the number of times a program service group 0A is repeated. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode.

Note: TX_RDS_PS_REPEAT_COUNT is supported in FMTX component 2.0 or later.

Available in: Si4711/13/21

Default: 0x0003

Range: 1–255

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	RDSPSRC[7:0]							

Bit	Name	Function
15:8	Reserved	Always write to 0.
7:0	RDSPSRC[7:0]	**Transmit RDS PS Repeat Count.** Number of times to repeat transmission of a PS message before transmitting the next PS message.

Property 0x2C05. TX_RDS_PS_MESSAGE_COUNT

Sets the number of program service messages through which to cycle. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode.

Note: TX_RDS_PS_MESSAGE_COUNT is supported in FMTX component 2.0 or later.

Available in: Si4711/13/21

Default: 0x0001

Range 1–12

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	RDSPSMC[3:0]			

Bit	Name	Function
15:4	Reserved	Always write to 0.
3:0	RDSPSMC[3:0]	**Transmit RDS PS Message Count.** Number of PS messages to cycle through. Default is 1.

Property 0x2C06. TX_RDS_PS_AF

Sets the AF RDS Program Service Alternate Frequency. This provides the ability to inform the receiver of a single alternate frequency using AF Method A coding and is transmitted along with the RDS_PS Groups. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode.

Note: TX_RDS_PS_AF is supported in FMTX component 2.0 or later.

Available in: Si4711/13/21

Default: 0xE0E0

Range: 0xE000–0xE0CC

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDSAF[15:0]															

Bit	Name	Function
15:0	RDSAF[15:0]	**Transmit RDS Program Service Alternate Frequency.** 0xE101 = 1 AF @ 87.6 MHz 0xE102 = 1 AF @ 87.7 MHz ... 0xE1CB = 1 AF @ 107.8 MHz 0xE1CC = 1 AF @ 107.9 MHz 0xE0E0 = No AF exists (default)

Property 0x2C07. TX_RDS_FIFO_SIZE

Sets the RDS FIFO size in number of blocks. Note that the value written must be one larger than the desired FIFO size. The number of blocks allocated will reduce the size of the Circular RDS Group Buffer by the same amount. For instance, if RDSFIFOSZ = 20, then the RDS Circular Buffer will be reduced by 20 blocks. The minimum number of blocks which should be allocated is 4. This provides enough room for a single group of any type (xA or xB) to be transmitted. Groups xA require 3 Blocks, Groups xB require 2 Blocks as block C' is always the same as the RDS PI code. Before setting this value, determine the available blocks through the TX_RDS_FIFO command, as the buffer size may vary between versions or part numbers. The guaranteed minimum FIFO size, however, is 53 blocks. The RDS FIFO and the RDS Circular Buffer should be emptied with the TX_RDS_FIFO command prior to changing the size of the FIFO. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode.

Note: TX_RDS_FIFO_SIZE is supported in FMTX component 2.0 or later.

Available in: Si4711/13/21

Default: 0x0000

Units: blocks

Step: 3 blocks

Range: 0, 4, 7, 10–54

Note: Actual maximum FIFO size returned by the TX_RDS_BUFF command is larger, however, this is 53 blocks is the guaranteed FIFO size.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	RDSFIFOSZ[7:0]							

Bit	Name	Function
15:8	Reserved	Always write 0.
7:0	RDSFIFOSZ[7:0]	**Transmit RDS FIFO Size.** 0 = FIFO disabled (default)

5.2. Commands and Properties for the FM/RDS Receiver (Si4704/05/06/2x/3x/4x/84/85)

Tables 8 and 9 summarize the commands and properties for the FM/RDS Receiver component applicable to Si4704/05/06/2x/3x/4x/84/85.

Table 8. FM/RDS Receiver Command Summary

Cmd	Name	Description	Available In
0x01	POWER_UP	Power up device and mode selection.	All
0x10	GET_REV	Returns revision information on the device.	All
0x11	POWER_DOWN	Power down device.	All
0x12	SET_PROPERTY	Sets the value of a property.	All
0x13	GET_PROPERTY	Retrieves a property's value.	All
0x14	GET_INT_STATUS	Reads interrupt status bits.	All
0x15	PATCH_ARGS*	Reserved command used for patch file downloads.	All
0x16	PATCH_DATA*	Reserved command used for patch file downloads.	All
0x20	FM_TUNE_FREQ	Selects the FM tuning frequency.	All
0x21	FM_SEEK_START	Begins searching for a valid frequency.	All
0x22	FM_TUNE_STATUS	Queries the status of previous FM_TUNE_FREQ or FM_SEEK_START command.	All
0x23	FM_RSQ_STATUS	Queries the status of the Received Signal Quality (RSQ) of the current channel.	All
0x24	FM_RDS_STATUS	Returns RDS information for current channel and reads an entry from RDS FIFO.	Si4705/06, Si4721, Si474x, Si4731/32/35/37/39, Si4785
0x27	FM_AGC_STATUS	Queries the current AGC settings	All
0x28	FM_AGC_OVERRIDE	Override AGC setting by disabling and forcing it to a fixed value	All
0x80	GPIO_CTL	Configures GPO1, 2, and 3 as output or Hi-Z.	All except Si4730-A10
0x81	GPIO_SET	Sets GPO1, 2, and 3 output level (low or high).	All except Si4730-A10

***Note:** Commands PATCH_ARGS and PATCH_DATA are only used to patch firmware. For information on applying a patch file, see "7.2. Powerup from a Component Patch" on page 233.

Table 9. FM/RDS Receiver Property Summary

Prop	Name	Description	Default	Available In
0x0001	GPO_IEN	Enables interrupt sources.	0x0000	All
0x0102	DIGITAL_OUTPUT_FORMAT	Configure digital audio outputs.	0x0000	Si4704-D60 and later, Si4705/06, Si4721/31/32/35/37/39, Si4730/34/36/38-D60 and later, Si4741/43/45, Si4784/85
0x0104	DIGITAL_OUTPUT_SAMPLE_RATE	Configure digital audio output sample rate.	0x0000	Si4704-D60 and later, Si4705/06, Si4721/31/32/35/37/39, Si4730/34/36/38-D60 and later, Si4741/43/45, Si4784/85
0x0201	REFCLK_FREQ	Sets frequency of reference clock in Hz. The range is 31130 to 34406 Hz, or 0 to disable the AFC. Default is 32768 Hz.	0x8000	All
0x0202	REFCLK_PRESCALE	Sets the prescaler value for RCLK input.	0x0001	All
0x1100	FM_DEEMPHASIS	Sets deemphasis time constant. Default is 75 µs.	0x0002	All except Si4749
0x1102	FM_CHANNEL_FILTER	Selects bandwidth of channel filter applied at the demodulation stage.	0x0001	Si4706, Si4749, Si4705/31/35/85-D50, and later, Si4732
			0x0000	Si4704/30/34/84-D50 and later
0x1105	FM_BLEND_STEREO_THRESHOLD	Selects bandwidth of channel filter applied at the demodulation stage.	0x0031	Si470x/2x, Si473x-C40 and earlier
0x1106	FM_BLEND_MONO_THRESHOLD	Sets RSSI threshold for mono blend (Full mono below threshold, blend above threshold). To force stereo set this to 0. To force mono set this to 127. Default value is 30 dBµV.	0x001E	Si470x/2x, Si473x-C40 and earlier
0x1107	FM_ANTENNA_INPUT	Selects the antenna type and the pin to which it is connected.	0x0000	Si4704/05/06/20/21

Table 9. FM/RDS Receiver Property Summary (Continued)

Prop	Name	Description	Default	Available In
0x1108	FM_MAX_TUNE_ ERROR	Sets the maximum freq error allowed before setting the AFC rail (AFCRL) indicator. Default value is 20 kHz.	0x001E	All
			0x0014	All others
0x1200	FM_RSQ_INT_ SOURCE	Configures interrupt related to Received Signal Quality metrics.	0x0000	All
0x1201	FM_RSQ_SNR_HI_ THRESHOLD	Sets high threshold for SNR interrupt.	0x007F	All
0x1202	FM_RSQ_SNR_LO_ THRESHOLD	Sets low threshold for SNR interrupt.	0x0000	All
0x1203	FM_RSQ_RSSI_HI_ THRESHOLD	Sets high threshold for RSSI interrupt.	0x007F	All
0x1204	FM_RSQ_RSSI_LO_ THRESHOLD	Sets low threshold for RSSI interrupt.	0x0000	All
0x1205	FM_RSQ_MULTIPATH_HI_ THRESHOLD	Sets high threshold for multipath interrupt.	0x007F	Si4706-C30 and later, Si474x, Si4704/05/30/31/34/35/84/85 -D50, and later, Si4732
0x1206	FM_RSQ_MULTIPATH_ LO_THRESHOLD	Sets low threshold for multipath interrupt.	0x0000	Si4706-C30 and later, Si474x, Si4704/05/30/31/34/35/84/85 -D50, and later, Si4732
0x1207	FM_RSQ_BLEND_ THRESHOLD	Sets the blend threshold for blend interrupt when boundary is crossed.	0x0081	All except Si4749
0x1300	FM_SOFT_MUTE_RATE	Sets the attack and decay rates when entering and leaving soft mute.	0x0040	Si4706/07/20/21/84/85-B20 and earlier, Si4704/05/3x-C40 and earlier
0x1301	FM_SOFT_MUTE_SLOPE	Configures attenuation slope during soft mute in dB attenuation per dB SNR below the soft mute SNR threshold. Default value is 2.	0x0002	Si4704/05/06/3x-C40 and later, Si4732, Si4740/41/42/43/44/45
0x1302	FM_SOFT_MUTE_ MAX_ATTENUATION	Sets maximum attenuation during soft mute (dB). Set to 0 to disable soft mute. Default is 16 dB.	0x0010	All except Si4749
0x1303	FM_SOFT_MUTE_ SNR_THRESHOLD	Sets SNR threshold to engage soft mute. Default is 4 dB.	0x0004	All except Si4749

Table 9. FM/RDS Receiver Property Summary (Continued)

Prop	Name	Description	Default	Available In
0x1304	FM_SOFT_MUTE_ RELEASE_RATE	Sets soft mute release rate. Smaller values provide slower release, and larger values provide faster release. The default is 8192 (approximately 8000 dB/s)	0x2000	Si4706-C30 and later, Si4740/41/42/43/44/45, Si4704/05/30/31/34/35/84/85 -D50 and later, Si4732
0x1305	FM_SOFT_MUTE_ ATTACK_RATE	Sets soft mute attack rate. Smaller values provide slower attack, and larger values provide faster attack. The default is 8192 (approximately 8000 dB/s)	0x2000	Si4706-C30 and later, Si4740/41/42/43/44/45, Si4704/05/30/31/34/35/84/85 -D50 and later, Si4732
0x1400	FM_SEEK_BAND_ BOTTOM	Sets the bottom of the FM band for seek. Default is 8750 (87.5 MHz).	0x222E	All
0x1401	FM_SEEK_BAND_TOP	Sets the top of the FM band for seek. Default is 10790 (107.9 MHz).	0x2A26	All
0x1402	FM_SEEK_FREQ_ SPACING	Selects frequency spacing for FM seek. Default value is 10 (100 kHz).	0x000A	All
0x1403	FM_SEEK_TUNE_ SNR_THRESHOLD	Sets the SNR threshold for a valid FM Seek/Tune. Default value is 3 dB.	0x0003	All
0x1404	FM_SEEK_TUNE_ RSSI_TRESHOLD	Sets the RSSI threshold for a valid FM Seek/Tune. Default value is 20 dBµV.	0x0014	All
0x1500	FM_RDS_INT_SOURCE	Configures RDS interrupt behavior.	0x0000	Si4705/06, Si4721, Si431/32/35/37/39, Si4741/43/45/49
0x1501	FM_RDS_INT_FIFO_ COUNT	Sets the minimum number of RDS groups stored in the receive FIFO required before RDSRECV is set.	0x0000	Si4705/06, Si4721, Si431/32/35/37/39, Si4741/43/45/49
0x1502	FM_RDS_CONFIG	Configures RDS setting.	0x0000	Si4705/06, Si4721, Si431/32/35/37/39, Si4741/43/45/49
0x1503	FM_RDS_CONFIDENCE	Sets the confidence level threshold for each RDS block.	0x1111	Si4706-C30 and later, Si474x, Si4704/05/30/31/34/35/84/85 -D50 and later, Si4732

Table 9. FM/RDS Receiver Property Summary (Continued)

Prop	Name	Description	Default	Available In
0x1700	FM_AGC_ATTACK_RATE	Sets the AGC attack rate. Larger values provide slower attack and smaller values provide faster attack. The default is 4 (approximately 1500 dB/s).	0x0004	Si474x
0x1701	FM_AGC_RE-LEASE_RATE	Sets the AGC release rate. Larger values provide slower release and smaller values provide faster release. The default is 140 (approximately 43 dB/s).	0x008C	Si474x
0x1800	FM_BLEND_RSSI_ STEREO_THRESHOLD	Sets RSSI threshold for stereo blend. (Full stereo above threshold, blend below threshold.) To force stereo, set this to 0. To force mono, set this to 127. Default value is 49 dBµV.	0x0031	Si4706-C30 and later, Si4740/41/42/43/44/45, Si4705/31/35/85-D50 and later, Si4732
0x1801	FM_BLEND_RSSI_-MONO_ THRESHOLD	Sets RSSI threshold for mono blend (Full mono below threshold, blend above threshold). To force stereo, set this to 0. To force mono, set this to 127. Default value is 30 dBµV.	0x001E	Si4706-C30 and later, Si4740/41/42/43/44/45, Si4705/31/35/85 -D50 and later, Si4732
0x1802	FM_BLEND_RSSI_ ATTACK_RATE	Sets the stereo to mono attack rate for RSSI based blend. Smaller values provide slower attack and larger values provide faster attack. The default is 4000 (approximately 16 ms).	0x0FA0	Si4706-C30 and later, Si4740/41/42/43/44/45, Si4705/31/35/85 -D50 and later, Si4732
0x1803	FM_BLEND_RSSI_ RELEASE_RATE	Sets the mono to stereo release rate for RSSI based blend. Smaller values provide slower release and larger values provide faster release. The default is 400 (approximately 164 ms).	0x0190	Si4706-C30 and later, Si4740/41/42/43/44/45, Si4705/31/35/85 -D50 and later, Si4732
0x1804	FM_BLEND_SNR_ STEREO_THRESHOLD	Sets SNR threshold for stereo blend (Full stereo above threshold, blend below threshold). To force stereo, set this to 0. To force mono, set this to 127. Default value is 27 dB.	0x001B	Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732

Table 9. FM/RDS Receiver Property Summary (Continued)

Prop	Name	Description	Default	Available In
0x1805	FM_BLEND_SNR_MONO_THRESHOLD	Sets SNR threshold for mono blend (Full mono below threshold, blend above threshold). To force stereo, set this to 0. To force mono, set this to 127. Default value is 14 dB.	0x000E	Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732
0x1806	FM_BLEND_SNR_ATTACK_RATE	Sets the stereo to mono attack rate for SNR based blend. Smaller values provide slower attack and larger values provide faster attack. The default is 4000 (approximately 16 ms).	0x0FA0	Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732
0x1807	FM_BLEND_SNR_RELEASE_RATE	Sets the mono to stereo release rate for SNR based blend. Smaller values provide slower release and larger values provide faster release. The default is 400 (approximately 164 ms).	0x0190	Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732
0x1808	FM_BLEND_MULTIPATH_STEREO_THRESHOLD	Sets multipath threshold for stereo blend (Full stereo below threshold, blend above threshold). To force stereo, set this to 100. To force mono, set this to 0. Default value is 20.	0x0014	Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732
0x1809	FM_BLEND_MULTIPATH_MONO_THRESHOLD	Sets Multipath threshold for mono blend (Full mono above threshold, blend below threshold). To force stereo, set to 100. To force mono, set to 0. The default is 60.	0x003C	Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732

Table 9. FM/RDS Receiver Property Summary (Continued)

Prop	Name	Description	Default	Available In
0x180A	FM_BLEND_MULTIPATH_ ATTACK_RATE	Sets the stereo to mono attack rate for Multipath based blend. Smaller values provide slower attack and larger values provide faster attack. The default is 4000 (approximately 16 ms).	0x0FA0	Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732
0x180B	FM_BLEND_MULTIPATH_ RELEASE_RATE	Sets the mono to stereo release rate for Multipath based blend. Smaller values provide slower release and larger values provide faster release. The default is 40 (approximately 1.64 s).	0x0028	Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732
0x180C	FM_BLEND_MAX_STE-REO_SEPARATION	Sets the maximum amount of stereo separation	0x0000	Si474x
0x1900	FM_NB_DETECT_ THRESHOLD	Sets the threshold for detecting impulses in dB above the noise floor. Default value is 16.	0x0010	Si4742/43/44/45
0x1901	FM_NB_INTERVAL	Interval in micro-seconds that original samples are replaced by interpolated clean samples. Default value is 24 µs.	0x0018	Si4742/43/44/45
0x1902	FM_NB_RATE	Noise blanking rate in 100 Hz units. Default value is 64.	0x0040	Si4742/43/44/45
0x1903	FM_NB_IIR_FILTER	Sets the bandwidth of the noise floor estimator Default value is 300.	0x012C	Si4742/43/44/45
0x1904	FM_NB_DELAY	Delay in micro-seconds before applying impulse blanking to the original samples. Default value is 133.	0x00AA	Si4742/43/44/45
0x1A00	FM_HICUT_ SNR_HIGH_ THRESHOLD	Sets the SNR level at which hi-cut begins to band limit. Default value is 24.	0x0018	Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732
0x1A01	FM_HICUT_ SNR_LOW_-THRESHOLD	Sets the SNR level at which hi-cut reaches maximum band limiting. Default value is 15.	0x000F	Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732

Table 9. FM/RDS Receiver Property Summary (Continued)

Prop	Name	Description	Default	Available In
0x1A02	FM_HICUT_ ATTACK_RATE	Sets the rate at which hi-cut lowers the cut-off frequency. Default value is 20000 (approximately 3 ms)	0x4E20	Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732
0x1A03	FM_HICUT_ RELEASE_RATE	Sets the rate at which hi-cut increases the cut-off frequency. Default value is 20. (approximately 3.3 s)	0x0014	Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732
0x1A04	FM_HICUT_ MULTIPATH_TRIGGER THRESHOLD	Sets the MULTIPATH level at which hi-cut begins to band limit. Default value is 20.	0x0014	Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732
0x1A05	FM_HICUT_ MULTIPATH_END_ THRESHOLD	Sets the MULTIPATH level at which hi-cut reaches maximum band limiting. Default value is 60.	0x003C	Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732
0x1A06	FM_HICUT_ CUTOFF_FREQUENCY	Sets the maximum band limit frequency for hi-cut and also sets the maximum audio frequency. Default value is 0 (disabled).	0x0000	Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732
0x4000	RX_VOLUME	Sets the output volume.	0x003F	All except Si4749
0x4001	RX_HARD_MUTE	Mutes the audio output. L and R audio outputs may be muted independently.	0x0000	All except Si4749

Table 10. Status Response for the FM/RDS Receiver

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	RDSINT	X	STCINT

Bit	Name	Function
7	CTS	**Clear to Send.** 0 = Wait before sending next command. 1 = Clear to send next command.
6	ERR	**Error**. 0 = No error 1 = Error
5:4	Reserved	Values may vary.
3	RSQINT	**Received Signal Quality Interrupt.** 0 = Received Signal Quality measurement has not been triggered. 1 = Received Signal Quality measurement has been triggered.
2	RDSINT	**Radio Data System (RDS) Interrupt (Si4705/21/31/32/35/37/39/85 Only).** 0 = Radio data system interrupt has not been triggered. 1 = Radio data system interrupt has been triggered.
1	Reserved	Values may vary.
0	STCINT	**Seek/Tune Complete Interrupt.** 0 = Tune complete has not been triggered. 1 = Tune complete has been triggered.

5.2.1. FM/RDS Receiver Commands

Command 0x01. POWER_UP

Initiates the boot process to move the device from powerdown to powerup mode. The boot can occur from internal device memory or a system controller downloaded patch. To confirm that the patch is compatible with the internal device library revision, the library revision should be confirmed by issuing the POWER_UP command with FUNC = 15 (query library ID). The device returns the response, including the library revision, and then moves into powerdown mode. The device can then be placed in powerup mode by issuing the POWER_UP command with FUNC = 0 (FM Receive) and the patch may be applied (See Section "7.2. Powerup from a Component Patch" on page 233).

The POWER_UP command configures the state of ROUT (pin 13, Si474x pin 15, Si4732 pin 16) and LOUT (pin 14, Si474x pin 16, Si4732 pin 1) for analog audio mode and GPO2/INT (pin 18, Si474x pin 20, Si4732 pin 3) for interrupt operation. For the Si4705/21/31/32/35/37/39/84/85-B20, the POWER_UP command also configures the state of GPO3/DCLK (pin 17, Si474x pin 19, Si4732 pin 2), DFS (pin 16, Si474x pin 18, Si4732 pin 1), and DOUT (pin 15, Si474x pin 17, Si4732 pin 16) for digital audio mode. The command configures GPO2/INT interrupts (GPO2OEN) and CTS interrupts (CTSIEN). If both are enabled, GPO2/INT is driven high during normal operation and low for a minimum of 1 µs during the interrupt. The CTSIEN bit is duplicated in the GPO_IEN property. The command is complete when the CTS bit (and optional interrupt) is set.

Note: To change function (e.g. FM RX to AM RX or FM RX to FM TX), issue POWER_DOWN command to stop current function; then, issue POWER_UP to start new function.

Note: Delay at least 500 ms between powerup command and first tune command to wait for the oscillator to stabilize if XOSCEN is set and crystal is used as the RCLK.

Available in: All

Command Arguments: Two

Response Bytes: None (FUNC = 0), Seven (FUNC = 15)

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	0	0	0	0	1
ARG1	CTSIEN	GPO2OEN	PATCH	XOSCEN	FUNC[3:0]			
ARG2	OPMODE[7:0]							

ARG	Bit	Name	Function
1	7	CTSIEN	**CTS Interrupt Enable.** 0 = CTS interrupt disabled. 1 = CTS interrupt enabled.
1	6	GPO2OEN	**GPO2 Output Enable.** 0 = GPO2 output disabled. 1 = GPO2 output enabled.
1	5	PATCH	**Patch Enable.** 0 = Boot normally. 1 = Copy NVM to RAM, but do not boot. After CTS has been set, RAM may be patched.

ARG	Bit	Name	Function
1	4	XOSCEN	**Crystal Oscillator Enable.** **Note:** Set to 0 for Si4740/41/42/43/44/45/49 0 = Use external RCLK (crystal oscillator disabled). 1 = Use crystal oscillator (RCLK and GPO3/DCLK with external 32.768 kHz crystal and OPMODE=00000101). See Si47xx Data Sheet Application Schematic for external BOM details.
1	3:0	FUNC[3:0]	**Function.** 0 = FM Receive. 1–14 = Reserved. 15 = Query Library ID.
2	7:0	OPMODE[7:0]	**Application Setting.** 00000000 = RDS output only (no audio outputs) Si4749 only 00000101 = Analog audio outputs (LOUT/ROUT). 00001011 = Digital audio output (DCLK, LOUT/DFS, ROUT/DIO) (Si4704/05/21/31/35/37/39/41/43/45/84/85 FMRX component 2.0 or later with XOSCEN = 0) 10110000 = Digital audio outputs (DCLK, DFS, DIO) (Si4704/05/21/31/35/37/39/41/43/45/84/85 FMRX component 2.0 or later with XOSCEN = 0). 10110101 = Analog and digital audio outputs (LOUT/ROUT and DCLK, DFS, DIO) (Si4704/05/21/31/35/37/39/41/43/45/84/85 FMRX component 2.0 or later with XOSCEN = 0).

Response (FUNC = 0, FM Receive)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	RDSINT	X	STCINT

Response (FUNC = 15, Query Library ID)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	RDSINT	X	STCINT
RESP1	PN[7:0]							
RESP2	FWMAJOR[7:0]							
RESP3	FWMINOR[7:0]							
RESP4	RESERVED[7:0]							
RESP5	RESERVED[7:0]							
RESP6	CHIPREV[7:0]							
RESP7	LIBRARYID[7:0]							

RESP	Bit	Name	Function
1	7:0	PN[7:0]	**Final 2 digits of part number (HEX).**

2	7:0	FWMAJOR[7:0]	**Firmware Major Revision (ASCII).**
3	7:0	FWMINOR[7:0]	**Firmware Minor Revision (ASCII).**
4	7:0	RESERVED[7:0]	**Reserved, various values.**
5	7:0	RESERVED[7:0]	**Reserved, various values.**
6	7:0	CHIPREV[7:0]	**Chip Revision (ASCII).**
7	7:0	LIBRARYID[7:0]	**Library Revision (HEX).**

Command 0x10. GET_REV

Returns the part number, chip revision, firmware revision, patch revision and component revision numbers. The command is complete when the CTS bit (and optional interrupt) is set. This command may only be sent when in powerup mode.

Available in: All

Command arguments: None

Response bytes: Fifteen (Si4705/06 only), Eight (Si4704/2x/3x/4x)

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	0	0

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	RDSINT	X	STCINT
RESP1	PN[7:0]							
RESP2	FWMAJOR[7:0]							
RESP3	FWMINOR[7:0]							
RESP4	$PATCH_H$[7:0]							
RESP5	$PATCH_L$[7:0]							
RESP6	CMPMAJOR[7:0]							
RESP7	CMPMINOR[7:0]							
RESP8	CHIPREV[7:0]							
RESP10	Reserved							
RESP11	Reserved							
RESP12	Reserved							
RESP13	Reserved							
RESP14	Reserved							
RESP15	CID[7:0] (Si4705 only)							

RESP	Bit	Name	Function
1	7:0	PN[7:0]	**Final 2 digits of Part Number (HEX).**
2	7:0	FWMAJOR[7:0]	**Firmware Major Revision (ASCII).**
3	7:0	FWMINOR[7:0]	**Firmware Minor Revision (ASCII).**
4	7:0	$PATCH_H$[7:0]	**Patch ID High Byte (HEX).**
5	7:0	$PATCH_L$[7:0]	**Patch ID Low Byte (HEX).**
6	7:0	CMPMAJOR[7:0]	**Component Major Revision (ASCII).**
7	7:0	CMPMINOR[7:0]	**Component Minor Revision (ASCII).**
8	7:0	CHIPREV[7:0]	**Chip Revision (ASCII).**
15	7:0	CID[7:0]	**CID (Si4705/06 only).**

Command 0x11. POWER_DOWN

Moves the device from powerup to powerdown mode. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode. Note that only the POWER_UP command is accepted in powerdown mode. **If the system controller writes a command other than POWER_UP when in powerdown mode, the device does not respond. The device will only respond when a POWER_UP command is written. GPO pins are powered down and not active during this state. For optimal power down current, GPO2 must be either internally driven low through GPIO_CTL command or externally driven low.**

Note: In FMRX component 1.0, a reset is required when the system controller writes a command other than POWER_UP when in powerdown mode.

Note: The following describes the state of all the pins when in powerdown mode:

GPIO1, GPIO2, and GPIO3 = 0

ROUT, LOUT, DOUT, DFS = HiZ

Available in: All

Command arguments: None

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	0	1

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	RDSINT	X	STCINT

Command 0x12. SET_PROPERTY

Sets a property shown in Table 9, “FM/RDS Receiver Property Summary,” on page 56. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode. See Figure 30, “CTS and SET_PROPERTY Command Complete tCOMP Timing Model,” on page 243 and Table 50, “Command Timing Parameters for the FM Receiver,” on page 245.

Available in: All

Command Arguments: Five

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	1	0
ARG1	0	0	0	0	0	0	0	0
ARG2	$PROP_H$[7:0]							
ARG3	$PROP_L$[7:0]							
ARG4	$PROPD_H$[7:0]							
ARG5	$PROPD_L$[7:0]							

ARG	Bit	Name	Function
1	7:0	Reserved	Always write to 0.
2	7:0	$PROP_H$[7:0]	**Property High Byte.** This byte in combination with $PROP_L$ is used to specify the property to modify.
3	7:0	$PROP_L$[7:0]	**Property Low Byte.** This byte in combination with $PROP_H$ is used to specify the property to modify.
4	7:0	$PROPD_H$[7:0]	**Property Value High Byte.** This byte in combination with $PROPD_L$ is used to set the property value.
5	7:0	$PROPD_L$[7:0]	**Property Value Low Byte.** This byte in combination with $PROPD_H$ is used to set the property value.

Command 0x13. GET_PROPERTY

Gets a property as shown in Table 9, “FM/RDS Receiver Property Summary,” on page 56. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode.

Available in: All

Command arguments: Three

Response bytes: Three

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	1	1
ARG1	0	0	0	0	0	0	0	0
ARG2	$PROP_H[7:0]$							
ARG3	$PROP_L[7:0]$							

ARG	Bit	Name	Function
1	7:0	Reserved	Always write to 0.
2	7:0	$PROP_H[7:0]$	**Property High Byte.** This byte in combination with $PROP_L$ is used to specify the property to get.
3	7:0	$PROP_L[7:0]$	**Property Low Byte.** This byte in combination with $PROP_H$ is used to specify the property to get.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	RDSINT	X	STCINT
RESP1	0	0	0	0	0	0	0	0
RESP2	$PROPD_H[7:0]$							
RESP3	$PROPD_L[7:0]$							

RESP	Bit	Name	Function
1	7:0	Reserved	Always returns 0.
2	7:0	$PROPD_H[7:0]$	**Property Value High Byte.** This byte in combination with $PROPD_L$ represents the requested property value.
3	7:0	$PROPD_L[7:0]$	**Property Value High Byte.** This byte in combination with $PROPD_H$ represents the requested property value.

Command 0x14. GET_INT_STATUS

Updates bits 6:0 of the status byte. This command should be called after any command that sets the STCINT, RDSINT, or RSQINT bits. When polling this command should be periodically called to monitor the STATUS byte, and when using interrupts, this command should be called after the interrupt is set to update the STATUS byte. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be set when in powerup mode.

Available in: All

Command arguments: None

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	1	0	0

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	RDSINT	X	STCINT

Command 0x20. FM_TUNE_FREQ

Sets the FM Receive to tune a frequency between 64 and 108 MHz in 10 kHz units. The CTS bit (and optional interrupt) is set when it is safe to send the next command. The ERR bit (and optional interrupt) is set if an invalid argument is sent. Note that only a single interrupt occurs if both the CTS and ERR bits are set. The optional STC interrupt is set when the command completes. The STCINT bit is set only after the GET_INT_STATUS command is called. This command may only be sent when in powerup mode. The command clears the STC bit if it is already set. See Figure 29, “CTS and STC Timing Model,” on page 243 and Table 50, “Command Timing Parameters for the FM Receiver,” on page 245.

FM: LO frequency is 128 kHz above RF for RF frequencies $\leq$ 90 MHz and 128 kHz below RF for RF frequencies > 90 MHz. For example, LO frequency is 80.128 MHz when tuning to 80.00 MHz.

Note: For FMRX components 2.0 or earlier, tuning range is 76–108 MHz.

Note: Fast bit is supported in FMRX components 4.0 or later.

Note: Freeze bit is supported in FMRX components 4.0 or later.

Available in: All

Command arguments: Four

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	1	0	0	0	0	0
ARG1	0	0	0	0	0	0	FREEZE	FAST
ARG2	$FREQ_H$[7:0]							
ARG3	$FREQ_L$[7:0]							
ARG4	ANTCAP[7:0]							

ARG	Bit	Name	Function
1	7:1	Reserved	Always write to 0.
1	1	FREEZE	**Freeze Metrics During Alternate Frequency Jump.** If set will cause the blend, hicut, and softmute to transition as a function of the associated attack/release parameters rather than instantaneously when tuning to alternate station.
1	0	FAST	**FAST Tuning.** If set, executes fast and invalidated tune. The tune status will not be accurate.
2	7:0	$FREQ_H$[7:0]	**Tune Frequency High Byte.** This byte in combination with $FREQ_L$ selects the tune frequency in 10 kHz. In FM mode the valid range is from 6400 to 10800 (64–108 MHz).
3	7:0	$FREQ_L$[7:0]	**Tune Frequency Low Byte.** This byte in combination with $FREQ_H$ selects the tune frequency in 10 kHz. In FM mode the valid range is from 6400 to 10800 (64–108 MHz).
4	7:0	ANTCAP[7:0]	**Antenna Tuning Capacitor (valid only when using TXO/LPI pin as the antenna input).** This selects the value of the antenna tuning capacitor manually, or automatically if set to zero. The valid range is 0 to 191. Automatic capacitor tuning is recommended. **Note:** When tuned manually, the varactor is offset by four codes. For example, if the varactor is set to a value of 5 manually, when read back the value will be 1. The four codes (1pf) delta accounts for the capacitance at the chip.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	RDSINT	X	STCINT

Command 0x21. FM_SEEK_START

Begins searching for a valid frequency. Clears any pending STCINT or RSQINT interrupt status. The CTS bit (and optional interrupt) is set when it is safe to send the next command. RSQINT status is only cleared by the RSQ status command when the INTACK bit is set. The ERR bit (and optional interrupt) is set if an invalid argument is sent. Note that only a single interrupt occurs if both the CTS and ERR bits are set. The optional STC interrupt is set when the command completes. The STCINT bit is set only after the GET_INT_STATUS command is called. This command may only be sent when in powerup mode. The command clears the STCINT bit if it is already set. See Figure 29, “CTS and STC Timing Model,” on page 243 and Table 50, “Command Timing Parameters for the FM Receiver,” on page 245.

Available in: All

Command arguments: One

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	1	0	0	0	0	1
ARG1	0	0	0	0	SEEKUP	WRAP	0	0

ARG	Bit	Name	Function
1	7:4	Reserved	Always write to 0.
1	3	SEEKUP	**Seek Up/Down.** Determines the direction of the search, either UP = 1, or DOWN = 0.
1	2	WRAP	**Wrap/Halt.** Determines whether the seek should Wrap = 1, or Halt = 0 when it hits the band limit.
1	1:0	Reserved	Always write to 0.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	RDSINT	X	STCINT

Command 0x22. FM_TUNE_STATUS

Returns the status of FM_TUNE_FREQ or FM_SEEK_START commands. The command returns the current frequency, RSSI, SNR, multipath, and the antenna tuning capacitance value (0-191). The command clears the STCINT interrupt bit when INTACK bit of ARG1 is set. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode.

Available in: All

Command arguments: One

Response bytes: Seven

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	1	0	0	0	1	0
ARG1	0	0	0	0	0	0	CANCEL	INTACK

ARG	Bit	Name	Function
1	7:2	Reserved	Always write to 0.
1	1	CANCEL	**Cancel seek.** If set, aborts a seek currently in progress.
1	0	INTACK	**Seek/Tune Interrupt Clear.** If set, clears the seek/tune complete interrupt status indicator.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	RDSINT	X	STCINT
RESP1	BLTF	X	X	X	X	X	AFCRL	VALID
RESP2	$READFREQ_H$[7:0]							
RESP3	$READFREQ_L$[7:0]							
RESP4	RSSI[7:0]							
RESP5	SNR[7:0]							
RESP6	MULT[7:0]							
RESP7	READANTCAP[7:0] (Si4704/05/06/2x only)							

RESP	Bit	Name	Function
1	7	BLTF	**Band Limit.** Reports if a seek hit the band limit (WRAP = 0 in FM_START_SEEK) or wrapped to the original frequency (WRAP = 1).
1	6:2	Reserved	Always returns 0.
1	1	AFCRL	**AFC Rail Indicator.** Set if the AFC rails.
1	0	VALID	**Valid Channel.** Set if the channel is currently valid as determined by the seek/tune properties (0x1403, 0x1404, 0x1108) and would have been found during a Seek.
2	7:0	$READFREQ_H$[7:0]	**Read Frequency High Byte.** This byte in combination with $READFREQ_L$ returns frequency being tuned (10 kHz).
3	7:0	$READFREQ_L$[7:0]	**Read Frequency Low Byte.** This byte in combination with $READFREQ_H$ returns frequency being tuned (10 kHz).
4	7:0	RSSI[7:0]	**Received Signal Strength Indicator.** This byte contains the receive signal strength when tune is complete (dBµV).
5	7:0	SNR[7:0]	**SNR.** This byte contains the SNR metric when tune is complete (dB).
6	7:0	MULT[7:0]	**Multipath.** This byte contains the multipath metric when tune is complete. Multipath indicator is available only for Si474x, Si4706-C30 and later and Si4704/05/30/31/34/35/84/85 -D50 and later, and Si4732.
7	7:0	READANTCAP [7:0]	**Read Antenna Tuning Capacitor (Si4704/05/06/2x only)**. This byte contains the current antenna tuning capacitor value.

Command 0x23. FM_RSQ_STATUS

Returns status information about the received signal quality. The commands returns the RSSI, SNR, frequency offset, and stereo blend percentage. It also indicates valid channel (VALID), soft mute engagement (SMUTE), and AFC rail status (AFCRL). This command can be used to check if the received signal is above the RSSI high threshold as reported by RSSIHINT, or below the RSSI low threshold as reported by RSSILINT. It can also be used to check if the signal is above the SNR high threshold as reported by SNRHINT, or below the SNR low threshold as reported by SNRLINT. For the Si4706/4x, it can be used to check if the detected multipath is above the multipath high threshold as reported by MULTHINT, or below the multipath low threshold as reported by MULTLINT. If the PILOT indicator is set, it can also check whether the blend has crossed a threshold as indicated by BLENDINT. The command clears the RSQINT, BLENDINT, SNRHINT, SNRLINT, RSSIHINT, RSSILINT, MULTHINT, and MULTLINT interrupt bits when INTACK bit of ARG1 is set. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode.

Available in: All

Command arguments: One

Response bytes: Seven

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	1	0	0	0	1	1
ARG1	0	0	0	0	0	0	0	INTACK

ARG	Bit	Name	Function
1	0	INTACK	**Interrupt Acknowledge.** 0 = Interrupt status preserved. 1 = Clears RSQINT, BLENDINT, SNRHINT, SNRLINT, RSSIHINT, RSSILINT, MULTHINT, MULTLINT.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	RDSINT	X	STCINT
RESP1	BLENDINT	X	MULTHINT	MULTLINT	SNRHINT	SNRLINT	RSSIHINT	RSSIILINT
RESP2	X	X	X	X	SMUTE	X	AFCRL	VALID
RESP3	PILOT	STBLEND[6:0]						
RESP4	RSSI[7:0]							
RESP5	SNR[7:0]							
RESP6	MULT[7:0]							
RESP7	FREQOFF[7:0]							

RESP	Bit	Name	Function
1	7	BLENDINT	**Blend Detect Interrupt.** 0 = Blend is within the Blend threshold settings. 1 = Blend goes above or below the Blend threshold settings.
1	5	MULTHINT	**Multipath Detect High (Si474x, Si4706-C30 and later and Si4704/05/30/31/34/35/84/85-D50 and later and Si4732 only).** 0 = Detected multipath value has not exceeded above the Multipath high threshold. 1 = Detected multipath value has exceeded above the Multipath high threshold.
1	4	MULTLINT	**Multipath Detect Low (Si474x, Si4706-C30 and later and Si4704/05/30/31/34/35/84/85-D50 and later and Si4732 only).** 0 = Detected multipath value has not fallen below the Multipath low threshold. 1 = Detected multipath value has fallen below the Multipath low threshold.
1	3	SNRHINT	**SNR Detect High.** 0 = Received SNR has not exceeded above SNR high threshold. 1 = Received SNR has exceeded above SNR high threshold.
1	2	SNRLINT	**SNR Detect Low.** 0 = Received SNR has not fallen below SNR low threshold. 1 = Received SNR has fallen below SNR low threshold.
1	1	RSSIHINT	**RSSI Detect High.** 0 = RSSI has not exceeded above RSSI high threshold. 1 = RSSI has exceeded above RSSI high threshold.
1	0	RSSILINT	**RSSI Detect Low.** 0 = RSSI has not fallen below RSSI low threshold. 1 = RSSI has fallen below RSSI low threshold.
2	3	SMUTE	**Soft Mute Indicator.** Indicates soft mute is engaged.
2	1	AFCRL	**AFC Rail Indicator.** Set if the AFC rails.
2	0	VALID	**Valid Channel.** Set if the channel is currently valid and would have been found during a Seek.
3	7	PILOT	**Pilot Indicator.** Indicates stereo pilot presence.
3	6:0	STBLEND[6:0]	**Stereo Blend Indicator.** Indicates amount of stereo blend in% (100 = full stereo, 0 = full mono).
4	7:0	RSSI[7:0]	**Received Signal Strength Indicator.** Contains the current receive signal strength (0–127 dBµV).
5	7:0	SNR[7:0]	**SNR.** Contains the current SNR metric (0–127 dB).
6	7:0	MULT[7:0]	**Multipath (Si474x, Si4706-C30 and later and Si4704/05/30/31/34/35/84/85-D50 and later and Si4732 only).** Contains the current multipath metric. (0 = no multipath; 100 = full multipath)
7	7:0	FREQOFF[7:0]	**Frequency Offset.** Signed frequency offset (kHz).

Command 0x24. FM_RDS_STATUS

Returns RDS information for current channel and reads an entry from the RDS FIFO. RDS information includes synch status, FIFO status, group data (blocks A, B, C, and D), and block errors corrected. This command clears the RDSINT interrupt bit when INTACK bit in ARG1 is set and, if MTFIFO is set, the entire RDS receive FIFO is cleared (FIFO is always cleared during FM_TUNE_FREQ or FM_SEEK_START). The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in power up mode. The FIFO size is 25 groups for FMRX component 2.0 or later, and 14 for FMRX component 1.0.

Notes:

1. FM_RDS_STATUS is supported in FMRX component 2.0 or later.
2. MTFIFO is not supported in FMRX component 2.0.

Available in: Si4705/06, Si4721, Si474x, Si4731/32/35/37/39, Si4785

Command arguments: One

Response bytes: Twelve

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	1	0	0	1	0	0
ARG1	0	0	0	0	0	STATUSONLY	MTFIFO	INTACK

ARG	Bit	Name	Function
1	2	STATUSONLY	**Status Only.** Determines if data should be removed from the RDS FIFO. 0 = Data in BLOCKA, BLOCKB, BLOCKC, BLOCKD, and BLE contain the oldest data in the RDS FIFO. 1 = Data in BLOCKA will contain the last valid block A data received for the current station. Data in BLOCKB will contain the last valid block B data received for the current station. Data in BLE will describe the bit errors for the data in BLOCKA and BLOCKB.
1	1	MTFIFO	**Empty FIFO** 0 = If FIFO not empty, read and remove oldest FIFO entry. 1 = Clear RDS Receive FIFO.
1	0	INTACK	**Interrupt Acknowledge** 0 = RDSINT status preserved. 1 = Clears RDSINT.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	RDSINT	X	STCINT
RESP1	X	X	RDSNEWBLOCKB	RDSNEWBLOCKA	X	RDSSYNCFOUND	RDSSYNCLOST	RDSRECV
RESP2	X	X	X	X	X	GRPLOST	X	RDSSYNC
RESP3	RDSFIFOUSED[7:0]							

Bit	D7	D6	D5	D4	D3	D2	D1	D0
RESP4	BLOCKA[15:8]							
RESP5	BLOCKA[7:0]							
RESP6	BLOCKB[15:8]							
RESP7	BLOCKB[7:0]							
RESP8	BLOCKC[15:8]							
RESP9	BLOCKC[7:0]							
RESP10	BLOCKD[15:8]							
RESP11	BLOCKD[7:0]							
RESP12	BLEA[1:0]		BLEB[1:0]		BLEC[1:0]		BLED[1:0]	

RESP	Bit	Name	Function
1	5	RDSNEWBLOCKB	**RDS New Block B.** 1 = Valid Block B data has been received.
1	4	RDSNEWBLOCKA	**RDS New Block A.** 1 = Valid Block A data has been received.
1	2	RDSSYNCFOUND	**RDS Sync Found.** 1 = Found RDS synchronization.
1	1	RDSSYNCLOST	**RDS Sync Lost.** 1 = Lost RDS synchronization.
1	0	RDSRECV	**RDS Received.** 1 = FIFO filled to minimum number of groups set by RDSFIFOCNT.
2	2	GRPLOST	**Group Lost.** 1 = One or more RDS groups discarded due to FIFO overrun.
2	0	RDSSYNC	**RDS Sync.** 1 = RDS currently synchronized.
3	7:0	RDSFIFOUSED	**RDS FIFO Used.** Number of groups remaining in the RDS FIFO (0 if empty). If non-zero, BLOCKA-BLOCKD contain the oldest FIFO entry and RDSFIFOUSED decrements by one on the next call to RDS_FIFO_STATUS (assuming no RDS data received in the interim).
4	7:0	BLOCKA[15:8]	**RDS Block A.** Block A group data from oldest FIFO entry if STATUSONLY is 0. Last valid Block A data if STATUSONLY is 1 (Si4749, Si4706-C30 and later and Si4705/31/35/85-D50 and later and Si4732 only).
5	7:0	BLOCKA[7:0]	
6	7:0	BLOCKB[15:8]	**RDS Block B.** Block B group data from oldest FIFO entry if STATUSONLY is 0. Last valid Block B data if STATUSONLY is 1 (Si4749, Si4706-C30 and later and Si4705/31/35/85-D50 and later and Si4732 only).
7	7:0	BLOCKB[7:0]	
8	7:0	BLOCKC[15:8]	**RDS Block C.** Block C group data from oldest FIFO entry.
9	7:0	BLOCKC[7:0]	

RESP	Bit	Name	Function
10	7:0	BLOCKD[15:8]	**RDS Block D.** Block D group data from oldest FIFO entry.
11	7:0	BLOCKD[7:0]	
12	7:6	BLEA[1:0]	**RDS Block A Corrected Errors.** 0 = No errors. 1 = 1–2 bit errors detected and corrected. 2 = 3–5 bit errors detected and corrected. 3 = Uncorrectable.
12	5:4	BLEB[1:0]	**RDS Block B Corrected Errors.** 0 = No errors. 1 = 1–2 bit errors detected and corrected. 2 = 3–5 bit errors detected and corrected. 3 = Uncorrectable.
12	3:2	BLEC[1:0]	**RDS Block C Corrected Errors.** 0 = No errors. 1 = 1–2 bit errors detected and corrected. 2 = 3–5 bit errors detected and corrected. 3 = Uncorrectable.
12	1:0	BLED[1:0]	**RDS Block D Corrected Errors.** 0 = No errors. 1 = 1–2 bit errors detected and corrected. 2 = 3–5 bit errors detected and corrected. 3 = Uncorrectable.

Command 0x27. FM_AGC_STATUS

Returns the AGC setting of the device. The command returns whether the AGC is enabled or disabled and it returns the LNA Gain index. This command may only be sent when in powerup mode.

Available in: All

Command arguments: None

Response bytes: Two

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	1	0	0	1	1	1

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	RDSINT	X	STCINT
RESP1	X	X	X	X	X	X	X	READ_RF-AGCDIS
RESP2	X	X	X	READ_LNA_GAIN_INDEX[4:0]				

RESP	Bit	Name	Function
1	0	READ_RFAGCDIS	**This bit indicates whether the RF AGC is disabled or not** 0 = RF AGC is enabled 1 = RF AGC is disabled
2	4:0	READ_LNA_GAIN_INDEX	**These bits returns the value of the LNA GAIN index** 0 = Minimum attenuation (max gain) 1 – 25 = Intermediate attenuation 26 = Maximum attenuation (min gain) **Note:** The max index is subject to change

Command 0x28. FM_AGC_OVERRIDE

Overrides AGC setting by disabling the AGC and forcing the LNA to have a certain gain that ranges between 0 (minimum attenuation) and 26 (maximum attenuation). This command may only be sent when in powerup mode.

Available in: All

Command arguments: Two

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	1	0	1	0	0	0
ARG1	X	X	X	X	X	X	X	RFAGCDIS
ARG2	X	X	X	LNA_GAIN_INDEX[4:0]				

ARG	Bit	Name	Function
1	0	RFAGCDIS	**This bit selects whether the RF AGC is disabled or not** 0 = RF AGC is enabled 1 = RF AGC is disabled
2	4:0	LNA_GAIN_INDEX	**These bits set the value of the LNA GAIN index** 0 = Minimum attenuation (max gain) 1 – 25 = Intermediate attenuation 26 = Maximum attenuation (min gain) Note: the max index is subject to change

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	RDSINT	X	STCINT

Command 0x80. GPIO_CTL

Enables output for GPO1, 2, and 3. GPO1, 2, and 3 can be configured for output (Hi-Z or active drive) by setting the GPO1OEN, GPO2OEN, and GPO3OEN bit. The state (high or low) of GPO1, 2, and 3 is set with the GPIO_SET command. To avoid excessive current consumption due to oscillation, GPO pins should not be left in a high impedance state. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode. The default is all GPO pins set for high impedance.

Notes:

1. GPIO_CTL is fully supported in FMRX component 2.0 or later. Only bit GPO3OEN is supported in FMRX component 1.0.
2. The use of GPO2 as an interrupt pin and/or the use of GPO3 as DCLK digital clock input will override this GPIO_CTL function for GPO2 and/or GPO3 respectively.

Available in: All except Si4710-A10

Command arguments: One

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	1	0	0	0	0	0	0	0
ARG1	0	0	0	0	GPO3OEN	GPO2OEN	GPO1OEN	0

ARG	Bit	Name	Function
1	7:4	Reserved	Always write 0.
1	3	GPO3OEN	**GPO3 Output Enable.** 0 = Output Disabled (Hi-Z) (default). 1 = Output Enabled.
1	2	GPO2OEN	**GPO2 Output Enable.** 0 = Output Disabled (Hi-Z) (default). 1 = Output Enabled.
1	1	GPO1OEN	**GPO1 Output Enable.** 0 = Output Disabled (Hi-Z) (default). 1 = Output Enabled.
1	0	Reserved	Always write 0.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	RDSINT	ASQINT	STCINT

Command 0x81. GPIO_SET

Sets the output level (high or low) for GPO1, 2, and 3. GPO1, 2, and 3 can be configured for output by setting the GPO1OEN, GPO2OEN, and GPO3OEN bit in the GPIO_CTL command. To avoid excessive current consumption due to oscillation, GPO pins should not be left in a high impedance state. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is all GPO pins set for high impedance.

Note: GPIO_SET is fully-supported in FMRX component 2.0 or later. Only bit GPO3LEVEL is supported in FMRX component 1.0.

Available in: All except Si4710-A10

Command arguments: One

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	1	0	0	0	0	0	0	1
ARG1	0	0	0	0	GPO3LEVEL	GPO2LEVEL	GPO1LEVEL	0

ARG	Bit	Name	Function
1	7:4	Reserved	Always write 0.
1	3	GPO3LEVEL	**GPO3 Output Level.** 0 = Output low (default). 1 = Output high.
1	2	GPO2LEVEL	**GPO2 Output Level.** 0 = Output low (default). 1 = Output high.
1	1	GPO1LEVEL	**GPO1 Output Level.** 0 = Output low (default). 1 = Output high.
1	0	Reserved	Always write 0.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	RDSINT	ASQINT	STCINT

5.2.2. FM/RDS Receiver Properties

Property 0x0001. GPO_IEN

Configures the sources for the GPO2/$\overline{\text{INT}}$ interrupt pin. Valid sources are the lower 8 bits of the STATUS byte, including CTS, ERR, RSQINT, RDSINT (Si4705/21/31/32/35/37/39/41/43/45/85 only), and STCINT bits. The corresponding bit is set before the interrupt occurs. The CTS bit (and optional interrupt) is set when it is safe to send the next command. The CTS interrupt enable (CTSIEN) can be set with this property and the POWER_UP command. The state of the CTSIEN bit set during the POWER_UP command can be read by reading this property and modified by writing this property. This property may only be set or read when in powerup mode.

Errata:RSQIEN is non-functional on FMRX component 2.0.
Available in: All

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	RSQREP	RDSREP	0	STCREP	CTSIEN	ERRIEN	0	0	RSQIEN	RDSIEN	0	STCIEN

Bit	Name	Function
15:12	Reserved	Always write to 0.
11	RSQREP	**RSQ Interrupt Repeat.** 0 = No interrupt generated when RSQINT is already set (default). 1 = Interrupt generated even if RSQINT is already set.
10	RDSREP	**RDS Interrupt Repeat (Si4705/21/31/35/37/39/41/43/45/85-C40 and Si4732 Only).** 0 = No interrupt generated when RDSINT is already set (default). 1 = Interrupt generated even if RDSINT is already set.
9	Reserved	Always write to 0.
8	STCREP	**STC Interrupt Repeat.** 0 = No interrupt generated when STCINT is already set (default). 1 = Interrupt generated even if STCINT is already set.
7	CTSIEN	**CTS Interrupt Enable. After PowerUp, this bit reflects the CTSIEN bit in ARG1 of PowerUp Command.** 0 = No interrupt generated when CTS is set. 1 = Interrupt generated when CTS is set.
6	ERRIEN	**ERR Interrupt Enable.** 0 = No interrupt generated when ERR is set (default). 1 = Interrupt generated when ERR is set.
5:4	Reserved	Always write to 0.
3	RSQIEN	**RSQ Interrupt Enable.** 0 = No interrupt generated when RSQINT is set (default). 1 = Interrupt generated when RSQINT is set.
2	RDSIEN	**RDS Interrupt Enable (Si4705/21/31/35/37/39/41/43/45/85-C40 and Si4732 Only).** 0 = No interrupt generated when RDSINT is set (default). 1 = Interrupt generated when RDSINT is set.
1	Reserved	Always write to 0.
0	STCIEN	**Seek/Tune Complete Interrupt Enable.** 0 = No interrupt generated when STCINT is set (default). 1 = Interrupt generated when STCINT is set.

Property 0x0102. DIGITAL_OUTPUT_FORMAT

Configures the digital audio output format. Configuration options include DCLK edge, data format, force mono, and sample precision.

Available in: Si4704-D60 and later, Si4705/06, Si4721/31/32/35/37/39, Si4730/34/36/38-D60 and later, Si4741/43/45, Si4784/85

Default: 0x0000

Note: DIGITAL_OUTPUT_FORMAT is supported in FM receive component 2.0 or later.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	OFALL	OMODE[3:0]				OMONO	OSIZE[1:0]	

Bit	Name	Function
15:8	Reserved	Always write to 0.
7	OFALL	**Digital Output DCLK Edge.** 0 = use DCLK rising edge 1 = use DCLK falling edge
6:3	OMODE[3:0]	**Digital Output Mode.** 0000 = I^2S 0110 = Left-justified 1000 = MSB at second DCLK after DFS pulse 1100 = MSB at first DCLK after DFS pulse
2	OMONO	**Digital Output Mono Mode.** 0 = Use mono/stereo blend (per blend thresholds) 1 = Force mono
1:0	OSIZE[1:0]	**Digital Output Audio Sample Precision.** 0 = 16-bits 1 = 20-bits 2 = 24-bits 3 = 8-bits

Property 0x0104. DIGITAL_OUTPUT_SAMPLE_RATE

Enables digital audio output and configures digital audio output sample rate in samples per second (sps). When DOSR[15:0] is 0, digital audio output is disabled. The over-sampling rate must be set in order to satisfy a minimum DCLK of 1 MHz. To enable digital audio output, program DOSR[15:0] with the sample rate in samples per second. **The system controller must establish DCLK and DFS prior to enabling the digital audio output else the device will not respond and will require reset. The sample rate must be set to 0 before the DCLK/DFS is removed. FM_TUNE_FREQ command must be sent after the POWER_UP command to start the internal clocking before setting this property.**

Note: DIGITAL_OUPTUT_SAMPLE_RATE is supported in FM receive component 2.0 or later.

Available in: Si4704-D60 and later, Si4705/06, Si4721/31/32/35/37/39, Si4730/34/36/38-D60 and later, Si4741/43/45, Si4784/85

Default: 0x0000 (digital audio output disabled)

Units: sps

Range: 32–48 ksps, 0 to disable digital audio output

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOSR[15:0]															

Bit	Name	Function
15:0	DOSR[15:0]	**Digital Output Sample Rate.** 32–48 ksps. 0 to disable digital audio output.

Property 0x0201. REFCLK_FREQ

Sets the frequency of the REFCLK from the output of the prescaler. The REFCLK range is 31130 to 34406 Hz (32768 ±5% Hz) in 1 Hz steps, or 0 (to disable AFC). For example, an RCLK of 13 MHz would require a prescaler value of 400 to divide it to 32500 Hz REFCLK. The reference clock frequency property would then need to be set to 32500 Hz. RCLK frequencies between 31130 Hz and 40 MHz are supported, however, there are gaps in frequency coverage for prescaler values ranging from 1 to 10, or frequencies up to 311300 Hz. The following table summarizes these RCLK gaps.

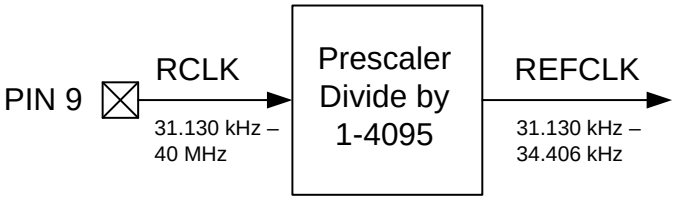


Figure 2. REFCLK Prescaler

Table 11. RCLK Gaps

Prescaler	RCLK Low (Hz)	RCLK High (Hz)
1	31130	34406
2	62260	68812
3	93390	103218
4	124520	137624
5	155650	172030
6	186780	206436
7	217910	240842
8	249040	275248
9	280170	309654
10	311300	344060

The RCLK must be valid 10 ns before sending and 20 ns after completing the FM_TUNE_FREQ and FM_SEEK_START commands. In addition, the RCLK must be valid at all times for proper AFC operation. The RCLK may be removed or reconfigured at other times. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 32768 Hz.

Available in: All

Default: 0x8000 (32768)

Units: 1 Hz

Step: 1 Hz

Range: 31130–34406

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	REFCLKF[15:0]															

Bit	Name	Function
15:0	REFCLKF[15:0]	**Frequency of Reference Clock in Hz.** The allowed REFCLK frequency range is between 31130 and 34406 Hz (32768 ±5%), or 0 (to disable AFC).

Property 0x0202. REFCLK_PRESCALE

Sets the number used by the prescaler to divide the external RCLK down to the internal REFCLK. The range may be between 1 and 4095 in 1 unit steps. For example, an RCLK of 13 MHz would require a prescaler value of 400 to divide it to 32500 Hz. The reference clock frequency property would then need to be set to 32500 Hz. The RCLK must be valid 10 ns before sending and 20 ns after completing the FM_TUNE_FREQ and FM_TUNE_START commands. In addition, the RCLK must be valid at all times for proper AFC operation. The RCLK may be removed or reconfigured at other times. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 1.

Available in: All

Default: 0x0001

Step: 1

Range: 1–4095

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	RCLK SEL	REFCLKP[11:0]											

Bit	Name	Function
15:13	Reserved	Always write to 0.
12	RCLKSEL	**RCLKSEL.** 0 = RCLK pin is clock source. 1 = DCLK pin is clock source.
11:0	REFCLKP[11:0]	**Prescaler for Reference Clock.** Integer number used to divide clock frequency down to REFCLK frequency. The allowed REFCLK frequency range is between 31130 and 34406 Hz (32768 5%), or 0 (to disable AFC).

Property 0x1100. FM_DEEMPHASIS

Sets the FM Receive de-emphasis to 50 or 75 µs. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 75 µs.

Available in: All except Si4749

Default: 0x0002

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DEEMPH[1:0]	

Bit	Name	Function
15:2	Reserved	Always write to 0.
1:0	DEEMPH[1:0]	**FM De-Emphasis.** 10 = 75 µs. Used in USA (default) 01 = 50 µs. Used in Europe, Australia, Japan 00 = Reserved 11 = Reserved

Property 0x1102. FM_CHANNEL_FILTER

Selects bandwidth of channel filter applied at the demodulation stage. Default is automatic which means the device automatically selects proper channel filter. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 1.

Available in: Si4706, Si4749, Si4704/05/30/31/34/35/84/85-D50 and later, Si4732

Default: 0x0001 (Si4706, Si4749, Si4705/31/35/85-D50 and later, Si4732)

0x0000 (Si4704/30/34/84-D50 and later)

Range: 0–4

Note: Automatic channel filter setting is not supported in FMRX component 3.0.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	FMCHFILT[15:0]															

Bit	Name	Function
15:0	FM_CHANNEL_FILTER	0 = Automatically select proper channel filter. 1 = Force wide (110 kHz) channel filter. 2 = Force narrow (84 kHz) channel filter. 3 = Force narrower (60 kHz) channel filter. 4 = Force narrowest (40 kHz) channel filter.

Property 0x1105. FM_BLEND_STEREO_THRESHOLD

Sets RSSI threshold for stereo blend (Full stereo above threshold, blend below threshold). To force stereo, set this to 0. To force mono, set this to 127. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 49 dBµV.

Available in: Si470x/2x, Si473x-C40 and earlier

Default: 0x0031

Units: dBµV

Step: 1

Range: 0–127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	STTHRESH[6:0]						

Bit	Name	Function
15:7	Reserved	Always write to 0.
6:0	STTHRESH	**FM Blend Stereo Threshold.** RSSI threshold below which the audio output goes into a blend mode. Above this threshold the audio output is in full stereo. Specified in units of dBµV in 1 dB steps (0–127). Default is 49 dBµV.

Property 0x1106. FM_BLEND_MONO_THRESHOLD

Sets RSSI threshold for mono blend (Full mono below threshold, blend above threshold). To force stereo, set this to 0. To force mono, set this to 127. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 30 dBµV.

Available in: Si470x/2x, Si473x-C40 and earlier

Default: 0x001E

Units: dBµV

Step: 1

Range: 0–127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	MONOTHRESH[6:0]						

Bit	Name	Function
15:7	Reserved	Always write to 0.
6:0	MONOTHRESH	**FM Blend Mono Threshold.** RSSI threshold below which the audio output goes into full mono mode. Above this threshold the audio output is in blend or full stereo. Specified in units of dBµV in 1 dB steps (0–127). Default is 30 dBµV.

Property 0x1107. FM_ANTENNA_INPUT

Selects what type of antenna and what pin it is connected to. Default is 0 which means the antenna used is a headphone (long) antenna and it is connected to the FMI pin. Setting the FMTXO bit to 1 means that the antenna used is an embedded (short) antenna and it is connected to the TXO/LPI pin.

Note: To assure proper tuning, the FM_TUNE_FREQ command should be issued immediately after this property is changed.

Available in: Si4704/05/06/20/21

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FMTXO

Bit	Name	Function
15:1	Reserved	Always write to 0
0	FMTXO	**Selects what type of antenna and which pin it is connected to:** 0 = Use FMI pin for headphone (long) antenna 1 = Use TXO/LPI pin for embedded (short) antenna

Property 0x1108. FM_MAX_TUNE_ERROR

Sets the maximum freq error allowed before setting the AFC rail indicator (AFCRL). The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 20 kHz.

Note: For FMRX components 2.0 or earlier, the default is set to 30 kHz. For best seek performance, set FM_MAX_TUNE_ERROR to 20 kHz.

Available in: All

Default: 0x001E (Si473x-B20 and earlier)

0x0014 (all others)

Units: kHz

Step: 1

Range: 0–255

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	FMMAXTUNEERR[7:0]							

Bit	Name	Function
15:8	Reserved	Always write to 0.
7:0	FMMAXTUNEERR	**FM Maximum Tuning Frequency Error.** Maximum tuning error allowed before setting the AFC Rail Indicator ON. Specified in units of kHz. Default is 20 kHz.

Property 0x1200. FM_RSQ_INT_SOURCE

Configures interrupt related to Received Signal Quality metrics. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 0.

Available in: All

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	BLEN-DIEN	0	MULT HIEN	MULT-LIEN	SNRHIEN	SNRLIEN	RSSIHIEN	RSSILIEN

Bit	Name	Function
15:8	Reserved	Always write to 0.
7	BLENDIEN	**Interrupt Source Enable: Blend.** Enable blend as the source of interrupt which the threshold is set by FM_R-SQ_BLEND_THRESHOLD.
6	Reserved	Always write to 0.
5	MULTHIEN	**Interrupt Source Enable: Multipath High (Si4706-C30 and later, Si474x and Si4704/05/30/31/34/35/84/85-D50 and later and Si4732 only).** Enable Multipath high as the source of interrupt which the threshold is set by FM_RSQ_-MULTIPATH_HI_THRESHOLD.
4	MULTLIEN	**Interrupt Source Enable: Multipath Low (Si4706-C30 and later, Si474x and Si4704/05/30/31/34/35/84/85-D50 and later and Si4732 only).** Enable Multipath low as the source of interrupt which the threshold is set by FM_RSQ_-MULTIPATH_LO_THRESHOLD.
3	SNRHIEN	**Interrupt Source Enable: SNR High.** Enable SNR high as the source of interrupt which the threshold is set by FM_RSQ_SN-R_HI_THRESHOLD.
2	SNRLIEN	**Interrupt Source Enable: SNR Low.** Enable SNR low as the as the source of interrupt which the threshold is set by FM_R-SQ_SNR_LO_THRESHOLD.
1	RSSIHIEN	**Interrupt Source Enable: RSSI High.** Enable RSSI high as the source of interrupt which the threshold is set by FM_R-SQ_RSSI_HI_THRESHOLD.
0	RSSILIEN	**Interrupt Source Enable: RSSI Low.** Enable RSSI low as the source of interrupt which the threshold is set by FM_R-SQ_RSSI_LO_THRESHOLD.

Property 0x1201. FM_RSQ_SNR_HI_THRESHOLD

Sets high threshold which triggers the RSQ interrupt if the SNR is above this threshold. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 127dB.

Available in: All

Default: 0x007F

Units: dB

Step: 1

Range: 0–127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	SNRH[6:0]						

Bit	Name	Function
15:7	Reserved	Always write to 0.
6:0	SNRH	**FM RSQ SNR High Threshold.** Threshold which triggers the RSQ interrupt if the SNR is above this threshold. Specified in units of dB in 1 dB steps (0–127). Default is 127 dB.

Property 0x1202. FM_RSQ_SNR_LO_THRESHOLD

Sets low threshold which triggers the RSQ interrupt if the SNR is below this threshold. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 0 dB.

Available in: All

Default: 0x0000

Units: dB

Step: 1

Range: 0–127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	SNRL[6:0]						

Bit	Name	Function
15:7	Reserved	Always write to 0.
6:0	SNRL	**FM RSQ SNR Low Threshold.** Threshold which triggers the RSQ interrupt if the SNR is below this threshold. Specified in units of dB in 1 dB steps (0–127). Default is 0 dB.

Property 0x1203. FM_RSQ_RSSI_HI_THRESHOLD

Sets high threshold which triggers the RSQ interrupt if the RSSI is above this threshold. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 127 dBµV.

Available in: All

Default: 0x007F

Units: dBµV

Step: 1

Range: 0–127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	RSSIH[6:0]						

Bit	Name	Function
15:7	Reserved	Always write to 0.
6:0	RSSIH	**FM RSQ RSSI High Threshold.** Threshold which triggers the RSQ interrupt if the RSSI is above this threshold. Specified in units of dBµV in 1 dB steps (0–127). Default is 127 dBµV.

Property 0x1204. FM_RSQ_RSSI_LO_THRESHOLD

Sets low threshold which triggers the RSQ interrupt if the RSSI is below this threshold. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 0 dBµV.

Available in: All

Default: 0x0000

Units: dBµV

Step: 1

Range: 0–127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	RSSIL[6:0]						

Bit	Name	Function
15:7	Reserved	Always write to 0.
6:0	RSSIL	**FM RSQ RSSI Low Threshold.** Threshold which triggers the RSQ interrupt if the RSSI is below this threshold. Specified in units of dBµV in 1 dB steps (0–127). Default is 0 dBµV.

Property 0x1205. FM_RSQ_MULTIPATH_HI_THRESHOLD

Sets the high threshold which triggers the RSQ interrupt if the Multipath level is above this threshold. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in power up mode. The value may be the threshold multipath percent (0–100), or 127 to disable the feature.

Available in: Si4706-C30 and later, Si474x, Si4704/05/30/31/34/35/84/85-D50 and later, Si4732

Default: 0x007F

Step: 1

Range: 0–127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	MULTH[6:0]						

Bit	Name	Function
15:7	Reserved	Always write to 0.
6:0	MULTH	**FM RSQ Multipath High Threshold.** Threshold which triggers the RSQ interrupt if the Multipath is above this threshold. Default is 127.

Property 0x1206. FM_RSQ_MULTIPATH_LO_THRESHOLD

Sets the low threshold which triggers the RSQ interrupt if the Multipath level is below this threshold. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in power up mode. The default is 0.

Available in: Si4706-C30 and later, Si474x, Si4704/05/30/31/34/35/84/85-D50 and later, Si4732

Default: 0x0000

Step: 1

Range: 0–127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	MULTL[6:0]						

Bit	Name	Function
15:7	Reserved	Always write to 0
6:0	MULTL	**FM RSQ Multipath Low Threshold.** Threshold which triggers the RSQ interrupt if the Multipath is below this threshold. Default is 0.

Property 0x1207. FM_RSQ_BLEND_THRESHOLD

Sets the blend threshold for blend interrupt when boundary is crossed. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 1%.

Available in: All except Si4749

Default: 0x0081

Units: %

Step: 1

Range: 0–100

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	PILOT	BLEND[6:0]						

Bit	Name	Function
15:8	Reserved	Always write to 0.
7	PILOT	**Pilot Indicator.** This bit has to be set to 1 (there has to be a pilot present) in order for FM_RSQ_BLEND_THRESHOLD to trigger an interrupt. Without a pilot tone, the part is always in full mono mode and never goes into blend.
6:0	BLEND	**FM RSQ Blend Threshold.** This is a boundary cross threshold. If the blend cross from above to below, or the other way around from below to above this threshold, it will trigger an interrupt. Specified in units of % in 1% steps (0–100). Default is 1%.

Property 0x1300. FM_SOFT_MUTE_RATE

Sets the attack and decay rates when entering and leaving soft mute. Later values increase rates, and lower values decrease rates. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 0x0040.

Available in: Si4706/07/20/21/84/85-B20 and earlier, Si4704/05/3x-C40 and earlier

Default: 64

Step: 1

Range: 1—255

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	SMRATE[7:0]							

Property 0x1301. FM_SOFT_MUTE_SLOPE

Configures attenuation slope during soft mute in dB attenuation per dB SNR below the soft mute SNR threshold. Soft mute attenuation is the minimum of SMSLOPE x (SMTHR – SNR) and SMATTN. The recommended SMSLOPE value is CEILING(SMATTN/SMTHR). SMATTN and SMTHR are set via the FM_SOFT_MUTE_MAX_ATTENUATION and FM_SOFT_MUTE_SNR_THRESHOLD properties. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in power up mode. The default soft mute slope property setting is 2 dB/dB in supported devices. The soft mute slope is not configurable in Si4704/05/3x-B20 devices (those with FMRX component 2.0) and is 2 dB/dB. The soft mute slope is not configurable in Si4710/20-A10 devices (those with FMRX component 1.0), and is 0 dB/dB (disabled).

Available in: Si4704/05/06/3x-C40 and later, Si4732, Si4740/41/42/43/44/45

Default: 0x0002

Range: 0–63

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	SMSLOPE[7:0]							

Property 0x1302. FM_SOFT_MUTE_MAX_ATTENUATION

Sets maximum attenuation during soft mute (dB). Set to 0 to disable soft mute. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 16 dB.

Available in: All except Si4749

Default: 0x0010

Units: dB

Step: 1

Range: 0–31

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	SMATTN[4:0]				

Bit	Name	Function
15:5	Reserved	Always write to 0.
4:0	SMATTN	**FM Soft Mute Maximum Attenuation.** Set maximum attenuation during soft mute. If set to 0, then soft mute is disabled. Specified in units of dB in 1 dB steps (0–31). Default is 16 dB.

Property 0x1303. FM_SOFT_MUTE_SNR_THRESHOLD

Sets SNR threshold to engage soft mute. Whenever the SNR for a tuned frequency drops below this threshold, the FM reception will go in soft mute, provided soft mute max attenuation property is non-zero. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 4 dB.

Available in: All except Si4749

Default: 0x0004

Units: dB

Step: 1

Range: 0–15

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	SMTHR[3:0]			

Bit	Name	Function
15:4	Reserved	Always write to 0.
3:0	SMTHR	**FM Soft Mute SNR Threshold.** Threshold which will engage soft mute if the SNR falls below this. Specified in units of dB in 1 dB steps (0–15). Default is 4 dB.

Property 0x1304. FM_SOFT_MUTE_RELEASE_RATE

Sets the soft mute release rate. Smaller values provide slower release and larger values provide faster release. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 8192 (approximately 8000 dB/s).

Release Rate (dB/s) = RELEASE[14:0]/1.024

Available in: Si4706-C30 and later, Si4740/41/42/43/44/45, Si4704/05/30/31/34/35/84/85-D50 and later, Si4732

Default: 0x2000

Range: 1–32767

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	RELEASE[14:0]														

Property 0x1305. FM_SOFT_MUTE_ATTACK_RATE

Sets the soft mute attack rate. Smaller values provide slower attack and larger values provide faster attack. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 8192 (approximately 8000 dB/s).

Attack Rate (dB/s) = ATTACK[14:0]/1.024

Available in: Si4706-C30 and later, Si4740/41/42/43/44/45, Si4704/05/30/31/34/35/84/85-D50 and later, Si4732

Default: 0x2000

Range: 1–32767

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	ATTACK[14:0]														

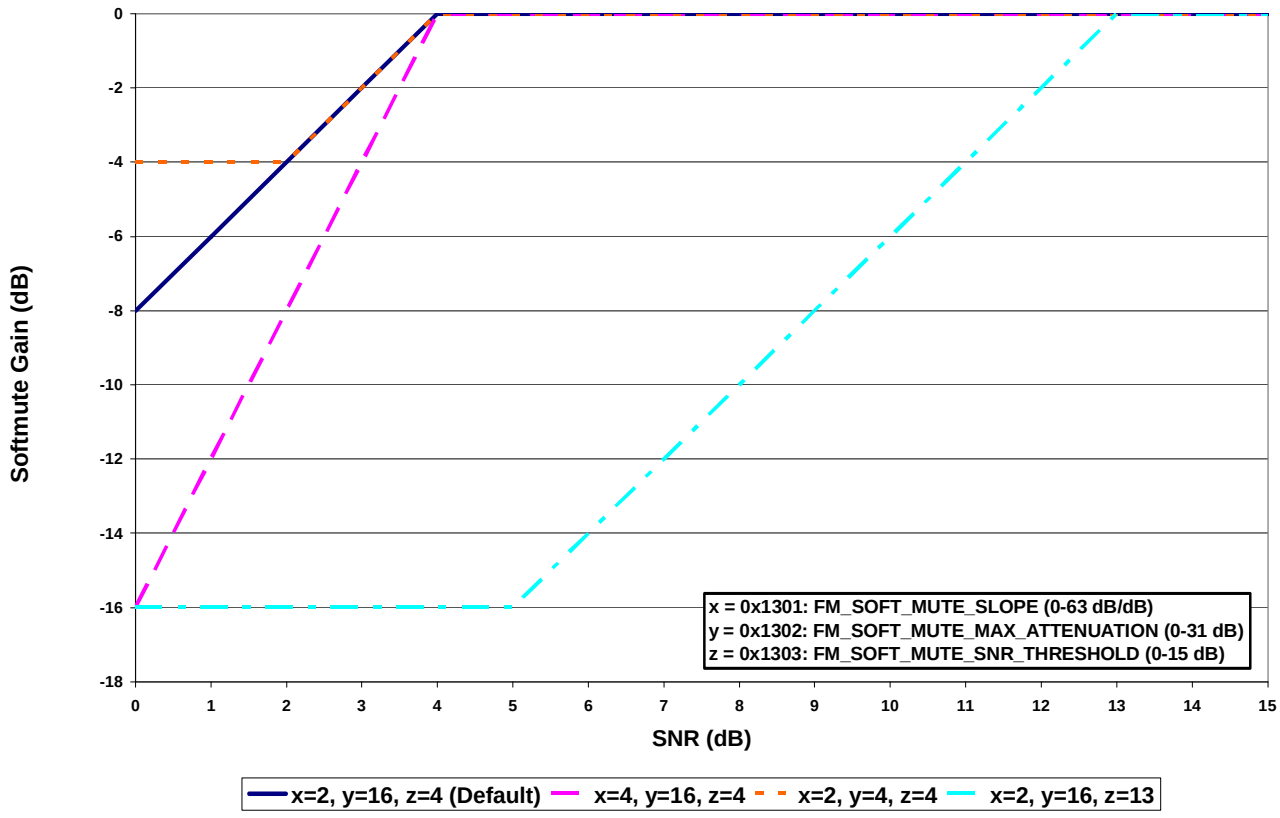


Figure 3. Softmute Gain (dB)

Property 0x1400. FM_SEEK_BAND_BOTTOM

Sets the bottom of the FM band for seek. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 87.5 MHz.

Available in: All

Default: 0x222E

Units: 10 kHz

Step: 50 kHz

Range: 64–108 MHz

Note: For FMRX components 2.0 or earlier, range is 76–108 MHz.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	FMSKFREQL[15:0]															

Bit	Name	Function
15:0	FMSKFREQL	**FM Seek Band Bottom Frequency.** Selects the bottom of the FM Band during Seek. Specified in units of 10 kHz. Default is 8750 (87.5 MHz).

Property 0x1401. FM_SEEK_BAND_TOP

Sets the top of the FM band for seek. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 107.9 MHz.

Available in: All

Default: 0x2A26

Units: 10 kHz

Step: 50 kHz

Range: 64–108 MHz

Note: For FMRX components 2.0 or earlier, range is 76–108 MHz.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	FMSKFREQH[15:0]															

Bit	Name	Function
15:0	FMSKFREQH	**FM Seek Band Top Frequency.** Selects the top of the FM Band during Seek. Specified in units of 10 kHz. Default is 10790 (107.9 MHz).

Property 0x1402. FM_SEEK_FREQ_SPACING

Selects frequency spacing for FM seek. There are only 3 valid values: 5, 10, and 20. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 100 kHz.

Available in: All

Default: 0x000A

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	SKSPACE[4:0]				

Bit	Name	Function
15:5	Reserved	Always write to 0.
4:0	SKSPACE	**FM Seek Frequency Spacing.** Selects the frequency spacing during Seek function. Specified in units of 10 kHz. There are only 3 valid values: 5 (50 kHz), 10 (100 kHz), and 20 (200 kHz). Default is 10.

Property 0x1403. FM_SEEK_TUNE_SNR_THRESHOLD

Sets the SNR threshold for a valid FM Seek/Tune. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 3 dB.

Available in: All

Default: 0x0003

Units: dB

Step: 1

Range: 0–127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	SKSNR[6:0]						

Bit	Name	Function
15:7	Reserved	Always write to 0.
6:0	SKSNR	**FM Seek/Tune SNR Threshold.** SNR Threshold which determines if a valid channel has been found during Seek/Tune. Specified in units of dB in 1 dB steps (0–127). Default is 3 dB.

Property 0x1404. FM_SEEK_TUNE_RSSI_THRESHOLD

Sets the RSSI threshold for a valid FM Seek/Tune. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 20 dBµV.

Available in: All

Default: 0x0014

Units: dBµV

Step: 1

Range: 0–127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	SKRSSI[6:0]						

Bit	Name	Function
15:7	Reserved	Always write to 0.
6:0	SKRSSI	**FM Seek/Tune Received Signal Strength Threshold.** RSSI threshold which determines if a valid channel has been found during seek/tune. Specified in units of dBµV in 1 dBµV steps (0–127). Default is 20 dBµV.

Property 0x1500. FM_RDS_INT_SOURCE

Configures interrupt related to RDS. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 0.

Available in: Si4705/06, Si4721, Si4731/32/35/37/39, Si4741/43/45/49

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	RDSNEW-BLOCKB	RDSNEW-BLOCKA	0	RDSSYNC-FOUND	RDSSYN-CLOST	RDSRECV

Bit	Name	Function
15:6	Reserved	Always write to 0.
5	RDSNEWBLOCKB	**RDS New Block B Found (Si4706, Si474x, and Si4705/31/35/85-D50 and later, and Si4732 only)** If set, generate an interrupt when Block B data is found or subsequently changed.
4	RDSNEWBLOCKA	**RDS New Block A Found (Si4706,Si474x and Si4705/31/35/85-D50 and later, and Si4732 only)** If set, generate an interrupt when Block A data is found or subsequently changed
3	Reserved	Always write to 0.
2	RDSSYNCFOUND	**RDS Sync Found.** If set, generate RDSINT when RDS gains synchronization.
1	RDSSYNCLOST	**RDS Sync Lost.** If set, generate RDSINT when RDS loses synchronization.
0	RDSRECV	**RDS Received.** If set, generate RDSINT when RDS FIFO has at least FM_RDS_INT_FIFO_COUNT entries.

Property 0x1501. FM_RDS_INT_FIFO_COUNT

Sets the minimum number of RDS groups stored in the RDS FIFO before RDSRECV is set. The maximum value is 25 for FRMX component 2.0 or later, and 14 for FMRX component 1.0. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. Default is 0.

Note: FM_RDS_INT_FIFO_COUNT is supported in FMRX component 2.0 or later.

Available in: Si4705/06, Si4721, Si4731/32/35/37/39, Si4741/43/45/49

Default: 0x0000

Range: 0–25

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	RDSFIFOCNT[7:0]							

Bit	Name	Function
7:0	RDSFIFOCNT	**RDS FIFO Count.** Minimum number of RDS groups stored in the RDS FIFO before RDSRECV is set.

Property 0x1502. FM_RDS_CONFIG

Configures RDS settings to enable RDS processing (RDSEN) and set RDS block error thresholds. When a RDS Group is received, all block errors must be less than or equal the associated block error threshold for the group to be stored in the RDS FIFO. If blocks with errors are permitted into the FIFO, the block error information can be reviewed when the group is read using the FM_RDS_STATUS command. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 0x0000.

Note: FM_RDS_CONFIG is supported in FMRX component 2.0 or later.

Available in: Si4705/06, Si4721, Si4731/32/35/37/39, Si4741/43/45/49

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	BLETHA[1:0]		BLETHB[1:0]		BLETHC[1:0]		BLETHD[1:0]		0	0	0	0	0	0	0	RDSEN

Bit	Name	Function
15:14	BLETHA[1:0]	**Block Error Threshold BLOCKA.** 0 = No errors. 1 = 1–2 bit errors detected and corrected. 2 = 3–5 bit errors detected and corrected. 3 = Uncorrectable.
13:12	BLETHB[1:0]	**Block Error Threshold BLOCKB.** 0 = No errors. 1 = 1–2 bit errors detected and corrected. 2 = 3–5 bit errors detected and corrected. 3 = Uncorrectable.
11:10	BLETHC[1:0]	**Block Error Threshold BLOCKC.** 0 = No errors. 1 = 1–2 bit errors detected and corrected. 2 = 3–5 bit errors detected and corrected. 3 = Uncorrectable.
9:8	BLETHD[1:0]	**Block Error Threshold BLOCKD.** 0 = No errors. 1 = 1–2 bit errors detected and corrected. 2 = 3–5 bit errors detected and corrected. 3 = Uncorrectable.
0	RDSEN	**RDS Processing Enable.** 1 = RDS processing enabled.

Recommended Block Error Threshold options:

2,2,2,2 = No group stored if any errors are uncorrected.

3,3,3,3 = Group stored regardless of errors.

0,0,0,0 = No group stored containing corrected or uncorrected errors.

3,2,3,3 = Group stored with corrected errors on B, regardless of errors on A, C, or D.

Property 0x1503. FM_RDS_CONFIDENCE

Selects the confidence level requirement for each RDS block. A higher confidence requirement will result in fewer decoder errors (% of blocks with BLE<3 that contains incorrect information) but more block errors (% of blocks with BLE=3). The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 0x1111.

Available in: Si4706-C30 and later, Si474x, Si4704/05/30/31/34/35/84/85-D50 and later, Si4732

Default: 0x1111

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	X	X	X	X	CONFIDENCEB[3:0]				CONFIDENCEC[3:0]				CONFIDENCED[3:0]			

Bit	Name	Function
11:8	CONFIDENCEB	Selects decoder error rate threshold for Block B.
7:4	CONFIDENCEC	Selects decoder error rate threshold for Block C.
3:0	CONFIDENCED	Selects decoder error rate threshold for Block D.

Property 0x1700. FM_AGC_ATTACK_RATE

Sets the AGC attack rate. Larger values provide slower attack and smaller values provide faster attack. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 4 (approximately 1500 dB/s).

$$\text{AGC Attack Rate (dB/s)} = \frac{6000}{\text{ATTACK}[7:0]}$$

Nominal “6000” is based on 50 Ω source impedance and will vary with source impedance. In most systems, an exact value is not important. However, to calculate for a different source impedance, perform the following steps:

1. Drive antenna input with desired source impedance (via antenna or antenna dummy).
2. Increase RF level until AGC index changes from 0 to 1. Record last RF level with index equal 0.
3. Increase RF level until AGC index reaches 20. Record RF level with index equal 20.
4. Replace “6000” in rate equation with “(RF20 – RF0)/0.00667”.

Available in: Si4740/41/42/43/44/45/49

Default: 0x0004

Step: 4

Range: 4–248

Note: Was property 0x4100 in FW2.B.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	ATTACK[7:0]							

Property 0x1701. FM_AGC_RELEASE_RATE

Sets the AGC release rate. Larger values provide slower release and smaller values provide faster release. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 140 (approximately 43 dB/s).

$$\text{AGC Release Rate (dB/s)} = \frac{6000}{\text{RELEASE}[7:0]}$$

Nominal “6000” is based on 50 Ω source impedance and will vary with source impedance. In most systems, an exact value is not important. However, to calculate for a different source impedance, perform the following steps:

1. Drive antenna input with desired source impedance (via antenna or antenna dummy).
2. Increase RF level until AGC index changes from 0 to 1. Record last RF level with index equal 0.
3. Increase RF level until AGC index reaches 20. Record RF level with index equal 20.
4. Replace “6000” in rate equation with “(RF20 – RF0)/0.00667”.

Available in: Si4740/41/42/43/44/45/49

Default: 0x008C

Step: 4

Range: 4–248

Note: Was property 0x4101 in FW2.B.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	RELEASE[7:0]							

Property 0x1800. FM_BLEND_RSSI_STEREO_THRESHOLD

Sets RSSI threshold for stereo blend (Full stereo above threshold, blend below threshold). To force stereo, set to 0. To force mono, set to 127. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 49 dBµV.

Available in: Si4706-C30 and later, Si4740/41/42/43/44/45, Si4704/05/30/31/34/35/84/85-D50 and later, Si4732

Default: 0x0031

Units: dBµV

Step: 1

Range: 0–127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	STRTHRESH[6:0]						

Property 0x1801. FM_BLEND_RSSI_MONO_THRESHOLD

Sets RSSI threshold for mono blend (Full mono below threshold, blend above threshold). To force stereo, set this to 0. To force mono, set this to 127. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 30 dBµV.

Available in: Si4706-C30 and later, Si4740/41/42/43/44/45, Si4704/05/30/31/34/35/84/85-D50 and later, Si4732

Default: 0x001E

Units: dBµV

Step: 1

Range: 0–127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	MONOTHRESH[6:0]						

Property 0x1802. FM_BLEND_RSSI_ATTACK_RATE

Sets the stereo to mono attack rate for RSSI based blend. Smaller values provide slower attack and larger values provide faster attack. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 4000 (approximately 16 ms). ATTACK[15:0] = 65536/time, where time is the desired transition time in ms.

Available in: Si4706-C30 and later, Si4740/41/42/43/44/45, Si4704/05/30/31/34/35/84/85-D50 and later, Si4732

Default: 0x0FA0

Step: 1

Range: 0 (disabled), 1–32767

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ATTACK[15:0]															

Property 0x1803. FM_BLEND_RSSI_RELEASE_RATE

Sets the mono to stereo release rate for RSSI based blend. Smaller values provide slower release and larger values provide faster release. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 400 (approximately 164 ms). RELEASE[15:0] = 65536/time, where time is the desired transition time in ms.

Available in: Si4706-C30 and later, Si4740/41/42/43/44/45, Si4704/05/30/31/34/35/84/85-D50 and later, Si4732

Default: 0x0190

Step: 1

Range: 0 (disabled), 1–32767

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RELEASE[15:0]															

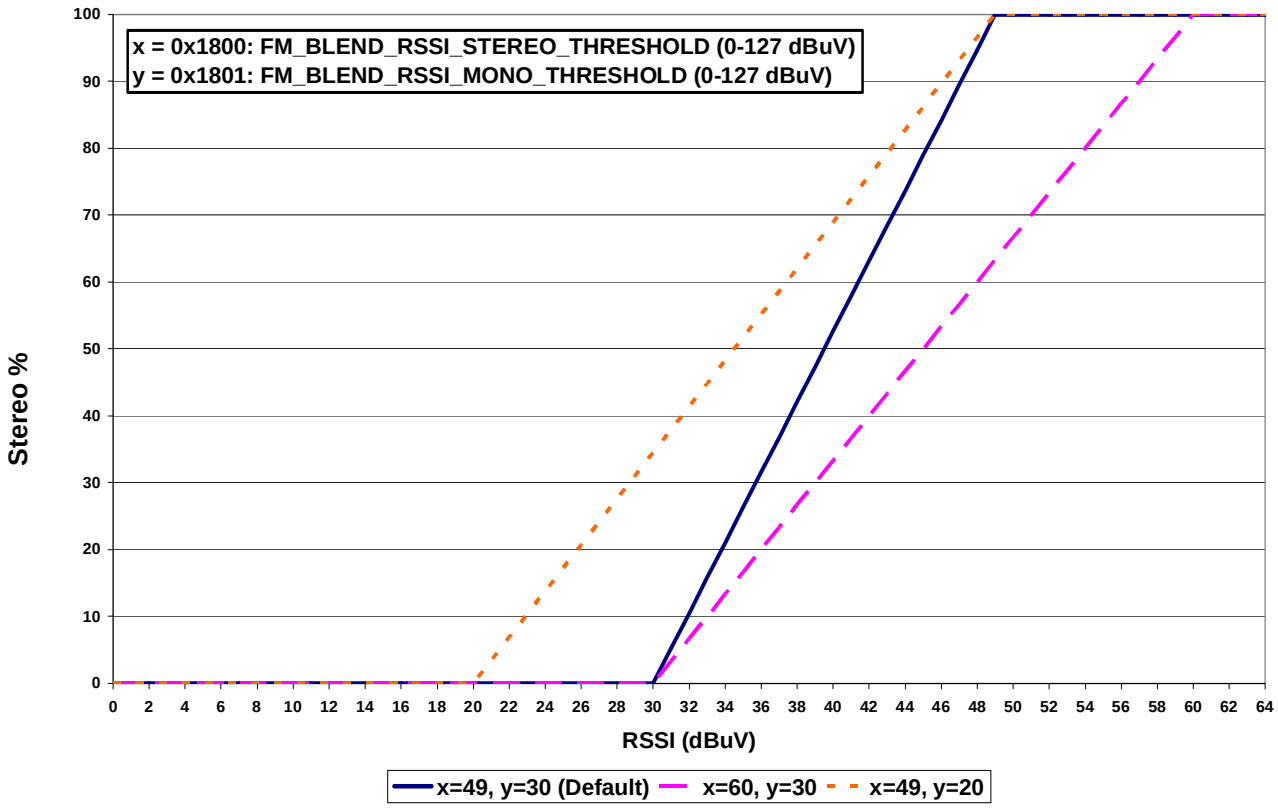


Figure 4. RSSI Blend

Property 0x1804. FM_BLEND_SNR_STEREO_THRESHOLD

Sets SNR threshold for stereo blend (Full stereo above threshold, blend below threshold). To force stereo, set this to 0. To force mono, set this to 127. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 27 dB.

Available in: Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732

Default: 0x001B

Units: dB

Step: 1

Range: 0–127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	STRTHRESH[6:0]						

Property 0x1805. FM_BLEND_SNR_MONO_THRESHOLD

Sets SNR threshold for mono blend (Full mono below threshold, blend above threshold). To force stereo, set to 0. To force mono, set to 127. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 14 dB.

Available in: Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732

Default: 0x000E

Units: dB

Step: 1

Range: 0–127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	MONOTHRESH[6:0]						

Property 0x1806. FM_BLEND_SNR_ATTACK_RATE

Sets the stereo to mono attack rate for SNR based blend. Smaller values provide slower attack and larger values provide faster attack. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 4000 (approximately 16 ms). ATTACK[15:0] = 65536/time, where time is the desired transition time in ms.

Available in: Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732

Default: 0x0FA0

Step: 1

Range: 0 (disabled), 1–32767

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ATTACK[15:0]															

Property 0x1807. FM_BLEND_SNR_RELEASE_RATE

Sets the mono to stereo release rate for SNR based blend. Smaller values provide slower release and larger values provide faster release. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 400 (approximately 164 ms). RELEASE[15:0] = 65536/time, where time is the desired transition time in ms.

Available in: Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732

Default: 0x0190

Step: 1

Range: 0 (disabled), 1–32767

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RELEASE[15:0]															

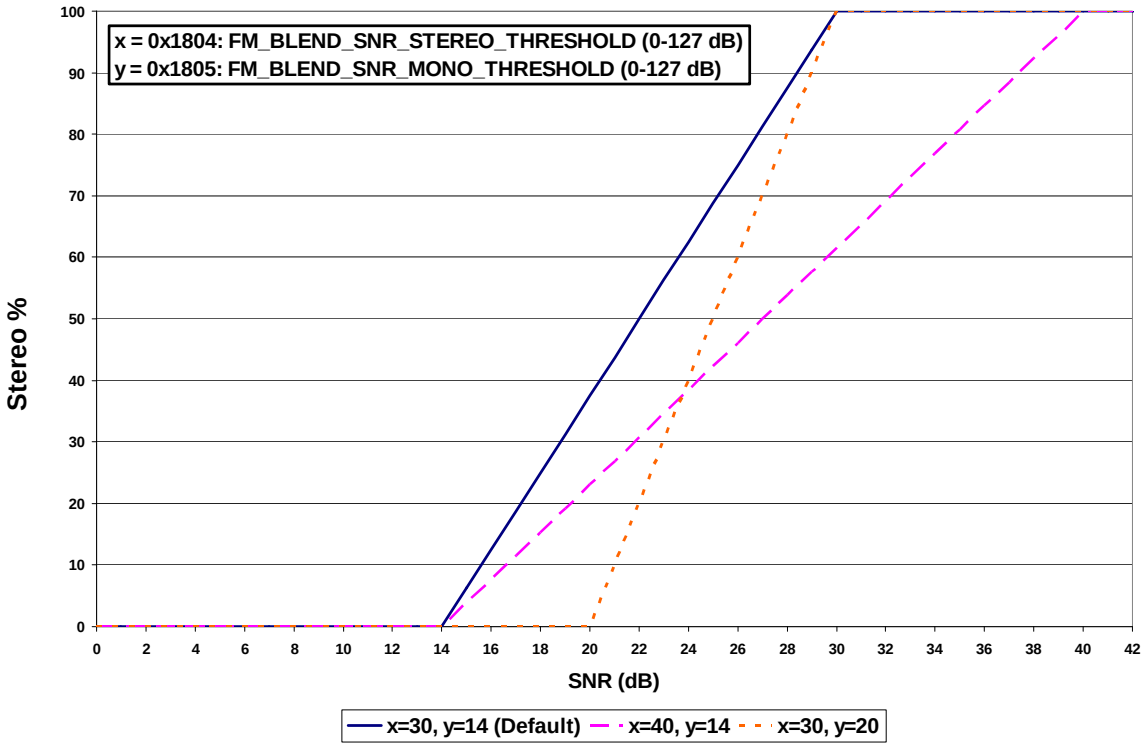


Figure 5. SNR Blend

Property 0x1808. FM_BLEND_MULTIPATH_STEREO_THRESHOLD

Sets Multipath threshold for stereo blend (Full stereo below threshold, blend above threshold). To force stereo, set to 100. To force mono, set to 0. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 20.

Available in: Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732

Default: 0x0014

Step: 1

Range: 0–100

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	STRTHRESH[6:0]						

Property 0x1809. FM_BLEND_MULTIPATH_MONO_THRESHOLD

Sets Multipath threshold for mono blend (Full mono above threshold, blend below threshold). To force stereo, set to 100. To force mono, set to 0. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 60.

Available in: Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732

Default: 0x003C

Step: 1

Range: 0–100

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	MONOTHRESH[6:0]						

Property 0x180A. FM_BLEND_MULTIPATH_ATTACK_RATE

Sets the stereo to mono attack rate for Multipath based blend. Smaller values provide slower attack and larger values provide faster attack. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 4000 (approximately 16 ms). ATTACK[15:0] = 65536/time, where time is the desired transition time in ms.

Available in: Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732

Default: 0x0FA0

Step: 1

Range: 0 (disabled), 1–32767

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ATTACK[15:0]															

Property 0x180B. FM_BLEND_MULTIPATH_RELEASE_RATE

Sets the mono to stereo release rate for Multipath based blend. Smaller values provide slower release and larger values provide faster release. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 40 (approximately 1.64 s). RELEASE[15:0] = 65536/time, where time is the desired transition time in ms.

Available in: Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732

Default: 0x0028

Step: 1

Range: 0 (disabled), 1–32767

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RELEASE[15:0]															

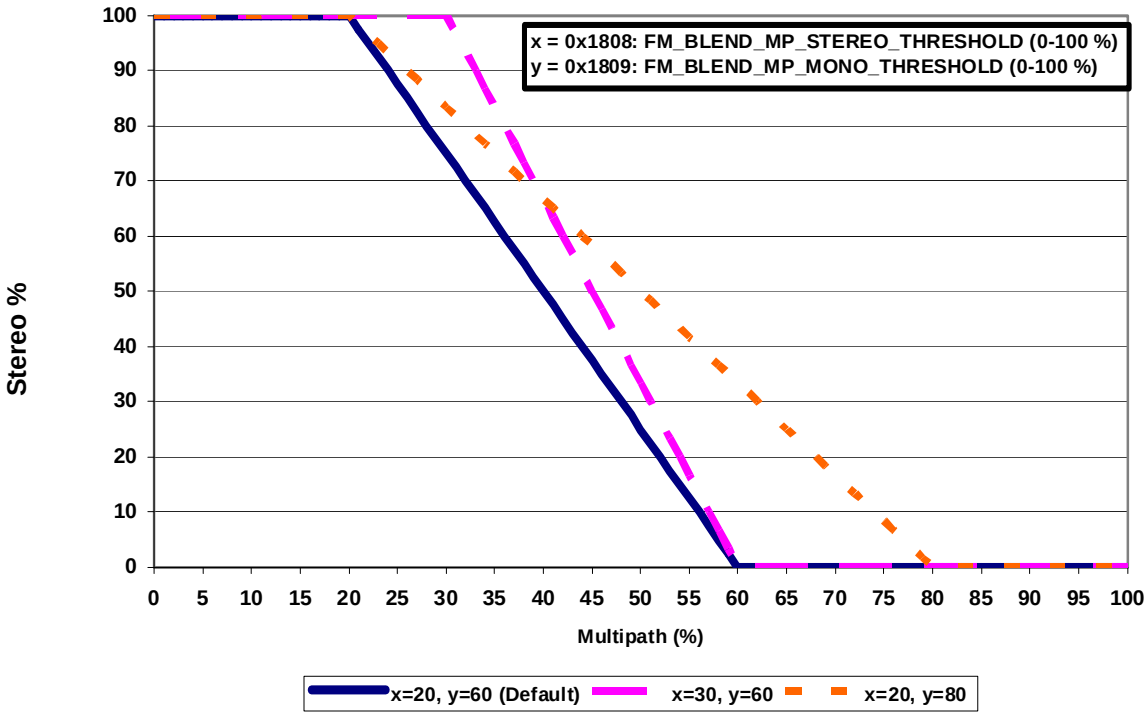


Figure 6. MP Blend

Property 0x180C. FM_BLEND_MAX_STEREO_SEPARATION

Sets the maximum allowable stereo separation. The default is 0, disabling the feature so that there is no limit on stereo separation.

Available in: Si474x

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	MAX_SEP[2:0]		

Bit	Name	Function
15:3	Reserved	Always write to 0.
2:0	MAX_SEP	**Maximum Stereo Separation.** 0 = disabled (default) 1 = 12 dB of separation, maximum 2 = 15 dB of separation, maximum 3 = 18 dB of separation, maximum 4 = 21 dB of separation, maximum 5 = 24 dB of separation, maximum 6 = 27 dB of separation, maximum 7 = 30 dB of separation, maximum

Property 0x1900. FM_NB_DETECT_THRESHOLD

Sets the threshold for detecting impulses in dB above the noise floor. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 16 dB. To disable the noise blanker feature, set the FM_NB_DETECT_THRESHOLD property (0x1900) to 0.

Available in: Si4742/43/44/45

Default: 0x0010

Range: 0–90

Note: Was property 0x4106 in FW2.B.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	NB_DETECT_THRESHOLD [15:0]															

Property 0x1901. FM_NB_INTERVAL

Interval in micro-seconds that original samples are replaced by interpolated clean samples. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 24 µs.

Available in: Si4742/43/44/45

Default: 0x0018

Range: 8–48

Note: Was property 0x4107 in FW2.B.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	NB_INTERVAL [15:0]															

Property 0x1902. FM_NB_RATE

Noise blanking rate in 100 Hz units. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 64 (6400 Hz).

Available in: Si4742/43/44/45

Default: 0x0040

Range: 1–64

Note: Was property 0x4108 in FW2.B.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	NB_RATE [15:0]															

Property 0x1903. FM_NB_IIR_FILTER

Sets the bandwidth of the noise floor estimator. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 300 (465 Hz).

Bandwidth (Hz) = NB_IIR_FILTER[15:0] x 1.55

Available in: Si4742/43/44/45

Default: 0x012C

Range: 300–1600

Note: Was property 0x4109 in FW2.B.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	NB_IIR_FILTER [15:0]															

Property 0x1904. FM_NB_DELAY

Delay in micro-seconds before applying impulse blanking to the original samples. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 170 µs.

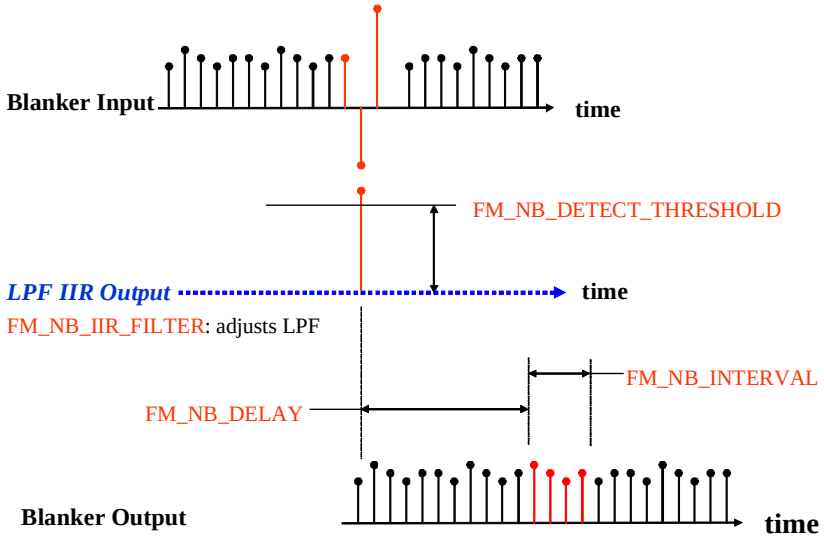
Available in: Si4742/43/44/45

Default: 0x00AA

Range: 125–219

Note: Was property 0x410A in FW2.B.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	NB_DELAY [15:0]															



FM_NB_RATE: sets maximum repeat rate NB is allowed to fire.

Figure 7. FM Noise Blanker

Property 0x1A00. FM_HICUT_SNR_HIGH_THRESHOLD

Sets the SNR level at which hi-cut begins to band limit. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read in POWERUP mode. The default is 24 dB.

Available in: Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732

Default: 0x0018

Range: 0–127

Note: Was property 0x180C in FW2.B.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	SNR_HIGH[6:0]						

Property 0x1A01. FM_HICUT_SNR_LOW_THRESHOLD

Sets the SNR level at which hi-cut reaches maximum band limiting. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read in POWERUP mode. The default is 15 dB.

Available in: Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732

Default: 0x000F

Range: 0–127

Note: Was property 0x180D in FW2.B.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	SNR_LOW[6:0]						

Property 0x1A02. FM_HICUT_ATTACK_RATE

Sets the rate at which hi-cut lowers the transition frequency. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read in POWERUP mode. The default is 20000 (approximately 3 ms).

ATTACK[15:0] = 65536/time, were time is the desired transition time in ms.

Available in: Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732

Default: 0x4E20

Range: 0 (disabled), 1–32767

Note: Was property 0x180E in FW2.B.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ATTACK[15:0]															

Property 0x1A03. FM_HICUT_RELEASE_RATE

Sets the rate at which hi-cut increases the transition frequency. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read in POWERUP mode. The default is 20 (approximately 3.3 s).

RELEASE[15:0] = 65536/time, were time is the desired transition time in ms.

Available in: Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732

Default: 0x0014

Range: 0 (disabled), 1–32767

Note: Was property 0x180F in FW2.B.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RELEASE[15:0]															

Property 0x1A04. FM_HICUT_MULTIPATH_TRIGGER_THRESHOLD

Sets the MULTIPATH level at which hi-cut begins to band limit. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read in POWERUP mode. The default is 20%.

Available in: Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732

Default: 0x0014

Range: 0–100

Note: Was property 0x1810 in FW2.B.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	MULT_TRIGGER[6:0]						

Property 0x1A05. FM_HICUT_MULTIPATH_END_THRESHOLD

Sets the MULTIPATH level at which hi-cut reaches maximum band limiting. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read in POWERUP mode. The default is 60%.

Available in: Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732

Default: 0x003C

Range: 0–100

Note: Was property 0x1811 in FW2.B.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	MULT_END[6:0]						

Property 0x1A06. FM_HICUT_CUTOFF_FREQUENCY

Sets the maximum band limit frequency for hi-cut and also sets the maximum audio frequency. The CTS bit (optional interrupt) is set when it is safe to send the next command. This property may only be set or read in POWERUP mode. The default is 0(disabled).

Available in: Si4740/41/42/43/44/45, Si4704/05-D50 and later, Si4706-C30 and later, Si4730/31/34/35/84/85-D50 and later, Si4732

Default 0x0000

Range: 0–7 (maximum band limit frequency for Hi-Cut)

0–7 (maximum audio frequency)

Note: Was property 0x1812 in FW2.B. The maximum audio frequency was not programmable in FW2.B.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	MAXIMUM AUDIO FREQ[2:0]			0	FREQUENCY[2:0]		

Bit	Name	Function
6:4	MAXIMUM AUDIO FREQUENCY[2:0]	**Maximum Audio Frequency.** 0 = Maximum Audio transition frequency = Max Audio BW 1 = Maximum Audio transition frequency = 2 kHz 2 = Maximum Audio transition frequency = 3 kHz 3 = Maximum Audio transition frequency = 4 kHz 4 = Maximum Audio transition frequency = 5 kHz 5 = Maximum Audio transition frequency = 6 kHz 6 = Maximum Audio transition frequency = 8 kHz 7 = Maximum Audio transition frequency = 11 kHz
2:0	FREQUENCY[2:0]	**Frequency.** 0 = Hi-Cut disabled 1 = Hi-cut transition frequency = 2 kHz 2 = Hi-cut transition frequency = 3 kHz 3 = Hi-cut transition frequency = 4 kHz 4 = Hi-cut transition frequency = 5 kHz 5 = Hi-cut transition frequency = 6 kHz 6 = Hi-cut transition frequency = 8 kHz 7 = Hi-cut transition frequency = 11 kHz

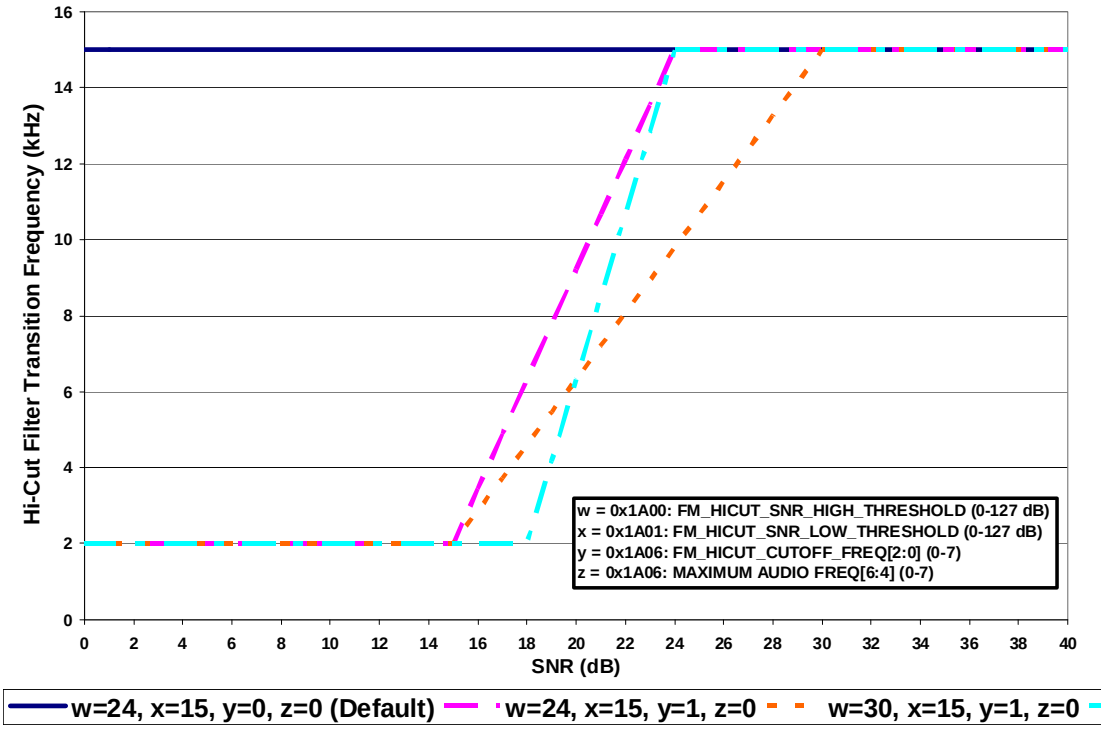


Figure 8. HiCut Controlled by SNR Metric

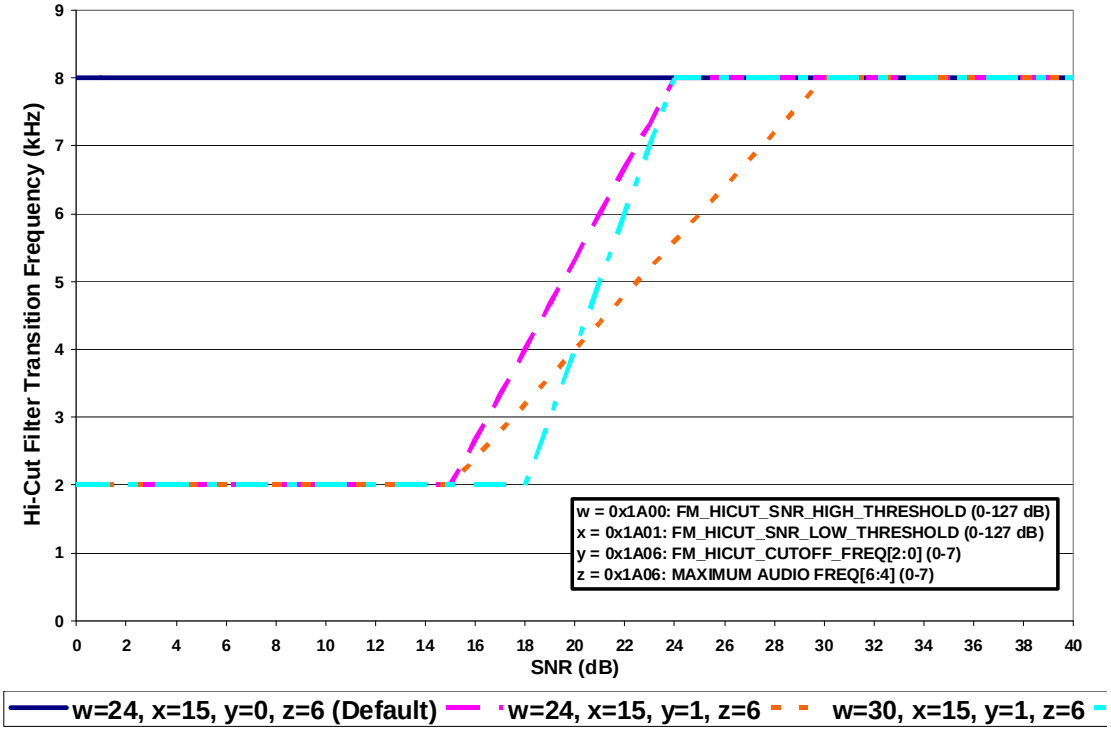


Figure 9. HiCut Controlled by SNR Metric with Maximum Audio Frequency 8 kHz

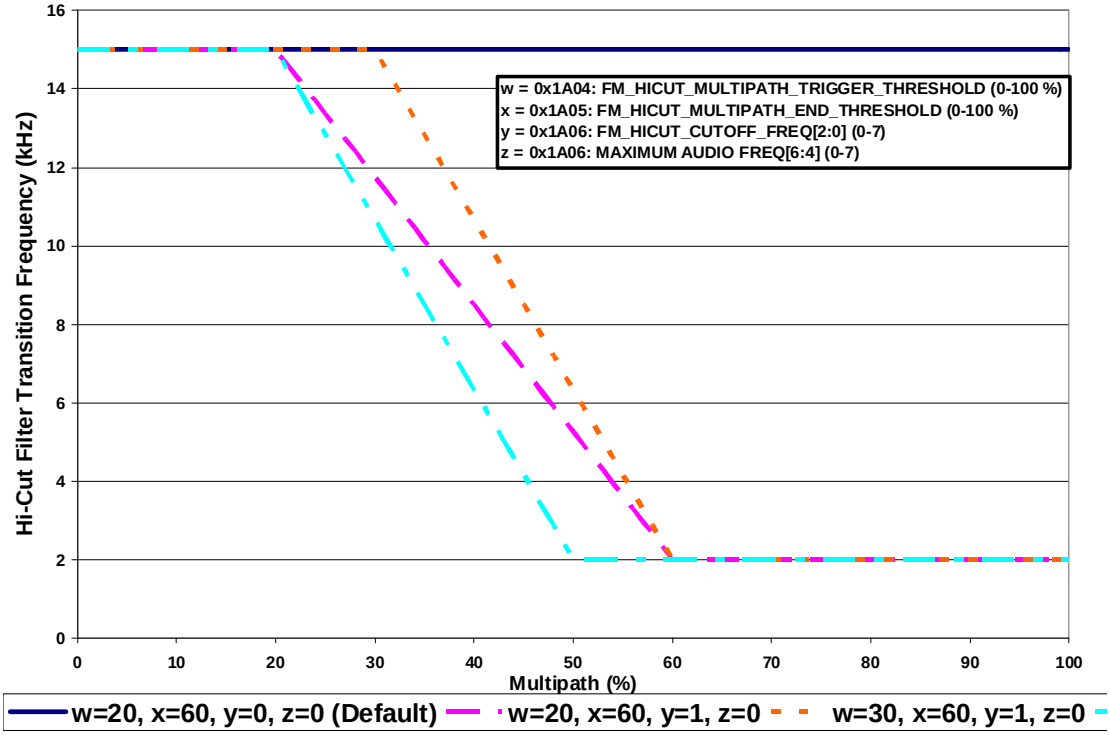


Figure 10. HiCut Controlled by Multipath Metric

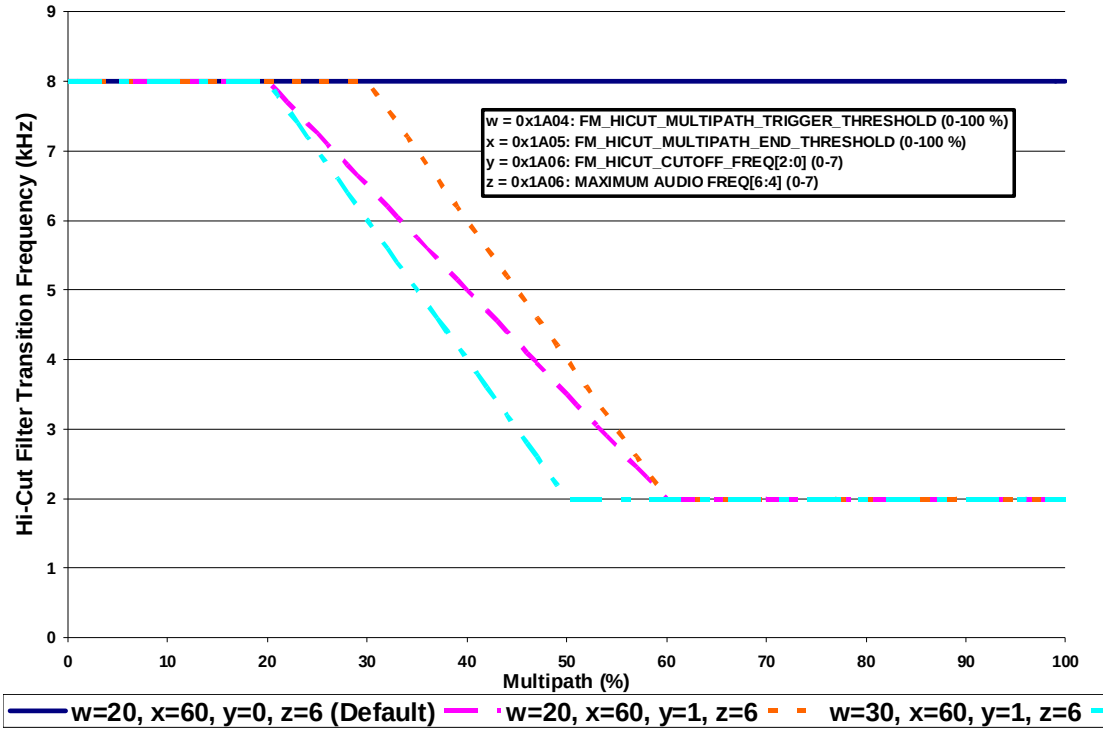


Figure 11. HiCut Controlled by Multipath Metric with Maximum Audio Frequency 8 kHz

Property 0x4000. RX_VOLUME

Sets the audio output volume. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 63.

Available in: All except Si4749

Default: 0x003F

Step: 1

Range: 0–63

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	VOL[5:0]					

Bit	Name	Function
15:6	Reserved	Always write to 0.
5:0	VOL	**Output Volume.** Sets the output volume level, 63 max, 0 min. Default is 63.

Property 0x4001. RX_HARD_MUTE

Mutes the audio output. L and R audio outputs may be muted independently. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is unmute (0x0000).

Available in: All except Si4749

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LMUTE	RMUTE

Bit	Name	Function
15:2	Reserved	Always write to 0.
1	LMUTE	Mutes L Audio Output.
0	RMUTE	Mutes R Audio Output.

5.3. Commands and Properties for the AM/SW/LW Receiver (Si4730/31/32/34/35/36/37/40/41/42/43/44/45)

AM (Medium Wave), SW (Short Wave), and LW (Long Wave) use the same AM_SW_LW component, thus the commands and properties for these functions are the same. For simplicity reason, the commands and properties only have a prefix AM instead of AM_SW_LW. The main difference among AM, SW, and LW is on the frequency range.

The common frequency range and spacing for AM/SW/LW are:

- SW 2.3 MHz to 23 MHz in 5 kHz frequency spacing
- AM in US 520 kHz to 1.71 MHz in 10 kHz frequency spacing
- AM in Asia 522 kHz to 1.71 MHz in 9 kHz frequency spacing
- LW 153 kHz to 279 kHz in 9 kHz frequency spacing

Tables 12 and 13 summarize the commands and properties for the AM/SW/LW Receiver components applicable to Si473x/4x.

Table 12. AM/LW/SW Receiver Command Summary

Cmd	Name	Description	Available In
0x01	POWER_UP	Power up device and mode selection.	All
0x10	GET_REV	Returns revision information on the device.	All
0x11	POWER_DOWN	Power down device.	All
0x12	SET_PROPERTY	Sets the value of a property.	All
0x13	GET_PROPERTY	Retrieves a property's value.	All
0x14	GET_INT_STATUS	Read interrupt status bits.	All
0x15	PATCH_ARGS*	Reserved command used for patch file downloads.	All
0x16	PATCH_DATA*	Reserved command used for patch file downloads.	All
0x40	AM_TUNE_FREQ	Tunes to a given AM frequency.	All
0x41	AM_SEEK_START	Begins searching for a valid frequency.	All
0x42	AM_TUNE_STATUS	Queries the status of the already issued AM_TUNE_FREQ or AM_SEEK_START command.	All
0x43	AM_RSQ_STATUS	Queries the status of the Received Signal Quality (RSQ) for the current channel.	All
0x47	AM_AGC_STATUS	Queries the current AGC settings.	All
0x48	AM_AGC_OVERRIDE	Overrides AGC settings by disabling and forcing it to a fixed value.	All
0x80	GPIO_CTL	Configures GPO1, 2, and 3 as output or Hi-Z.	All
0x81	GPIO_SET	Sets GPO1, 2, and 3 output level (low or high).	All

***Note:** Commands PATCH_ARGS and PATCH_DATA are only used to patch firmware. For information on applying a patch file, see "7.2. Powerup from a Component Patch" on page 233.

Table 13. AM/SW/LW Receiver Property Summary

Prop	Name	Description	Default	Available In
0x0001	GPO_IEN	Enables interrupt sources.	0x0000	All
0x0102	DIGITAL_OUTPUT_FORMAT	Configure digital audio outputs	0x0000	Si4705/06, Si4731/35/37/39, Si4730/34/36/38-D60 and later, Si4732, Si4741/43/45, Si4784/85
0x0104	DIGITAL_OUTPUT_SAMPLE_RATE	Configure digital audio output sample rate	0x0000	Si4705/06, Si4731/35/37/39, Si4730/34/36/38-D60 and later, Si4732, Si4741/43/45, Si4784/85
0x0201	REFCLK_FREQ	Sets frequency of reference clock in Hz. The range is 31130 to 34406 Hz, or 0 to disable the AFC. Default is 32768 Hz.	0x8000	All
0x0202	REFCLK_PRESCALE	Sets the prescaler value for RCLK input.	0x0001	All
0x3100	AM_DEEMPHASIS	Sets deemphasis time constant. Can be set to 50 µs. Deemphasis is disabled by default.	0x0000	All
0x3102	AM_CHANNEL_FILTER[1]	Selects the bandwidth of the channel filter for AM reception. The choices are 6, 4, 3, 2, 2.5, 1.8, or 1 (kHz). The default bandwidth is 2 kHz.	0x0003	All
0x3103	AM_AUTOMATIC_VOLUME_CONTROL_MAX_GAIN	Sets the maximum gain for automatic volume control.	0x1543	Si473x-C40 and later, Si4732
			0x7800	Si474x
0x3104	AM_MODE_AFC_SW_PULL_IN_RANGE	Sets the SW AFC pull-in range.	0x21F7	Si4734/35-C40 and later, Si4732, Si4742/43/44/45
0x3105	AM_MODE_AFC_SW_LOCK_IN_RANGE	Sets the SW AFC lock-in.	0x2DF5	Si4734/35-C40 and later, Si4732, Si4742/43/44/45

Notes:

1. The 1 kHz option, 1.8 kHz option, and 100 Hz high-pass Line Noise Rejection filter are supported on Si473x-C40 and later devices and Si4732 devices and Si474x devices (AM_SW_LW component 3.0 or later).
   The 2.5 kHz option is supported on Si473x-C40 and later devices and Si4732 devices (AM_SW_LW component 5.0 or later).
2. Component 1.0 incorrectly reports 0x06B9 (1721 kHz) as default for AM_SEEK_BAND_TOP. After POWER_UP command is complete, set AM_SEEK_BAND_TOP to 0x06AE (1710 kHz) using the SET_PROPERTY command.

Table 13. AM/SW/LW Receiver Property Summary (Continued)

Prop	Name	Description	Default	Available In
0x3200	AM_RSQ_INTERRUPTS	Configures interrupt related to Received Signal Quality metrics. All interrupts are disabled by default.	0x0000	All
0x3201	AM_RSQ_SNR_HIGH_THRESHOLD	Sets high threshold for SNR interrupt.	0x007F	All
0x3202	AM_RSQ_SNR_LOW_THRESHOLD	Sets low threshold for SNR interrupt.	0x0000	All
0x3203	AM_RSQ_RSSI_HIGH_THRESHOLD	Sets high threshold for RSSI interrupt.	0x007F	All
0x3204	AM_RSQ_RSSI_LOW_THRESHOLD	Sets low threshold for RSSI interrupt.	0x0000	All
0x3300	AM_SOFT_MUTE_RATE	Sets the attack and decay rates when entering or leaving soft mute. The default is 278 dB/s.	0x0040	All
0x3301	AM_SOFT_MUTE_SLOPE	Sets the AM soft mute slope. Default value is a slope of 1.	0x0002	Si4730/31/34/35/36/37-B20 and earlier, Si4740/41/42/43/44/45-C10 and earlier
			0x0001	All others
0x3302	AM_SOFT_MUTE_MAX_ATTENUATION	Sets maximum attenuation during soft mute (dB). Set to 0 to disable soft mute. Default is 8 dB.	0x0010	Si4730/31/34/35/36/37-B20 and earlier, Si4740/41/42/43/44/45-C10 and earlier
			0x0008	All others
0x3303	AM_SOFT_MUTE_SNR_THRESHOLD	Sets SNR threshold to engage soft mute. Default is 8 dB.	0x000A	Si4730/31/34/35/36/37-B20 and earlier, Si4740/41/42/43/44/45-C10 and earlier
			0x0008	All others

Notes:

1. The 1 kHz option, 1.8 kHz option, and 100 Hz high-pass Line Noise Rejection filter are supported on Si473x-C40 and later devices and Si4732 devices and Si474x devices (AM_SW_LW component 3.0 or later).
   The 2.5 kHz option is supported on Si473x-C40 and later devices and Si4732 devices (AM_SW_LW component 5.0 or later).
2. Component 1.0 incorrectly reports 0x06B9 (1721 kHz) as default for AM_SEEK_BAND_TOP. After POWER_UP command is complete, set AM_SEEK_BAND_TOP to 0x06AE (1710 kHz) using the SET_PROPERTY command.

Table 13. AM/SW/LW Receiver Property Summary (Continued)

Prop	Name	Description	Default	Available In
0x3304	AM_SOFT_MUTE_ RELEASE_RATE	Sets softmute release rate. Smaller values provide slower release, and larger values provide faster release. The default is 8192 (approximately 8000 dB/s).	0x2000	Si4740/41/42/43/ 44/45
0x3305	AM_SOFT_MUTE_ ATTACK_RATE	Sets software attack rate. Smaller values provide slower attack, and larger values provide faster attack. The default is 8192 (approximately 8000 dB/s).	0x2000	Si4740/41/42/43/ 44/45
0x3400	AM_SEEK_BAND_ BOTTOM	Sets the bottom of the AM band for seek. Default is 520.	0x0208	All
0x3401	AM_SEEK_BAND_TOP[2]	Sets the top of the AM band for seek. Default is 1710.	0x06AE	All
0x3402	AM_SEEK_FREQ_ SPACING	Selects frequency spacing for AM seek. Default is 10 kHz spacing.	0x000A	All
0x3403	AM_SEEK_SNR_ THRESHOLD	Sets the SNR threshold for a valid AM Seek/Tune. If the value is zero then SNR threshold is not considered when doing a seek. Default value is 5 dB.	0x0005	All
0x3404	AM_SEEK_RSSI_ THRESHOLD	Sets the RSSI threshold for a valid AM Seek/Tune. If the value is zero then RSSI threshold is not considered when doing a seek. Default value is 25 dBµV.	0x0019	All
0x3702	AM_AGC_ATTACK_ RATE	Sets the number of milliseconds the high peak detector must be exceeded before decreasing gain. Default value is 4 (approximately 1400 dB/s).	0x0004	Si4740/41/42/43/ 44/45
0x3703	AM_AGC_RELEASE_RA TE	Sets the number of milliseconds the low peak detector must not be exceeded before increasing the gain. Default value is 140 (approximately 40 dB/s).	0x008C	Si4740/41/42/43/ 44/45
0x3705	AM_FRONTEND_AGC_ CONTROL	Adjusts AM AGC for frontend (external) attenuator and LNA. (Si4740/41/42/43/44/45 only)	0x130C	Si4740/41/42/43/ 44/45
0x3900	AM_NB_DETECT_ THRESHOLD	Sets the threshold for detecting impulses in dB above the noise floor. Default value is 12.	0x000C	Si4742/43/44/45
0x3901	AM_NB_INTERVAL	Interval in micro-seconds that original samples are replaced by interpolated clean samples. Default value is 55 µs.	0x0037	Si4742/43/44/45
0x3902	AM_NB_RATE	Noise blanking rate in 100 Hz units. Default value is 64.	0x0040	Si4742/43/44/45

Notes:

1. The 1 kHz option, 1.8 kHz option, and 100 Hz high-pass Line Noise Rejection filter are supported on Si473x-C40 and later devices and Si4732 devices and Si474x devices (AM_SW_LW component 3.0 or later).
   The 2.5 kHz option is supported on Si473x-C40 and later devices and Si4732 devices (AM_SW_LW component 5.0 or later).
2. Component 1.0 incorrectly reports 0x06B9 (1721 kHz) as default for AM_SEEK_BAND_TOP. After POWER_UP command is complete, set AM_SEEK_BAND_TOP to 0x06AE (1710 kHz) using the SET_PROPERTY command.

Table 13. AM/SW/LW Receiver Property Summary (Continued)

Prop	Name	Description	Default	Available In
0x3903	AM_NB_IIR_FILTER	Sets the bandwidth of the noise floor estimator. Default value is 300.	0x012C	Si4742/43/44/45
0x3904	AM_NB_DELAY	Delay in micro-seconds before applying impulse blanking to the original samples. Default value is 172.	0x00AC	Si4742/43/44/45
0x4000	RX_VOLUME	Sets the output volume.	0x003F	All
0x4001	RX_HARD_MUTE	Mutes the L and R audio outputs.	0x0000	All

Notes:

1. The 1 kHz option, 1.8 kHz option, and 100 Hz high-pass Line Noise Rejection filter are supported on Si473x-C40 and later devices and Si4732 devices and Si474x devices (AM_SW_LW component 3.0 or later).
   The 2.5 kHz option is supported on Si473x-C40 and later devices and Si4732 devices (AM_SW_LW component 5.0 or later).
2. Component 1.0 incorrectly reports 0x06B9 (1721 kHz) as default for AM_SEEK_BAND_TOP. After POWER_UP command is complete, set AM_SEEK_BAND_TOP to 0x06AE (1710 kHz) using the SET_PROPERTY command.

Table 14. Status Response for the AM/SW/LW Receiver

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	X	X	STCINT

Bit	Name	Function
7	CTS	**Clear to Send.** 0 = Wait before sending next command. 1 = Clear to send next command.
6	ERR	**Error.** 0 = No error 1 = Error
5:4	Reserved	Values may vary.
3	RSQINT	**Received Signal Quality Interrupt.** 0 = Received Signal Quality measurement has not been triggered. 1 = Received Signal Quality measurement has been triggered.
2:1	Reserved	Values may vary.
0	STCINT	**Seek/Tune Complete Interrupt.** 0 = Tune complete has not been triggered. 1 = Tune complete has been triggered.

5.3.1. AM/SW/LW Receiver Commands

Command 0x01. POWER_UP

Initiates the boot process to move the device from powerdown to powerup mode. The boot can occur from internal device memory or a system controller downloaded patch. To confirm that the patch is compatible with the internal device library revision, the library revision should be confirmed by issuing the POWER_UP command with FUNC = 15 (query library ID). The device returns the response, including the library revision, and then moves into powerdown mode. The device can then be placed in powerup mode by issuing the POWER_UP command with FUNC = 1 (AM/SW/LW Receive) and the patch may be applied. See Section "7.2. Powerup from a Component Patch" on page 233 for more information.

The POWER_UP command configures the state of ROUT (pin 13, Si4732 pin 16) and LOUT (pin 14, Si4732 pin 1) for analog audio mode and GPO2/INT (pin 18, Si4732 pin 3) for interrupt operation. For the Si4731/32/35/37, the POWER_UP command also configures the state of GPO3/DCLK (pin 17, Si4732 pin 2), DFS (pin 16, Si4732 pin 1), and DOUT (pin 15, Si4732 pin 16) for digital audio mode. The command configures GPO2/INT interrupts (GPO2OEN) and CTS interrupts (CTSIEN). If both are enabled, GPO2/INT is driven high during normal operation and low for a minimum of 1 µs during the interrupt. The CTSIEN bit is duplicated in the GPO_IEN property. The command is complete when the CTS bit (and optional interrupt) is set.

Note: To change function (e.g. AM/SW/LW RX to FM RX), issue POWER_DOWN command to stop current function; then, issue POWER_UP to start new function.

Note: Delay at least 500 ms between powerup command and first tune command to wait for the oscillator to stabilize if XOSCEN is set and crystal is used as the RCLK.

Available in: All

Command Arguments: Two

Response Bytes: None (FUNC = 1), Seven (FUNC = 15)

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	0	0	0	0	1
ARG1	CTSIEN	GPO2OEN	PATCH	XOSCEN	FUNC[3:0]			
ARG2	OPMODE[7:0]							

ARG	Bit	Name	Function
1	7	CTSIEN	**CTS Interrupt Enable.** 0 = CTS interrupt disabled. 1 = CTS interrupt enabled.
1	6	GPO2OEN	**GPO2 Output Enable.** 0 = GPO2 output disabled (Hi-Z). 1 = GPO2 output enabled.
1	5	PATCH	**Patch Enable.** 0 = Boot normally 1 = Copy NVM to RAM, but do not boot. After CTS has been set, RAM may be patched.

ARG	Bit	Name	Function
1	4	XOSCEN	**Crystal Oscillator Enable.** 0 = Use external RCLK (crystal oscillator disabled). 1 = Use crystal oscillator (RCLK and GPO3/DCLK with external 32.768 kHz crystal and OPMODE = 00000101). See Si473x Data Sheet Application Schematic for external BOM details.
1	3:0	FUNC[3:0]	**Function.** 0 = Reserved. 1 = AM/SW/LW Receive. 2–14 = Reserved. 15 = Query Library ID.
2	7:0	OPMODE[7:0]	**Application Setting** 00000101 = Analog audio outputs (LOUT/ROUT). 00001011 = Digital audio output (DCLK, LOUT/DFS, ROUT/DIO)(Si4731/32/35/37 only with XOSCEN = 0) 10110000 = Digital audio outputs (DCLK, DFS, DIO) (Si4731/35/37 only with XOSCEN = 0). 10110101 = Analog and digital audio outputs (LOUT/ROUT and DCLK, DFS, DIO) (Si4731/35/37 only with XOSCEN = 0).

Response (to FUNC = 1, AM Receive)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	X	X	STCINT

Response (to FUNC = 15, Query Library ID)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	X	X	STCINT
RESP1	PN[7:0]							
RESP2	FWMAJOR[7:0]							
RESP3	FWMINOR[7:0]							
RESP4	RESERVED[7:0]							
RESP5	RESERVED[7:0]							
RESP6	CHIPREV[7:0]							
RESP7	LIBRARYID[7:0]							

RESP	Bit	Name	Function
1	7:0	PN[7:0]	**Final 2 digits of part number (HEX).**
2	7:0	FWMAJOR[7:0]	**Firmware Major Revision (ASCII).**
3	7:0	FWMINOR[7:0]	**Firmware Minor Revision (ASCII).**
4	7:0	RESERVED[7:0]	**Reserved, various values.**
5	7:0	RESERVED[7:0]	**Reserved, various values.**
6	7:0	CHIPREV[7:0]	**Chip Revision (ASCII).**
7	7:0	LIBRARYID[7:0]	**Library Revision (HEX).**

Command 0x10. GET_REV

Returns the part number, chip revision, firmware revision, patch revision and component revision numbers. The command is complete when the CTS bit (and optional interrupt) is set. This command may only be sent when in powerup mode.

Available in: All

Command arguments: None

Response bytes: Eight

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	0	0

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	X	X	STCINT
RESP1	PN[7:0]							
RESP2	FWMAJOR[7:0]							
RESP3	FWMINOR[7:0]							
RESP4	$PATCH_H$[7:0]							
RESP5	$PATCH_L$[7:0]							
RESP6	CMPMAJOR[7:0]							
RESP7	CMPMINOR[7:0]							
RESP8	CHIPREV[7:0]							

RESP	Bit	Name	Function
1	7:0	PN[7:0]	**Final 2 digits of Part Number (HEX).**
2	7:0	FWMAJOR[7:0]	**Firmware Major Revision (ASCII).**
3	7:0	FWMINOR[7:0]	**Firmware Minor Revision (ASCII).**
4	7:0	$PATCH_H$[7:0]	**Patch ID High Byte (HEX).**
5	7:0	$PATCH_L$[7:0]	**Patch ID Low Byte (HEX).**
6	7:0	CMPMAJOR[7:0]	**Component Major Revision (ASCII).**
7	7:0	CMPMINOR[7:0]	**Component Minor Revision (ASCII).**
8	7:0	CHIPREV[7:0]	**Chip Revision (ASCII).**

Command 0x11. POWER_DOWN

Moves the device from powerup to powerdown mode. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode. Note that only the POWER_UP command is accepted in powerdown mode. **If the system controller writes a command other than POWER_UP when in powerdown mode, the device does not respond. The device will only respond when a POWER_UP command is written. GPO pins are powered down and not active during this state. For optimal power down current, GPO2 must be either internally driven low through GPIO_CTL command or externally driven low.**

Note: In AMRX component 1.0, a reset is required when the system controller writes a command other than POWER_UP when in powerdown mode.

Note: The following describes the state of all the pins when in powerdown mode:
GPIO1, GPIO2, GPIO3 = 0
ROUT, LOUT, DOUT, DFS = HiZ

Available in: All

Command arguments: None

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	0	1

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	X	X	STCINT

Command 0x12. SET_PROPERTY

Sets a property shown in Table 13, “AM/SW/LW Receiver Property Summary,” on page 124. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode. See Figure 30, “CTS and SET_PROPERTY Command Complete tCOMP Timing Model,” on page 243 and Table 51, “Command Timing Parameters for the AM Receiver,” on page 246.

Available in: All

Command Arguments: Five

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	1	0
ARG1	0	0	0	0	0	0	0	0
ARG2	$PROP_H$[7:0]							
ARG3	$PROP_L$[7:0]							
ARG4	$PROPD_H$[7:0]							
ARG5	$PROPD_L$[7:0]							

ARG	Bit	Name	Function
1	7:0	Reserved	Always write to 0.
2	7:0	$PROP_H$[7:0]	**Property High Byte.** This byte in combination with $PROP_L$ is used to specify the property to modify. See Section "5.3.2. AM/SW/LW Receiver Properties" on page 146.
3	7:0	$PROP_L$[7:0]	**Property Low Byte.** This byte in combination with $PROP_H$ is used to specify the property to modify. See Section "5.3.2. AM/SW/LW Receiver Properties" on page 146.
4	7:0	$PROPD_H$[7:0]	**Property Value High Byte.** This byte in combination with $PROPD_L$ is used to set the property value. See Section "5.3.2. AM/SW/LW Receiver Properties" on page 146.
5	7:0	$PROPD_L$[7:0]	**Property Value Low Byte.** This byte in combination with $PROPD_H$ is used to set the property value. See Section "5.3.2. AM/SW/LW Receiver Properties" on page 146.

Command 0x13. GET_PROPERTY

Gets a property shown in Table 13, “AM/SW/LW Receiver Property Summary,” on page 124. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode.

Available in: All

Command arguments: Three

Response bytes: Three

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	1	1
ARG1	0	0	0	0	0	0	0	0
ARG2	$PROP_H[7:0]$							
ARG3	$PROP_L[7:0]$							

ARG	Bit	Name	Function
1	7:0	Reserved	Always write to 0.
2	7:0	$PROP_H[7:0]$	**Property High Byte.** This byte in combination with $PROP_L$ is used to specify the property to get.
3	7:0	$PROP_L[7:0]$	**Property Low Byte.** This byte in combination with $PROP_H$ is used to specify the property to get.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	X	X	STCINT
RESP1	0	0	0	0	0	0	0	0
RESP2	$PROPD_H[7:0]$							
RESP3	$PROPD_L[7:0]$							

RESP	Bit	Name	Function
1	7:0	Reserved	Always returns 0.
2	7:0	$PROPD_H[7:0]$	**Property Value High Byte.** This byte in combination with $PROPD_L$ represents the requested property value.
3	7:0	$PROPD_L[7:0]$	**Property Value High Byte.** This byte in combination with $PROPD_H$ represents the requested property value.

Command 0x14. GET_INT_STATUS

Updates bits 6:0 of the status byte. This command should be called after any command that sets the STCINT or RSQINT bits. When polling this command should be periodically called to monitor the STATUS byte, and when using interrupts, this command should be called after the interrupt is set to update the STATUS byte. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be set when in powerup mode.

Available in: All

Command arguments: None

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	1	0	0

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	X	X	STCINT

Command 0x40. AM_TUNE_FREQ

Tunes the AM/SW/LW receive to a frequency between 149 and 23 MHz in 1 kHz steps. In AM only mode, the valid frequency is between 520 and 1710 kHz in 1 kHz steps. The CTS bit (and optional interrupt) is set when it is safe to send the next command. The ERR bit (and optional interrupt) is set if an invalid argument is sent. Note that only a single interrupt occurs if both the CTS and ERR bits are set. The optional STC interrupt is set when the command completes. The STCINT bit is set only after the GET_INT_STATUS command is called. This command may only be sent when in powerup mode. The command clears the STC bit if it is already set. See Figure 29, “CTS and STC Timing Model,” on page 243 and Table 51, “Command Timing Parameters for the AM Receiver,” on page 246.

AM: LO frequency is 45 kHz above RF for RF frequencies $\leq$ 1000 kHz and 45 kHz below RF for RF frequencies > 1000 kHz. For example, LO frequency is 945 kHz when tuning to 900 kHz.

Note: FAST bit is supported in Si473x-C40 and later devices and Si4732 devices and Si474x devices (AMRX component 3.0 or later).
ANTCAP bits are supported in AMRX component 2.0 or later (all devices except Si4730-A10).

Available in: All

Command arguments: Five

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	1	0	0	0	0	0	0
ARG1	0	0	0	0	0	0	0	FAST
ARG2	$FREQ_H$[7:0]							

ARG3	$FREQ_L$[7:0]
ARG4	$ANTCAP_H$[15:8]
ARG5	$ANTCAP_L$[7:0]

ARG	Bit	Name	Function
1	7:1	Reserved	Always write to 0.
1	0	FAST	**FAST Tuning.** If set, executes fast and invalidated tune. The tune status will not be accurate.
2	7:0	$FREQ_H$ [7:0]	**Tune Frequency High Byte.** This byte in combination with $FREQ_L$ selects the tune frequency in kHz. In AM/SW/LW mode, the valid range is from 149 to 23000 (149 kHz–23 MHz). In AM only mode the valid range is from 520 to 1710 (520–1710 kHz).
3	7:0	$FREQ_L$ [7:0]	**Tune Frequency Low Byte.** This byte in combination with $FREQ_H$ selects the tune frequency in kHz. In AM/SW/LW mode, the valid range is from 149 to 23000 (149 kHz–23 MHz). In AM only mode the valid range is from 520 to 1710 (520–1710 kHz).
4	15:8	$ANTCAP_H$ [15:8]	**Antenna Tuning Capacitor High Byte.** This byte in combination with $ANTCAP_L$ selects the tuning capacitor value. If both bytes are set to zero, the tuning capacitor value is selected automatically. If the value is set to anything other than 0, the tuning capacitance is manually set as 95 fF x ANTCAP + 7 pF. ANTCAP manual range is 1–6143. Automatic capacitor tuning is recommended. **Note:** In SW mode, $ANTCAP_H$[15:8] needs to be set to 0 and $ANTCAP_L$[7:0] needs to be set to 1.
5	7:0	$ANTCAP_L$ [7:0]	**Antenna Tuning Capacitor Low Byte.** This byte in combination with $ANTCAP_H$ selects the tuning capacitor value. If both bytes are set to zero, the tuning capacitor value is selected automatically. If the value is set to anything other than 0, the tuning capacitance is manually set as 95 fF x ANTCAP + 7 pF. ANTCAP manual range is 1–6143. Automatic capacitor tuning is recommended. **Note:** In SW mode, $ANTCAP_H$[15:8] needs to be set to 0 and $ANTCAP_L$[7:0] needs to be set to 1.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	X	X	STCINT

Command 0x41. AM_SEEK_START

Initiates a seek for a channel that meets the RSSI and SNR criteria for AM. Clears any pending STCINT or RSQINT interrupt status. RSQINT is only cleared by the RSQ status command when the INTACK bit is set. The CTS bit (and optional interrupt) is set when it is safe to send the next command. The ERR bit (and optional interrupt) is set if an invalid argument is sent. Note that only a single interrupt occurs if both the CTS and ERR bits are set. The optional STC interrupt is set when the command completes. The STCINT bit is set only after the GET_INT_STATUS command is called. This command may only be sent when in powerup mode. The command clears the STCINT bit if it is already set. See Figure 29, “CTS and STC Timing Model,” on page 243 and Table 51, “Command Timing Parameters for the AM Receiver,” on page 246.

Note: ANTCAP bits are supported in AMRX component 2.1 or later.

Available in: All

Command arguments: Five

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	1	0	0	0	0	0	1
ARG1	0	0	0	0	SEEKUP	WRAP	0	0
ARG2	0	0	0	0	0	0	0	0
ARG3	0	0	0	0	0	0	0	0
ARG4	$ANTCAP_H$[15:8]							
ARG5	$ANTCAP_L$[7:0]							

ARG	Bit	Name	Function
1	7:4	Reserved	Always write to 0.
1	3	SEEKUP	**Seek Up/Down.** Determines the direction of the search, either UP = 1, or DOWN = 0.
1	2	WRAP	**Wrap/Halt.** Determines whether the seek should Wrap = 1, or Halt = 0 when it hits the band limit.
1	1:0	Reserved	Always write to 0.
2	7:0	Reserved	Always write to 0.
3	7:0	Reserved	Always write to 0.
4	15:8	$ANTCAP_H$[15:8]	**Antenna Tuning Capacitor High Byte.** This byte in combination with $ANTCAP_L$ selects the tuning capacitor value. If both bytes are set to zero, the tuning capacitor value is selected automatically. If the value is set to anything other than 0, the tuning capacitance is manually set as 95 fF x ANTCAP + 7 pF. ANTCAP manual range is 1–6143. Automatic capacitor tuning is recommended. **Note:** In SW mode, $ANTCAP_H$[15:8] needs to be set to 0 and $ANTCAP_L$[7:0] needs to be set to 1.
5	7:0	$ANTCAP_L$[7:0]	**Antenna Tuning Capacitor Low Byte.** This byte in combination with $ANTCAP_H$ selects the tuning capacitor value. If both bytes are set to zero, the tuning capacitor value is selected automatically. If the value is set to anything other than 0, the tuning capacitance is manually set as 95 fF x ANTCAP + 7 pF. ANTCAP manual range is 1–6143. Automatic capacitor tuning is recommended. **Note:** In SW mode, $ANTCAP_H$[15:8] needs to be set to 0 and $ANTCAP_L$[7:0] needs to be set to 1.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	X	X	STCINT

Command 0x42. AM_TUNE_STATUS

Returns the status of AM_TUNE_FREQ or AM_SEEK_START commands. The commands returns the current frequency, RSSI, SNR, and the antenna tuning capacitance value (0–6143). The command clears the STCINT interrupt bit when INTACK bit of ARG1 is set. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode.

Note: AFCRL bit does not work properly on AMRX component 2.1 or earlier.

Available in: All

Command arguments: One

Response bytes: Seven

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	1	0	0	0	0	1	0
ARG1	0	0	0	0	0	0	CANCEL	INTACK

ARG	Bit	Name	Function
1	7:2	Reserved	Always write to 0.
1	1	CANCEL	**Cancel seek.** If set, aborts a seek currently in progress.
1	0	INTACK	**Seek/Tune Interrupt Clear.** If set, clears the seek/tune complete interrupt status indicator.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	X	X	STCINT
RESP1	BLTF	X	X	X	X	X	AFCRL	VALID
RESP2	$READFREQ_H$[7:0]							
RESP3	$READFREQ_L$[7:0]							
RESP4	RSSI[7:0]							
RESP5	SNR[7:0]							
RESP6	$READANTCAP_H$ [15:8]							
RESP7	$READANTCAP_L$ [7:0]							

RESP	Bit	Name	Function
1	7	BLTF	**Band Limit.** Reports if a seek hit the band limit (WRAP = 0 in AM_START_SEEK) or wrapped to the original frequency (WRAP = 1).
1	6:2	Reserved	Always returns 0.
1	1	AFCRL	**AFC Rail Indicator.** Set if the AFC rails.
1	0	VALID	**Valid Channel.** Set if the channel is currently valid and would have been found during a seek.
2	7:0	$READFREQ_H$[7:0]	**Read Frequency High Byte.** This byte in combination with $READFREQ_L$ returns frequency being tuned (kHz).
3	7:0	$READFREQ_L$[7:0]	**Read Frequency Low Byte.** This byte in combination with $READFREQ_H$ returns frequency being tuned (kHz).
4	7:0	RSSI[7:0]	**Received Signal Strength Indicator.** This byte contains the receive signal strength when tune is completed (dBµV).
5	7:0	SNR[7:0]	**SNR.** This byte contains the SNR metric when tune is completed (dB).
6	7:0	$READANTCAP_H$ [15:8]	**Read Antenna Tuning Capacitor High Byte.** This byte in combination with $READANTCAP_L$ returns the current antenna tuning capacitor value. The tuning capacitance is 95 fF x READANTCAP + 7 pF.
7	7:0	$READANTCAP_L$ [7:0]	**Read Antenna Tuning Capacitor Low Byte.** This byte in combination with $READANTCAP_H$ returns the current antenna tuning capacitor value. The tuning capacitance is 95 fF x READANTCAP + 7 pF.

Command 0x43. AM_RSQ_STATUS

Returns status information about the received signal quality. The commands returns RSSI and SNR. It also indicates valid channel (VALID), soft mute engagement (SMUTE), and AFC rail status (AFCRL). This command can be used to check if the received signal is above the RSSI high threshold as reported by RSSIHINT, or below the RSSI low threshold as reported by RSSILINT. It can also be used to check if the signal is above the SNR high threshold as reported by SNRHINT, or below the SNR low threshold as reported by SNRLINT. The command clears the RSQINT, SNRHINT, SNRLINT, RSSIHINT, and RSSILINT interrupt bits when INTACK bit of ARG1 is set. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode.

Note: AFCRL bit does not work properly on AMRX component 2.1 or earlier.

Available in: All

Command arguments: One

Response bytes: Five

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	1	0	0	0	0	1	1
ARG1	0	0	0	0	0	0	0	INTACK

ARG	Bit	Name	Function
1	0	INTACK	**Interrupt Acknowledge.** 0 = Interrupt status preserved. 1 = Clears RSQINT, SNRHINT, SNRLINT, RSSIHINT, RSSILINT

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	X	X	STCINT
RESP1	X	X	X	X	SNRHINT	SNRLINT	RSSI-HINT	RSSIILINT
RESP2	X	X	X	X	SMUTE	X	AFCRL	VALID
RESP3	X	X	X	X	X	X	X	X
RESP4	RSSI[7:0]							
RESP5	SNR[7:0]							

RESP	Bit	Name	Function
1	3	SNRHINT	**SNR Detect High.** 0 = Received SNR has not exceeded above SNR high threshold. 1 = Received SNR has exceeded above SNR high threshold.
1	2	SNRLINT	**SNR Detect Low.** 0 = Received SNR has not exceeded below SNR low threshold. 1 = Received SNR has exceeded below SNR low threshold.
1	1	RSSIHINT	**RSSI Detect High.** 0 = RSSI has not exceeded above RSSI high threshold. 1 = RSSI has exceeded above RSSI high threshold.
1	0	RSSILINT	**RSSI Detect Low.** 0 = RSSI has not exceeded below RSSI low threshold. 1 = RSSI has exceeded below RSSI low threshold.
2	3	SMUTE	**Soft Mute Indicator.** Indicates soft mute is engaged.
2	1	AFCRL	**AFC Rail Indicator.** Set if the AFC rails.
2	0	VALID	**Valid Channel.** Set if the channel is currently valid and would have been found during a seek.
4	7:0	RSSI[7:0]	**Received Signal Strength Indicator.** Contains the current receive signal strength (dBµV).
5	7:0	SNR[7:0]	**SNR.** Contains the current SNR metric (dB).

Command 0x47. AM_AGC_STATUS

Returns the AM AGC setting of the device. The command returns whether the AGC is enabled or disabled and it returns the gain index. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in power up mode.

Available in: All

Command arguments: None

Response bytes: Two

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	1	0	0	0	1	1	1

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	X	X	STCINT
RESP1	X	X	X	X	X	X	X	AMAGCDIS
RESP2	AMAGCNDX[7:0]							

RESP	Bit	Name	Function
1	0	AMAGCDIS	**AM AGC Disable** This bit indicates if the AGC is enabled or disabled. 0 = AGC enabled. 1 = AGC disabled.
2	7:0	AMAGCNDX	**AM AGC Index** This byte reports the current AGC gain index. 0 = Minimum attenuation (max gain) 1 – 36+ATTN_BACKUP = Intermediate attenuation 37+ATTN_BACKUP = Maximum attenuation (min gain) **Note:** The max index is subject to change. See Property 0x3705 AM_FRONTEND_AGC_CONTROL for details on ATTN_BACKUP.

Command 0x48. AM_AGC_OVERRIDE

Overrides the AM AGC setting by disabling the AGC and forcing the gain index that ranges between 0 (minimum attenuation) and 37+ATTN_BACKUP (maximum attenuation). The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in power up mode.

Available in: All

Command arguments: Two

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	1	0	0	1	0	0	0
ARG1	0	0	0	0	0	0	0	AMAGCDIS
ARG2	AMAGCNDX[7:0]							

ARG	Bit	Name	Function
1	0	AMAGCDIS	**AM AGC Disable** This bit selects whether the AGC is enabled or disabled. 0 = AGC enabled. 1 = AGC disabled.
2	7:0	AMAGCNDX	**AM AGC Index** If AMAGCDIS = 1, this byte forces the AGC gain index. 0 = Minimum attenuation (max gain) 1 – 36+ATTN_BACKUP = Intermediate attenuation 37+ATTN_BACKUP = Maximum attenuation (min gain) ***Note:** The max index is subject to change. See Property 0x3705 AM_FRONTEND_AGC_CONTROL for details on ATTN_BACKUP.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	X	X	STCINT

Command 0x80. GPIO_CTL

Enables output for GPO1, 2, and 3. GPO1, 2, and 3 can be configured for output (Hi-Z or active drive) by setting the GPO1OEN, GPO2OEN, and GPO3OEN bit. The state (high or low) of GPO1, 2, and 3 is set with the GPIO_SET command. To avoid excessive current consumption due to oscillation, GPO pins should not be left in a high impedance state. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode. The default is all GPO pins set for high impedance.

Notes:

1. GPIO_CTL is supported in AM_SW_LW component 2.0 or later.
2. The use of GPO2 as an interrupt pin and/or the use of GPO3 as DCLK digital clock input will override this GPIO_CTL function for GPO2 and/or GPO3 respectively.

Available in: All

Command arguments: One

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	1	0	0	0	0	0	0	0
ARG1	0	0	0	0	GPO3OEN	GPO2OEN	GPO1OEN	0

ARG	Bit	Name	Function
1	7:4	Reserved	Always write 0.
1	3	GPO3OEN	**GPO3 Output Enable.** 0 = Output Disabled (Hi-Z) (default). 1 = Output Enabled.
1	2	GPO2OEN	**GPO2 Output Enable.** 0 = Output Disabled (Hi-Z) (default). 1 = Output Enabled.
1	1	GPO1OEN	**GPO1 Output Enable.** 0 = Output Disabled (Hi-Z) (default). 1 = Output Enabled.
1	0	Reserved	Always write 0.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	RDSINT	ASQINT	STCINT

Command 0x81. GPIO_SET

Sets the output level (high or low) for GPO1, 2, and 3. GPO1, 2, and 3 can be configured for output by setting the GPO1OEN, GPO2OEN, and GPO3OEN bit in the GPIO_CTL command. To avoid excessive current consumption due to oscillation, GPO pins should not be left in a high impedance state. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is all GPO pins set for high impedance.

Note: GPIO_SET is supported in AM_SW_LW component 2.0 or later.

Available in: All

Command arguments: One

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	1	0	0	0	0	0	0	1
ARG1	0	0	0	0	GPO3LEVEL	GPO2LEVEL	GPO1LEVEL	0

ARG	Bit	Name	Function
1	7:4	Reserved	Always write 0.
1	3	GPO3LEVEL	**GPO3 Output Level.** 0 = Output low (default). 1 = Output high.
1	2	GPO2LEVEL	**GPO2 Output Level.** 0 = Output low (default). 1 = Output high.
1	1	GPO1LEVEL	**GPO1 Output Level.** 0 = Output low (default). 1 = Output high.
1	0	Reserved	Always write 0.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	RDSINT	ASQINT	STCINT

5.3.2. AM/SW/LW Receiver Properties

Property 0x0001. GPO_IEN

Configures the sources for the GPO2/$\overline{\text{INT}}$ interrupt pin. Valid sources are the lower 8 bits of the STATUS byte, including CTS, ERR, RSQINT, and STCINT bits. The corresponding bit is set before the interrupt occurs. The CTS bit (and optional interrupt) is set when it is safe to send the next command. The CTS interrupt enable (CTSIEN) can be set with this property and the POWER_UP command. The state of the CTSIEN bit set during the POWER_UP command can be read by reading this property and modified by writing this property. This property may only be set or read when in powerup mode.

Available in: All

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	RSQREP	0	0	STCREP	CTSIEN	ERRIEN	0	0	RSQIEN	0	0	STCIEN

Bit	Name	Function
15:12	Reserved	Always write to 0.
11	RSQREP	**RSQ Interrupt Repeat.** 0 = No interrupt generated when RSQINT is already set (default) 1 = Interrupt generated even if RSQINT is already set
10:9	Reserved	Always write to 0.
8	STCREP	**STC Interrupt Repeat.** 0 = No interrupt generated when STCINT is already set (default) 1 = Interrupt generated even if STCINT is already set
7	CTSIEN	**CTS Interrupt Enable.** After PowerUp, this bit reflects the CTSIEN bit in ARG1 of PowerUp Command. 0 = No interrupt generated when CTS is set 1 = Interrupt generated when CTS is set
6	ERRIEN	**ERR Interrupt Enable.** 0 = No interrupt generated when ERR is set (default) 1 = Interrupt generated when ERR is set
5:4	Reserved	Always write to 0.
3	RSQIEN	**RSQ Interrupt Enable.** 0 = No interrupt generated when RSQINT is set (default) 1 = Interrupt generated when RSQINT is set
2:1	Reserved	Always write to 0.
0	STCIEN	**Seek/Tune Complete Interrupt Enable.** 0 = No interrupt generated when STCINT is set (default) 1 = Interrupt generated when STCINT is set

Property 0x0102. DIGITAL_OUTPUT_FORMAT

Configures the digital audio output format. Configuration options include DCLK edge, data format, force mono, and sample precision.

Note: DIGITAL_OUTPUT_FORMAT is supported in AM_SW_LW component 2.0 or later.

Available in: Si4705/06, Si4731/32/35/37/39, Si4730/34/36/38-D60 and later, Si4741/43/45, Si4784/85

Default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	OFALL	OMODE[3:0]				0	OSIZE[1:0]	

Bit	Name	Function
15:8	Reserved	Always write to 0.
7	OFALL	**Digital Output DCLK Edge.** 0 = use DCLK rising edge 1 = use DCLK falling edge
6:3	OMODE[3:0]	**Digital Output Mode.** 0000 = I^2S 0110 = Left-justified 1000 = MSB at second DCLK after DFS pulse 1100 = MSB at first DCLK after DFS pulse
2	Reserved	Always write to 0.
1:0	OSIZE[1:0]	**Digital Output Audio Sample Precision.** 0 = 16-bits 1 = 20-bits 2 = 24-bits 3 = 8-bits

Property 0x0104. DIGITAL_OUTPUT_SAMPLE_RATE

Enables digital audio output and configures digital audio output sample rate in samples per second (sps). When DOSR[15:0] is 0, digital audio output is disabled. To enable digital audio output, program DOSR[15:0] with the sample rate in samples per second. The over-sampling rate must be set in order to satisfy a minimum DCLK of 1 MHz. **The system controller must establish DCLK and DFS prior to enabling the digital audio output else the device will not respond and will require reset. The sample rate must be set to 0 before DCLK/DFS is removed. AM_TUNE_FREQ command must be sent after the POWER_UP command to start the internal clocking before setting this property.**

Note: DIGITAL_OUTPUT_SAMPLE_RATE is supported in AM_SW_LW component 2.0 or later.
Available in: Si4705/06, Si4731/32/35/37/39, Si4730/34/36/38-D60 and later, Si4741/43/45, Si4784/85
Default: 0x0000 (digital audio output disabled)
Units: sps
Range: 32–48 ksps, 0 to disable digital audio output

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOSR[15:0]															

Bit	Name	Function
15:0	DOSR[15:0]	**Digital Output Sample Rate.** 32–48 ksps. 0 to disable digital audio output.

Property 0x0201. REFCLK_FREQ

Sets the frequency of the REFCLK from the output of the prescaler. The REFCLK range is 31130 to 34406 Hz (32768 5% Hz) in 1 Hz steps, or 0 (to disable AFC). For example, an RCLK of 13MHz would require a prescaler value of 400 to divide it to 32500 Hz REFCLK. The reference clock frequency property would then need to be set to 32500 Hz. RCLK frequencies between 31130 Hz and 40 MHz are supported, however, there are gaps in frequency coverage for prescaler values ranging from 1 to 10, or frequencies up to 311300 Hz. The following table summarizes these RCLK gaps.

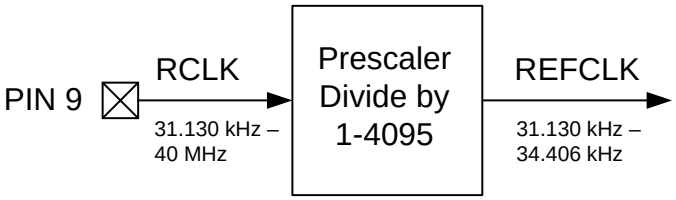


Figure 12. REFCLK Prescaler

Table 15. RCLK Gaps

Prescaler	RCLK Low (Hz)	RCLK High (Hz)
1	31130	34406
2	62260	68812
3	93390	103218
4	124520	137624
5	155650	172030
6	186780	206436
7	217910	240842
8	249040	275248
9	280170	309654
10	311300	344060

The RCLK must be valid 10 ns before and 10 ns after completing the WB_TUNE_FREQ command. In addition, the RCLK must be valid at all times when the carrier is enabled for proper AGC operation. The RCLK may be removed or reconfigured at other times. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode. The default is 32768 Hz.

Available in: All

Default: 0x8000 (32768)

Units: 1 Hz

Step: 1Hz

Range: 31130-34406

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	REFCLKF[15:0]															

Bit	Name	Function
15:0	REFCLKF[15:0]	**Frequency of Reference Clock in Hz.** The allowed REFCLK frequency range is between 31130 and 34406 Hz (32768 5%), or 0 (to disable AFC).

Property 0x0202. REFCLK_PRESCALE

Sets the number used by the prescaler to divide the external RCLK down to the internal REFCLK. The range may be between 1 and 4095 in 1 unit steps. For example, an RCLK of 13 MHz would require a prescaler value of 400 to divide it to 32500 Hz. The reference clock frequency property would then need to be set to 32500 Hz. The RCLK must be valid 10 ns before sending and 20 ns after completing the AM_TUNE_FREQ and AM_SEEK_START commands. In addition, the RCLK must be valid at all times for proper AFC operation. The RCLK may be removed or reconfigured at other times. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 1.

Available in: All

Default: 0x0001

Step: 1

Range: 1–4095

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	RCLK SEL	RCLKP[11:0]											

Bit	Name	Function
15:13	Reserved	Always write to 0.
12	RCLKSEL	**RCLKSEL.** 0 = RCLK pin is clock source. 1 = DCLK pin is clock source.
11:0	RCLKP[11:0]	**Prescaler for Reference Clock.** Integer number used to divide the RCLK frequency down to REFCLK frequency. The allowed REFCLK frequency range is between 31130 and 34406* Hz (32768 ±5%), or 0 (to disable AFC).

***Note:** For shortwave frequencies, choose a prescalar value such that you can limit the REFCLK frequency range to 31130–32768* Hz.

Property 0x3100. AM_DEEMPHASIS

Sets the AM Receive de-emphasis to 50 µs. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is disabled.

Available in: All

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DEEMPH

Bit	Name	Function
15:1	Reserved	Always write to 0.
0	DEEMPH	**AM De-Emphasis.** 1 = 50 µs. 0 = Disabled.

Property 0x3102. AM_CHANNEL_FILTER

Selects the bandwidth of the AM channel filter. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 2 kHz bandwidth channel filter.

Note: The 1 kHz option, 1.8 kHz option, and 100 Hz high-pass Line Noise Rejection filter are supported on Si473x-C40 and later devices and Si4732 devices and Si474x devices (AM_SW_LW component 3.0 or later).
The 2.5 kHz option is supported on Si473x-C40 and later devices and Si4732 devices (AM_SW_LW component 5.0 or later).

Available in: All

Default: 0x0003

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	AMPLFLT	0	0	0	0	AMCHFLT[03:0]			

Bit	Name	Function
15:9	Reserved	Always write to 0.
8	AMPLFLT	Enables the AM Power Line Noise Rejection Filter
7:4	Reserved	Always write to 0.
3:0	AMCHFILT	**AM Channel Filter.** Selects the bandwidth of the AM channel filter. The following choices are available: 0 = 6 kHz Bandwidth 1 = 4 kHz Bandwidth 2 = 3 kHz Bandwidth 3 = 2 kHz Bandwidth 4 = 1 kHz Bandwidth 5 = 1.8 kHz Bandwidth 6 = 2.5 kHz Bandwidth, gradual roll off 7–15 = Reserved (Do not use)

Property 0x3103. AM_AUTOMATIC_VOLUME_CONTROL_MAX_GAIN

Sets the maximum gain for automatic volume control. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 16 dB.

The maximum AVC gain affects audio output level, especially under weak signal conditions. It amplifies the signal as well as noise. When a signal is very weak (needs a lot of gain) then the maximum gain will be applied, and may make the noise too harsh for the listener, even the soft mute functions. The user can reduce the noise further by adjusting the maximum AVC gain. The property allows the user to optimize the trade-off between maintaining output level and suppressing noise.

Note: The maximum AVC gain is not configurable in Si473x-B20 devices (FMRX component 2.1 and earlier), and is 90.3 dB. This would be equivalent to AM_AUTOMATIC_VOLUME_CONTROL_MAX_GAIN property value 0x7800, which is the maximum value.

Available in: Si473x-C40 and later, Si4732, Si474x

Default: 0x1543 (Si473x-C40 and later, Si4732)

0x7800 (Si474x)

Step: 1

Range: 0X1000 ~ 0x7800

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	AVC_MAXGAIN [14:0]														

Bit	Name	Function
15	Reserved	Always write to 0.
14:0	AVC_MAXGAIN	**Automatic Volume Control Max Gain.** Maximum gain for automatic volume control. The max gain value is given by AVC_MAXGAIN = g * 340.2 where g is the desired maximum AVC gain in dB. Minimum of 12 dB is recommend when SOFTMUTE is enabled.

Property 0x3104. AM_MODE_AFC_SW_PULL_IN_RANGE

Sets the SW AFC pull-in or tracking range. The value PULL_IN_RANGE is relative to the tuned frequency and is specified as $1/(PPM \times 10^{-6})$. For example to program a pull-in range of 115 ppm,
PULL_IN_RANGE = $1/(115 \times 10^{-6})$ = 8695. The command is complete when the CTS bit (and optional interrupt) is set.

Available in: Si4734/35-C40 and later, Si4732, Si4742/43/44/45

Default: 0x21F7 (115 ppm)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	SWPIR[15:0]															

Bit	Name	Function
15:0	SWPIR[15:0]	**SW Pull-In Range** The SW pull-in range expressed relative to the tuned frequency.

Property 0x3105. AM_MODE_AFC_SW_LOCK_IN_RANGE

Sets the SW AFC lock-in or capture range. The value LOCK_IN_RANGE is relative to the tuned frequency and is specified as 1/(PPM×10^{-6}). For example to program a lock-in range of 85 ppm,
LOCK_IN_RANGE = 1/(85×10^{-6}) = 11765. The command is complete when the CTS bit (and optional interrupt) is set.

Available in: Si4734/35-C40 and later, Si4732, Si4742/43/44/45

Default: 0x2DF5 (85 ppm)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	SWPIR[15:0]															

Bit	Name	Function
15:0	SWPIR[15:0]	**SW Pull-In Range** The SW lock-in range expressed relative to the tuned frequency.

Property 0x3200. AM_RSQ_INT_SOURCE

Configures interrupt related to Received Signal Quality metrics. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode.

Available in: All

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	SNRHIEN	SNRLIEN	RSSIHIEN	RSSILIEN

Bit	Name	Function
15:4	Reserved	Always write 0.
3	SNRHIEN	**Interrupt Source Enable: SNR High.** Enable SNR high as the source of interrupt which the threshold is set by AM_RSQ_SNR_HI_THRESHOLD.
2	SNRLIEN	**Interrupt Source Enable: SNR Low.** Enable SNR low as the as the source of interrupt which the threshold is set by AM_RSQ_SNR_LO_THRESHOLD.
1	RSSIHIEN	**Interrupt Source Enable: RSSI High.** Enable RSSI low as the source of interrupt which the threshold is set by AM_RSQ_RSSI_HI_THRESHOLD.
0	RSSILIEN	**Interrupt Source Enable: RSSI Low.** Enable RSSI low as the source of interrupt which the threshold is set by AM_RSQ_RSSI_LO_THRESHOLD.

Property 0x3201. AM_RSQ_SNR_HI_THRESHOLD

Sets high threshold which triggers the RSQ interrupt if the SNR is above this threshold. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 127 dB.

Available in: All
Default: 0x007F
Units: dB
Step: 1
Range: 0–127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	SNRH[6:0]						

Bit	Name	Function
15:7	Reserved	Always write to 0.
6:0	SNRH	**AM RSQ SNR High Threshold.** Threshold which triggers the RSQ interrupt if the SNR goes above this threshold. Specified in units of dB in 1 dB steps (0–127). Default is 0 dB.

Property 0x3202. AM_RSQ_SNR_LO_THRESHOLD

Sets low threshold which triggers the RSQ interrupt if the SNR is below this threshold. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 0 dB.

Available in: All

Default: 0x0000

Units: dB

Step: 1

Range: 0–127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	SNRL[6:0]						

Bit	Name	Function
15:7	Reserved	Always write to 0.
6:0	SNRL	**AM RSQ SNR Low Threshold.** Threshold which triggers the RSQ interrupt if the SNR goes below this threshold. Specified in units of dB in 1 dB steps (0–127). Default is 0 dB.

Property 0x3203. AM_RSQ_RSSI_HI_THRESHOLD

Sets high threshold which triggers the RSQ interrupt if the RSSI is above this threshold. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 127 dB.

Available in: All

Default: 0x007F

Units: dBµV

Step: 1

Range: 0–127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	RSSIH[6:0]						

Bit	Name	Function
15:7	Reserved	Always write to 0.
6:0	RSSIH	**AM RSQ RSSI High Threshold.** Threshold which triggers the RSQ interrupt if the RSSI goes above this threshold. Specified in units of dBµV in 1 dB steps (0–127). Default is 0 dBµV.

Property 0x3204. AM_RSQ_RSSI_LO_THRESHOLD

Sets low threshold which triggers the RSQ interrupt if the RSSI is below this threshold. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 0 dB.

Available in: All

Default: 0x0000

Units: dBµV

Step: 1

Range: 0–127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	RSSIL[6:0]						

Bit	Name	Function
15:7	Reserved	Always write to 0.
6:0	RSSIL	**AM RSQ RSSI Low Threshold.** Threshold which triggers the RSQ interrupt if the RSSI goes below this threshold. Specified in units of dBµV in 1 dB steps (0–127). Default is 0 dBµV.

Property 0x3300. AM_SOFT_MUTE_RATE

Sets the attack and decay rates when entering or leaving soft mute. The value specified is multiplied by 4.35 dB/s to come up with the actual attack rate. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default rate is 278 dB/s.

Available in: All

Default: 0x0040

Actual Rate: SMRATE x 4.35

Units: dB/s

Step: 1

Range: 1–255

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	SMRATE[15:0]															

Bit	Name	Function
15:0	SMRATE	**AM Soft Mute Rate.** Determines how quickly the AM goes into soft mute when soft mute is enabled. The actual rate is calculated by taking the value written to the field and multiplying it with 4.35 dB/s. The default rate is 278 dB/s (SMRATE[15:0] = 0x0040).

Property 0x3301. AM_SOFT_MUTE_SLOPE

Configures attenuation slope during soft mute in dB attenuation per dB SNR below the soft mute SNR threshold. Soft mute attenuation is the minimum of SMSLOPE x (SMTHR – SNR) and SMATTN. The recommended SMSLOPE value is CEILING(SMATTN/SMTHR). SMATTN and SMTHR are set via the AM_SOFT_MUTE_MAX_ATTENUATION and AM_SOFT_MUTE_SNR_THRESHOLD properties. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default slope is 1 dB/dB for AMRX component 5.0 or later and 2 dB/dB for AMRX component 3.0 or earlier.

Available in: All

Default: 0x0002 (Si4730/31/34/35/36/37-B20 and earlier, Si4740/41/42/43/44/45-C10 and earlier)

0x0001 (all others)

Units: dB/dB

Range: 1–5

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	SMSLOPE[3:0]			

Bit	Name	Function
15:4	Reserved	Always write to 0.
3:0	SMSLOPE[3:0]	**AM Slope Mute Attenuation Slope.** Set soft mute attenuation slope in dB attenuation per dB SNR below the soft mute SNR threshold.

Property 0x3302. AM_SOFT_MUTE_MAX_ATTENUATION

Sets maximum attenuation during soft mute (dB). Set to 0 to disable soft mute. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default attenuation is 8 dB for AMRX component 5.0 or later and 16 dB for AMRX component 3.0 or earlier.

Available in: All

Default: 0x0010 (Si4730/31/34/35/36/37-B20 and earlier, Si4740/41/42/43/44/45-C10 and earlier)

0x0008 (all others)

Units: dB

Step: 1

Range: 0–63

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	SMATTN[5:0]					

Bit	Name	Function
15:6	Reserved	Always write to 0.
5:0	SMATTN	**AM Soft Mute Max Attenuation.** Maximum attenuation to apply when in soft mute. Specified in units of dB. Default maximum attenuation is 8 dB.

Property 0x3303. AM_SOFT_MUTE_SNR_THRESHOLD

Sets the SNR threshold to engage soft mute. Whenever the SNR for a tuned frequency drops below this threshold the AM reception will go in soft mute, provided soft mute max attenuation property is non-zero. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default SNR threshold is 8 dB for AMRX component 5.0 or later and 10 dB for AMRX component 3.0 or earlier.

Available in: All

Default: 0x000A (Si4730/31/34/35/36/37-B20 and earlier, Si4740/41/42/43/44/45-C10 and earlier)

0x0008 (all others)

Units: dB

Step: 1

Range: 0–63

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	SMTHR[5:0]					

Bit	Name	Function
15:6	Reserved	Always write to 0.
5:0	SMTHR	**AM Soft Mute SNR Threshold.** The SNR threshold for a tuned frequency below which soft mute is engaged provided the value written to the AM_SOFT_MUTE_MAX_ATTENUATION property is not zero. Default SNR threshold is 8 dB.

Property 0x3304. AM_SOFT_MUTE_RELEASE_RATE

Sets the soft mute release rate. Smaller values provide slower release and larger values provide faster release. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 8192 (approximately 8000 dB/s).

Release Rate (dB/s) = RELEASE[14:0]/1.024

Available in: Si4740/41/42/43/44/45

Default: 0x2000

Range: 1–32767

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	RELEASE[14:0]														

Property 0x3305. AM_SOFT_MUTE_ATTACK_RATE

Sets the soft mute attack rate. Smaller values provide slower attack and larger values provide faster attack. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 8192 (approximately 8000 dB/s).

Attack Rate (dB/s) = ATTACK[14:0]/1.024

Available in: Si4740/41/42/43/44/45

Default: 0x2000

Range: 1–32767

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	ATTACK[14:0]														

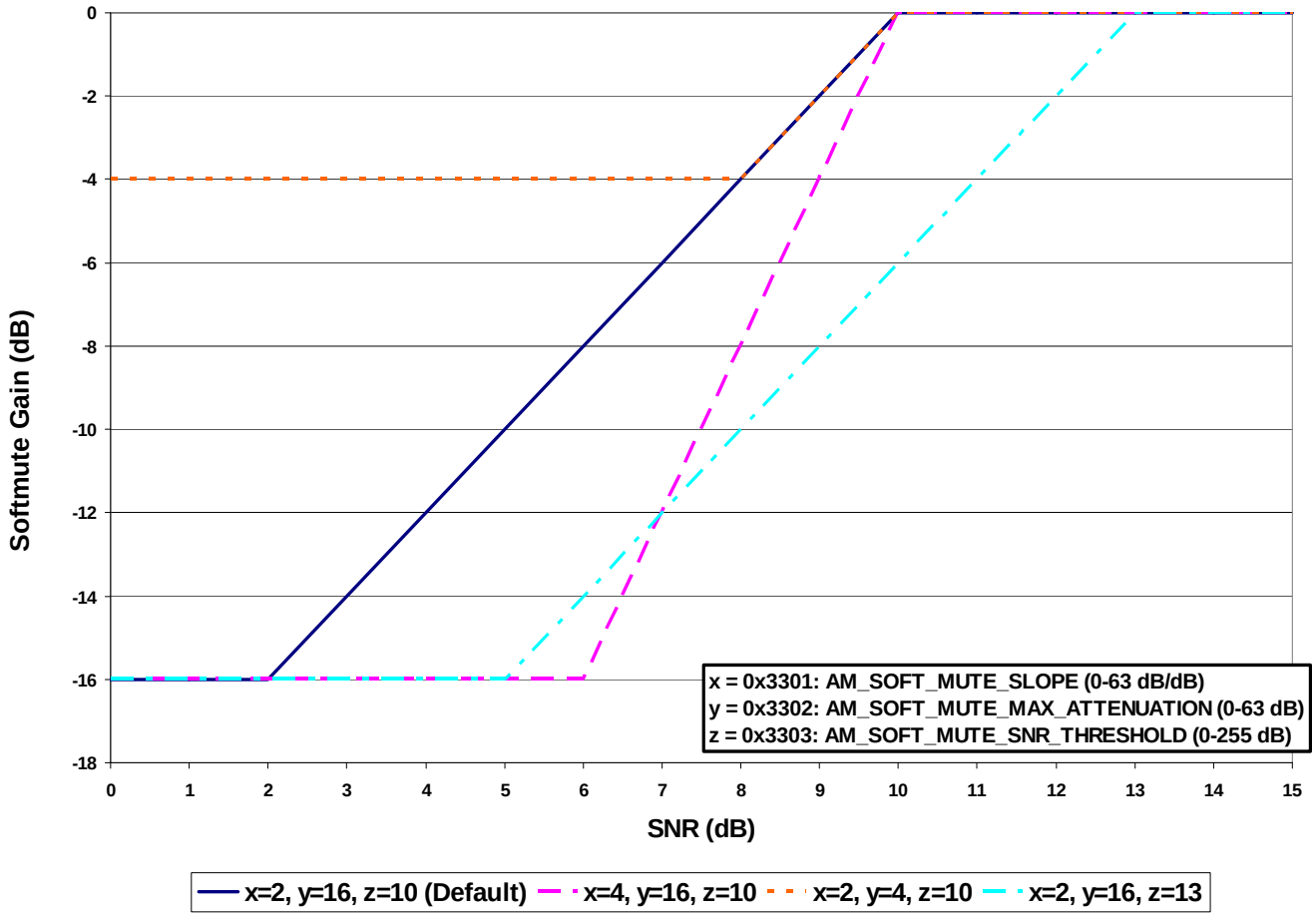


Figure 13. AM Softmute SNR

Property 0x3400. AM_SEEK_BAND_BOTTOM

Sets the lower boundary for the AM band in kHz. This value is used to determine when the lower end of the AM band is reached when performing a seek. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 520 kHz (0x0208).

Available in: All

Default: 0x0208

Units: kHz

Step: 1 kHz

Valid Range: 149–23000 kHz

Recommended Range:

- AM in US: 520–1710 kHz
- AM in Asia: 522–1710 kHz
- SW: 2300–23000 kHz
- LW: 153–279 kHz

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	AMSKFREQL[15:0]															

Bit	Name	Function
15:0	AMSKFREQL	**AM Seek Band Bottom.** Specify the lower boundary of the AM band when performing a seek. The seek either stops at this limit or wraps based on the parameters of AM_SEEK_START command that was issued to initiate a seek. The default value for the lower boundary of the AM band is 520 kHz.

Property 0x3401. AM_SEEK_BAND_TOP

Sets the upper boundary for the AM band in kHz. This value is used to determine when the higher end of the AM band is reached when performing a seek. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 1710 kHz (0x06AE).

Available in: All

Default: 0x06AE

Note: Firmware 1.0 incorrectly reports 0x06B9 (1721 kHz) as default for AM_SEEK_BAND_TOP. After POWER_UP command is complete, set AM_SEEK_BAND_TOP to 0x06AE (1710 kHz) using the SET_PROPERTY command.

Units: kHz

Step: 1 kHz

Valid Range: 149–23000 kHz

Recommended Range:

- AM in US: 520–1710 kHz
- AM in Asia: 522–1710 kHz
- SW: 2300–23000 kHz
- LW: 153–279 kHz

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	AMSKFREQH[15:0]															

Bit	Name	Function
15:0	AMSKFREQH	**AM Seek Band Top.** Specify the higher boundary of the AM band when performing a seek. The seek either stops at this limit or wraps based on the parameters of AM_SEEK_START command that was issued to initiate a seek. The default value for the upper boundary of the AM band is 1710 kHz.

Property 0x3402. AM_SEEK_FREQ_SPACING

Sets the frequency spacing for the AM Band when performing a seek. The frequency spacing determines how far the next tune is going to be from the currently tuned frequency. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default frequency spacing is 10 kHz.

Available in: All

Default: 0x000A

Units: kHz

Valid Values: 1 (1 kHz), 5 (5 kHz), 9 (9 kHz), and 10 (10 kHz).

Recommended Value:

- AM in US: 10 (10 kHz)
- AM in Asia: 9 (9 kHz)
- SW: 5 (5 kHz)
- LW: 9 (9 kHz)

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	AMSKSPACE[3:0]			

Bit	Name	Function
15:4	Reserved	Always write to 0.
3:0	AMSKSPACE	**AM Seek Frequency Spacing.** Sets the frequency spacing when performing a seek in the AM band. The default frequency spacing is 10 kHz.

Property 0x3403. AM_SEEK_TUNE_SNR_THRESHOLD

Sets the SNR threshold for a valid AM Seek/Tune. If the value is zero, then SNR is not used as a valid criteria when doing a seek for AM. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default threshold is 5 dB.

Available in: All

Default: 0x0005

Units: dB

Step: 1

Range: 0–63

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	AMSKSNR[5:0]					

Bit	Name	Function
15:6	Reserved	Always write to 0.
5:0	AMSKSNR	**AM Seek/Tune SNR Threshold.** SNR Threshold which determines if a valid channel has been found during Seek/Tune. Specified in units of dB in 1 dB steps (0–63). Default threshold is 5 dB.

Property 0x3404. AM_SEEK_TUNE_RSSI_THRESHOLD

Sets the RSSI threshold for a valid AM Seek/Tune. If the value is zero then RSSI is not used as a valid criteria when doing a seek for AM. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 25 dBµV.

Available in: All

Default: 0x0019

Units: dBµV

Step: 1

Range: 0–63

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	AMSKRSSI[5:0]					

Bit	Name	Function
15:6	Reserved	Always write to 0.
5:0	AMSKRSSI	**AM Seek/Tune Received Signal Strength Threshold.** RSSI Threshold which determines if a valid channel has been found during Seek/Tune. Specified in units of dBµV in 1 dBµV steps (0–63). Default threshold is 25 dBµV.

Property 0x3702. AM_AGC_ATTACK_RATE

Sets the AGC attack rate. Large values provide slower attack, and smaller values provide faster attack. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read in POWERUP mode. The default is 4 (approximately 1400 dB/s).

$$\text{AGC Attack Rate (dB/s)} = \frac{5600}{\text{ATTACK}[7:0]}$$

Nominal "5600" is based on Skyworks' AM antenna dummy and Si474xEVB reference design and may vary with source impedance and design changes. In most systems, an exact value is not important. However, to calculate for a different source impedance and/or design:

1. Drive antenna input with desired source impedance (via antenna or antenna dummy).
2. Increase RF level until AGC index changes from 19 to 20. Record last RF level with index equal 19.
3. Increase RF level until AGC index reaches 39. Record RF level with index equal 39.
4. Replace “5600” in rate equation with “(RF39 – RF19)/0.00667”.

Available in: Si4740/41/42/43/44/45

Default: 0x0004

Step: 4

Range: 4–248

Notes:

1. Was property 0x4102 in FW2.C.

2. For FW2.E, attack rate may be faster than programmed depending on initial and final RF levels.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	ATTACK [7:0]							

Property 0x3703. AM_AGC_RELEASE_RATE

Sets the AGC release rate. Larger values provide slower release, and smaller values provide faster release. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read in POWERUP mode. The default is 140 (approximately 40 dB/s).

$$\text{AGC Release Rate (dB/s)} = \frac{5600}{\text{RELEASE}[7:0]}$$

Nominal "5600" is based on Skyworks' AM antenna dummy and Si474xEVB reference design and may vary with source impedance and design changes. In most systems, an exact value is not important. However, to calculate for a different source impedance and/or design:

1. Drive antenna input with desired source impedance (via antenna or antenna dummy).
2. Increase RF level until AGC index changes from 19 to 20. Record last RF level with index equal 19.
3. Increase RF level until AGC index reaches 39. Record RF level with index equal 39.
4. Replace "5600" in rate equation with "(RF39 – RF19)/0.00667".

Available in: Si4740/41/42/43/44/45

Default: 0x008C

Step: 4

Range:4–248

Note: Was property 0x4103 in FW2.C.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	RELEASE [7:0]						

Property 0x3705. AM_FRONTEND_AGC_CONTROL

Adjusts the AM AGC for external front-end attenuator and external front-end cascode LNA. This property contains two fields: MIN_GAIN_INDEX and ATTN_BACKUP. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 0x130C (MIN_AGC_INDEX=19 and ATTN_BACKUP=12).

Available in: Si4740/41/42/43/44/45

Default: 0x130C

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	MIN_GAIN_INDEX[7:0]								ATTN_BACKUP[7:0]							

MIN_GAIN_INDEX impacts sensitivity and U/D performance. Lower values improve sensitivity, but degrade far away blocker U/D performance. [Note: Values below 19 have minimal sensitivity improvement.] Higher values degrade sensitivity, but improve U/D. With MIN_GAIN_INDEX=19 and Si4743 EVB reference design, the Si474x provides sensitivity of 28dBuV typical and U/D exceeding 55dB on far away blockers. With MIN_GAIN_INDEX=24, the Si474x provides sensitivity of 34dBuV typical and U/D approaching 70dB on far away blockers.

The recommended MIN_GAIN_INDEX optimization procedure is:

1. Determine source impedance and AM antenna dummy.
2. Determine sensitivity RF input and SINAD requirements.
3. Set frequency to 1000kHz.
4. With source impedance in #1 and RF input in #2, adjust MIN_GAIN_INDEX until SINAD requirements are achieved with minimum necessary margin.

5. Program this value into Si474x MIN_GAIN_INDEX as part of initialization after POWERUP command.

ATTN_BACKUP insures the AGC gain indexes are monotonic and is used when the external attenuator is engaged via GPO1/AGC2. The actual attenuation achieved depends on the source impedance or AM antenna dummy. Since AGC gain implementation is subject to change, the optimum value is best determined with specific antenna and board design.

The recommend ATTN_BACKUP optimization procedure is:

1. Determine source impedance and AM antenna dummy.
2. Determine maximum RF input and associated SINAD requirements.
3. Set frequency to 1710kHz.
4. With ATTN_BACKUP set to 12 (default), disable the AGC at AMAGCNDX=47 using AM_AGC_OVERRIDE command.
5. With source impedance in #1 and RF input in #2, adjust attenuator impedance until SINAD requirements are achieved with minimum necessary margin. For Si4743EVB Rev 1.3, C7 (1200pF) attenuates against passive antenna sources and R8 (1 ohm) attenuates against active (50 ohm) sources.
6. Enable the AGC using AM_AGC_OVERRIDE.
7. Sweep the RF input from 0 to 126 dBuV and then from 126 to 0 dBuV in 1 dB steps and observe the AMAGCNDX at each RF level using AM_AGC_STATUS command.
8. If AMAGCNDX is observed to oscillate at any RF level, increase ATTN_BACKUP by 1 and repeat from step 7.
9. If AMAGCNDX is observed not to oscillate at any RF level, decrease ATTN_BACKUP by one and repeat from step 7.
10. Add one to smallest ATTN_BACKUP for which no oscillations are observed and program this value into Si474x ATTN_BACKUP as part of initialization after POWERUP command.

Table 16. Recommended Values for MIN_GAIN_INDEX and ATTN_BACKUP with FW2.E and later, Si4743EVB Rev 1.3 and Various AM Antenna Dummies

AM Antenna Dummy	MIN_GAIN_INDEX	ATTN_BACKUP
50 Ω/15 pF/62 pF (Skyworks)	19	12
50 Ω/40 pF/40 pF	19	12
50MN Series	19	12
Active (50 Ω)	19	20

Property 0x3900. AM_NB_DETECT_THRESHOLD

Sets the threshold for detecting impulses in dB above the noise floor. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read in POWERUP mode. The default is 12 dB.

Available in: Si4742/43/44/45

Default: 0x000C

Range: 0–90

Note: Was property 0x4105 in FW2.C.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	NB_DETECT_THRESHOLD [15:0]															

Property 0x3901. AM_NB_INTERVAL

Interval in micro-seconds that original samples are replaced by sample-hold clean samples. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read in POWERUP mode. The default is 55 µs.

Available in: Si4742/43/44/45

Default: 0x0037

Range: 15–110

Note: Was property 0x4106 in FW2.C.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	NB_INTERVAL [15:0]															

Property 0x3902. AM_NB_RATE

Noise blanking rate in 100 Hz units. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read in POWERUP mode. The default is 64 (6400 Hz).

Available in: Si4742/43/44/45

Default: 0x0040

Range: 1–64

Note: Was property 0x4107 in FW2.C.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	NB_RATE [15:0]															

Property 0x3903. AM_NB_IIR_FILTER

Sets the bandwidth of the noise floor estimator. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read in POWERUP mode. The default is 300 (465 Hz).

Bandwidth (Hz) = NB_IIR_FILTER[15:0] x 1.55

Available in: Si4742/43/44/45

Default: 0x012C

Range: 300–1600

Note: Was property 0x4108 in FW2.C.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	NB_IIR_FILTER [15:0]															

Property 0x3904. AM_NB_DELAY

Delay in micro-seconds before applying impulse blanking to the original samples. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read in POWERUP mode. The default is 172 µs.

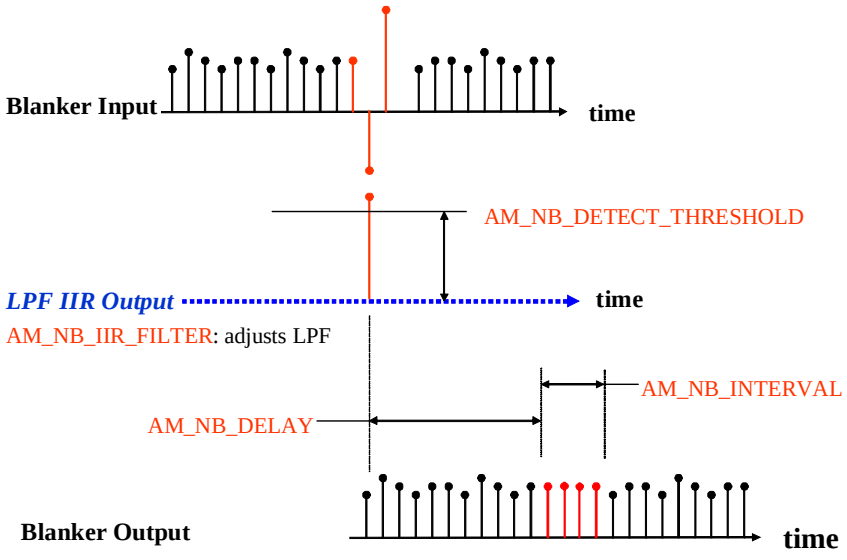
Available in: Si4742/43/44/45

Default: 0x00AC

Range: 125–219

Note: Was property 0x4109 in FW2.C.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	NB_DELAY [15:0]															



AM_NB_RATE: sets maximum repeat rate NB is allowed to fire.

Figure 14. AM Noise Blanker

Property 0x4000. RX_VOLUME

Sets the audio output volume. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 63.

Available in: All

Default: 0x003F

Step: 1

Range: 0–63

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	VOL[5:0]					

Bit	Name	Function
15:6	Reserved	Always write to 0.
5:0	VOL	**Output Volume.** Sets the output volume level, 63 max, 0 min. Default is 63.

Property 0x4001. RX_HARD_MUTE

Mutes the audio output. L and R audio outputs may not be muted independently. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is unmute (0x0000).

Available in: All

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LMUTE	RMUTE

Bit	Name	Function
15:2	Reserved	Always write to 0.
1	LMUTE	Mutes both L and R Audio Outputs.
0	RMUTE	Mutes both L and R Audio Outputs.

5.4. Commands and Properties for the WB Receiver (Si4707/36/37/38/39/42/43)

The following two tables are the summary of the commands and properties for the Weather Band Receiver component applicable to Si4707/36/37/38/39/42/43.

Table 17. WB Receiver Command Summary

Cmd	Name	Description	Available In
0x01	POWER_UP	Power up device and mode selection.	All
0x10	GET_REV	Returns revision information on the device.	All
0x11	POWER_DOWN	Power down device.	All
0x12	SET_PROPERTY	Sets the value of a property.	All
0x13	GET_PROPERTY	Retrieves a property's value.	All
0x14	GET_INT_STATUS	Reads interrupt status bits.	All
0x15	PATCH_ARGS*	Reserved command used for patch file downloads.	All
0x16	PATCH_DATA*	Reserved command used for patch file downloads.	All
0x50	WB_TUNE_FREQ	Selects the WB tuning frequency.	All
0x52	WB_TUNE_STATUS	Queries the status of previous WB_TUNE_FREQ or WB_SEEK_START command.	All
0x53	WB_RSQ_STATUS	Queries the status of the Received Signal Quality (RSQ) of the current channel	All
0x54	WB_SAME_STATUS	Retrieves Specific Area Message Encoding (SAME) information and acknowledges SAMEINT interrupts.	Si4707
0x55	WB_ASQ_STATUS	Queries the status of the 1050 kHz alert tone in Weather Band.	All
0x57	WB_AGC_STATUS	Queries the current AGC settings	All
0x58	WB_AGC_OVERRIDE	Override AGC setting by disabling and forcing it to a fixed value	All
0x80	GPIO_CTL	Configures GPO1, 2, and 3 as output or Hi-Z	All
0x81	GPIO_SET	Sets GPO1, 2, and 3 output level (low or high)	All

***Note:** Commands PATCH_ARGS and PATCH_DATA are only used to patch firmware. For information on applying a patch file, see "7.2. Powerup from a Component Patch" on page 233.

Table 18. WB Receive Property Summary

Prop	Name	Description	Default	Available In
0x0001	GPO_IEN	Enables interrupt sources.	0x0000	All
0x0102	DIGITAL_OUTPUT_ FORMAT	Configure digital audio outputs.	0x0000	Si4737/39/43
0x0104	DIGITAL_OUTPUT_ SAMPLE_RATE	Configure digital audio output sample rate.	0x0000	Si4737/39/43
0x0201	REFCLK_FREQ	Sets frequency of reference clock in Hz. The range is 31130 to 34406 Hz, or 0 to disable the AFC. Default is 32768 Hz.	0x8000	All
0x0202	REFCLK_PRESCALE	Sets the prescaler value for RCLK input.	0x0001	All
0x5108	WB_MAX_TUNE_ERROR	Sets the maximum freq error allowed before setting the AFC_RAIL indicator. Default value is 10 kHz.	0x000A	All
0x5200	WB_RSQ_INT_SOURCE	Configures interrupt related to Received Signal Quality metrics.	0x0000	All
0x5201	WB_RSQ_SNR_HI_THRESHOLD	Sets high threshold for SNR interrupt.	0x007F	All
0x5202	WB_RSQ_SNR_LO_THRESHOLD	Sets low threshold for SNR interrupt.	0x0000	All
0x5203	WB_RSQ_RSSI_HI_THRESHOLD	Sets high threshold for RSSI interrupt.	0x007F	All
0x5204	WB_RSQ_RSSI_LO_THRESHOLD	Sets low threshold for RSSI interrupt.	0x0000	All
0x5403	WB_VALID_SNR_THRESHOLD	Sets SNR threshold to indicate a valid channel	0x0003	All
0x5404	WB_VALID_RSSI_THRESHOLD	Sets RSSI threshold to indicate a valid channel	0x0014	All
0x5500	WB_SAME_INTERRUPT_SOURCE	Configures SAME interrupt sources.	0x0000	Si4707
0x5600	WB_ASQ_INT_SOURCE	Configures interrupt related to the 1050 kHz alert tone	0x0000	All
0x4000	RX_VOLUME	Sets the output volume.	0x003F	All
0x4001	RX_HARD_MUTE	Mutes the audio output. L and R audio outputs may not be muted independently.	0x0000	All

Table 19. Status Response for the WB Receiver

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	SAMEINT	ASQINT	STCINT

Bit	Name	Function
7	CTS	**Clear to Send.** 0 = Wait before sending next command. 1 = Clear to send next command.
6	ERR	**Error.** 0 = No error 1 = Error
5:4	Reserved	Values may vary.
3	RSQINT	**Received Signal Quality Interrupt.** 0 = Received Signal Quality measurement has not been triggered. 1 = Received Signal Quality measurement has been triggered.
2	SAMEINT	**SAME Interrupt (Si4707 Only).** 0 = SAME interrupt has not been triggered. 1 = SAME interrupt has been triggered.
1	ASQINT	**Audio Signal Quality Interrupt.** 0 = Audio Signal Quality measurement has not been triggered. 1 = Audio Signal Quality measurement has been triggered.
0	STCINT	**Seek/Tune Complete Interrupt.** 0 = Tune complete has not been triggered. 1 = Tune complete interrupt has been triggered.

5.4.1. WB Receiver Commands

Command 0x01. POWER_UP

Initiates the boot process to move the device from powerdown to powerup mode. The boot can occur from internal device memory or a system controller downloaded patch. To confirm that the patch is compatible with the internal device library revision, the library revision should be confirmed by issuing the POWER_UP command with FUNC = 15 (query library ID). The device returns the response, including the library revision, and then moves into powerdown mode. The device can then be placed in powerup mode by issuing the POWER_UP command with FUNC = 3 (WB Receive) and the patch may be applied.

The POWER_UP command configures the state of ROUT (pin 13), LOUT (pin 14) for analog audio mode. For Si4743 component 2A or higher, the POWER_UP command also configures the state of GPO3/DCLK (pin 19), DFS (pin 18), and DOUT (pin 17) for digital audio mode. The command configures GPO2/INT~ interrupts (GPO2OEN) and CTS interrupts (CTSIEN). If both are enabled, GPO2/IRQ is driven high during normal operation and low for a minimum of 1 µs during the interrupt. The CTSIEN bit is duplicated in the GPO_IEN property. The command is complete when the CTS bit (and optional interrupt) is set.

To change function (e.g., WB RX to FM RX), issue POWER_DOWN command to stop current function; then, issue POWER_UP to start new function.

Note: Delay at least 500 ms between powerup command and first tune command to wait for the oscillator to stabilize if XOSCEN is set and crystal is used as the RCLK.

Available in: All

Command Arguments: Two

Response Bytes: None (FUNC=3), Seven (FUNC=15)

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	0	0	0	0	1
ARG1	CTSIEN	GPO2OEN	PATCH	XOSCEN	FUNC[3:0]			
ARG2	OPMODE[7:0]							

Arg	Bit	Name	Function
1	7	CTSIEN	**CTS Interrupt Enable.** 0 = CTS interrupt disabled. 1 = CTS interrupt enabled.
1	6	GPO2OEN	**GPO2 Output Enable.** 0 = GPO2 output disabled. 1 = GPO2 output enabled.
1	5	PATCH	**Patch Enable.** 0 = Boot normally 1 = Copy NVM to RAM, but do not boot. After CTS has been set, RAM may be patched
1	4	XOSCEN	**Crystal Oscillator Enable.** 0 = Use external RCLK (crystal oscillator disabled) 1 = Use crystal oscillator (RCLK and GPO3/DCLK with external 32.768kHz crystal and OPMODE = 00000101) See Si47xx Data Sheet Application Schematic for external BOM details.
1	3:0	FUNC[3:0]	**Function.** 3 = WB Receive. 0–2, 4–14 = Reserved 15 = Query Library ID.
2	7:0	OPMODE[7:0]	**Application Setting** 00000101 = Analog audio outputs (LOUT/ROUT) 00001011 = Digital audio output (DCLK, LOUT/DFS, ROUT/DIO) 10110000 = Digital audio outputs (DCLK, DFS, DIO) (Si4743 component 2.A or higher with XOSCEN = 0) 10110101 = Analog and digital outputs (LOUT/ROUT and DCLK, DFS, DIO) (Si4743 component 2.A or higher with XOSCEN = 0)

Response (FUNC = 3, WB Receive)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	SAMEINT	ASQINT	STCINT

Response (FUNC = 15, Query Library ID)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	SAMEINT	ASQINT	STCINT
RESP1	PN[7:0]							
RESP2	FWMAJOR[7:0]							
RESP3	FWMINOR[7:0]							
RESP4	RESERVED[7:0]							
RESP5	RESERVED[7:0]							
RESP6	CHIPREV[7:0]							
RESP7	LIBRARYID[7:0]							

RESP	Bit	Name	Function
1	7:0	PN[7:0]	**Final 2 digits of part number (HEX).**
2	7:0	FWMAJOR[7:0]	**Firmware Major Revision (ASCII).**
3	7:0	FWMINOR[7:0]	**Firmware Minor Revision (ASCII).**
4	7:0	RESERVED[7:0]	**Reserved, various values.**
5	7:0	RESERVED[7:0]	**Reserved, various values.**
6	7:0	CHIPREV[7:0]	**Chip Revision (ASCII).**
7	7:0	LIBRARYID[7:0]	**Library Revision (HEX).**

Command 0x10. GET_REV

Returns the part number, chip revision, firmware revision, patch revision and component revision numbers. The command is complete when the CTS bit (and optional interrupt) is set. This command may only be sent when in powerup mode.

Available in: All

Command arguments: None

Response bytes: Eight

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	0	0

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	SAMEINT	ASQINT	STCINT
RESP1	PN[7:0]							
RESP2	FWMAJOR[7:0]							
RESP3	FWMINOR[7:0]							
RESP4	$PATCH_H$[7:0]							
RESP5	$PATCH_L$[7:0]							
RESP6	CMPMAJOR[7:0]							
RESP7	CMPMINOR[7:0]							
RESP8	CHIPREV[7:0]							

RESP	Bit	Name	Function
1	7:0	PN[7:0]	**Final 2 digits of Part Number**
2	7:0	FWMAJOR[7:0]	**Firmware Major Revision**
3	7:0	FWMINOR[7:0]	**Firmware Minor Revision**
4	7:0	$PATCH_H$[7:0]	**Patch ID High Byte**
5	7:0	$PATCH_L$[7:0]	**Patch ID Low Byte**
6	7:0	CMPMAJOR[7:0]	**Component Major Revision**
7	7:0	CMPMINOR[7:0]	**Component Minor Revision**
8	7:0	CHIPREV[7:0]	**Chip Revision**

Command 0x11. POWER_DOWN

Moves the device form powerup to powerdown mode. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode. Note that only the POWER_UP command is accepted in powerdown mode. **If the system controller writes a command other than POWER_UP when in powerdown mode, the device does not respond. The device will only respond when a POWER_UP command is written.**

Note: The following describes the state of all the pins when in powerdown mode:
GPIO1, GPIO2, and GPIO3 = 0
ROUT, LOUT, DOUT, DFS = Hiz.

Available in: All

Command arguments: None

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	0	1

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	SAMEINT	ASQINT	STCINT

Command 0x12. SET_PROPERTY

Sets a property shown in Table 18, “WB Receive Property Summary,” on page 171. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode.

Available in: All

Command Arguments: Five

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	1	0
ARG1	0	0	0	0	0	0	0	0
ARG2	$PROP_H$[7:0]							
ARG3	$PROP_L$[7:0]							
ARG4	$PROPV_H$[7:0]							
ARG5	$PROPV_L$[7:0]							

Arg	Bit	Name	Function
1	7:0	Reserved	Always write to 0.
2	7:0	$PROP_H$[7:0]	**Property High Byte.** This byte in combination with $PROP_L$ is used to specify the property to modify.
3	7:0	$PROP_L$[7:0]	**Property Low Byte.** This byte in combination with $PROP_H$ is used to specify the property to modify.
4	7:0	$PROPV_H$[7:0]	**Property Value High Byte.** This byte in combination with $PROPV_L$ is used to set the property value.
5	7:0	$PROPV_L$[7:0]	**Property Value Low Byte.** This byte in combination with $PROPV_H$ is used to set the property value.

Command 0x13. GET_PROPERTY

Gets a property as shown in Table 18, “WB Receive Property Summary,” on page 171. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode.

Available in: All

Command arguments: Three

Response bytes: Three

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	1	1
ARG1	0	0	0	0	0	0	0	0
ARG2	$PROPG_H$[7:0]							
ARG3	$PROPG_L$[7:0]							

Arg	Bit	Name	Function
1	7:0	Reserved	Always write to 0.
2	7:0	$PROPG_H$[7:0]	**Property High Byte.** This byte in combination with $PROP_L$ is used to specify the property to get.
3	7:0	$PROPG_L$[7:0]	**Property Low Byte.** This byte in combination with $PROP_H$ is used to specify the property to get.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	SAMEINT	ASQINT	STCINT
RESP1	0	0	0	0	0	0	0	0
RESP2	$PROPV_H[7:0]$							
RESP3	$PROPV_L[7:0]$							

RESP	Bit	Name	Function
1	7:0	Reserved	Always returns 0.
2	7:0	$PROPV_H[7:0]$	**Property Value High Byte.** This byte in combination with $PROPV_L$ will represent the requested property value.
3	7:0	$PROPV_L[7:0]$	**Property Value High Byte.** This byte in combination with $PROPV_H$ will represent the requested property value.

Command 0x14. GET_INT_STATUS

Updates bits 6:0 of the status byte. This command should be called after any command that sets the STCINT, RSQINT, SAMEINT (Si4707 only), or ASQINT bits. When polling this command should be periodically called to monitor the status byte, and when using interrupts, this command should be called after the interrupt is set to updated the status byte. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode.

Available in: All

Command arguments: None

Response bytes: One

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	1	0	0

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	SAMEINT	ASQINT	STCINT

Command 0x50. WB_TUNE_FREQ

Sets the WB Receive to tune the frequency between 162.4 MHz and 162.55 MHz in 2.5 kHz units. For example 162.4 MHz = 64960 and 162.55 MHz = 65020. The CTS bit (and optional interrupt) is set when it is safe to send the next command. The ERR bit (and optional interrupt) is set if an invalid argument is sent. Note that only a single interrupt occurs if both the CTS and ERR bits are set. The optional STC interrupt is set when the command completes. The STCINT bit is set only after the GET_INT_STATUS command is called. This command may only be sent when in powerup mode. The command clears the STC bit if it is already set.

Available in: All

Command arguments: Three

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	1	0	1	0	0	0	0
ARG1	0	0	0	0	0	0	0	0
ARG2	$FREQ_H$[7:0]							
ARG3	$FREQ_L$[7:0]							

Arg	Bit	Name	Function
1	7:0	Reserved	Always write to 0.
2	7:0	$FREQ_H$[7:0]	**Tune Frequency High Byte.** This byte in combination with $FREQ_L$ selects the tune frequency in kHz. In WB mode the valid range is from 64960 to 65020 (162.4–162.55 MHz).
3	7:0	$FREQ_L$[7:0]	**Tune Frequency Low Byte.** This byte in combination with $FREQ_H$ selects the tune frequency in kHz. In WB mode the valid range is from 64960 to 65020 (162.4–162.55 MHz).

Command 0x52. WB_TUNE_STATUS

Returns the status of WB_TUNE_FREQ. The commands returns the current frequency, and RSSI/SNR at the moment of tune. The command clears the STCINT interrupt bit when INTACK bit of ARG1 is set. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode.

Available in: All

Command arguments: One

Response bytes: Five

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	1	0	1	0	0	1	0
ARG1	0	0	0	0	0	0	0	INTACK

Arg	Bit	Name	Function
1	7:1	Reserved	Always write to 0.
1	0	INTACK	**Seek/Tune Interrupt Clear.** If set this bit clears the seek/tune complete interrupt status indicator.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	SAMEINT	ASQINT	STCINT
RESP1	X	X	X	X	X	X	AFCRL	VALID
RESP2	$READFREQ_H$[7:0]							
RESP3	$READFREQ_L$[7:0]							
RESP4	RSSI[7:0]							
RESP5	SNR[7:0]							

Data	Bit	Name	Function
1	7:2	Reserved	Always returns 0.
1	1	AFCRL	**AFC Rail Indicator.** This bit will be set if the AFC rails.
1	0	VALID	**Valid Channel.** Confirms if the tuned channel is currently valid.
2	7:0	$READFREQ_H$[7:0]	**Read Frequency High Byte.** This byte in combination with $READFREQ_L$ returns frequency being tuned.
3	7:0	$READFREQ_L$[7:0]	**Read Frequency Low Byte.** This byte in combination with $READFREQ_H$ returns frequency being tuned.
4	7:0	RSSI[7:0]	**Received Signal Strength Indicator.** This byte will contain the receive signal strength at the tuned frequency.
5	7:0	SNR[7:0]	**SNR.** This byte will contain the SNR metric at the tuned frequency.

Command 0x53. WB_RSQ_STATUS

Returns status information about the received signal quality. The commands returns the RSSI, SNR, and frequency offset. It also indicates whether the frequency is a currently valid frequency as indicated by VALID, and whether the AFC is railed or not as indicated by AFCRL. This command can be used to check if the received signal is above the RSSI high threshold as reported by RSSIHINT, or below the RSSI low threshold as reported by RSSILINT. It can also be used to check if the received signal is above the SNR high threshold as reported by SNRHINT, or below the SNR low threshold as reported by SNRLINT. The command clears the STCINT interrupt bit when INTACK bit of ARG1 is set. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode.

Available in: All

Command arguments: One

Response bytes: Seven

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	1	0	1	0	0	1	1
ARG1	0	0	0	0	0	0	0	INTACK

Arg	Bit	Name	Function
1	0	INTACK	**Interrupt Acknowledge** 0 = Interrupt status preserved. 1 = Clears RSQINT, SNRHINT, SNRLINT, RSSIHINT, RSSILINT

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	SAMEINT	ASQINT	STCINT
RESP1	X	X	X	X	SNRHINT	SNRLINT	RSSIHINT	RSSIILINT
RESP2	X	X	X	X	X	X	AFCRL	VALID
RESP3	X	X	X	X	X	X	X	X
RESP4	RSSI[7:0]							
RESP5	ASNR[7:0]							
RESP6	X	X	X	X	X	X	X	X
RESP7	FREQOFF[7:0]							

Data	Bit	Name	Function
1	3	SNRHINT	**SNR Detect High.** 0 = Received SNR has not exceeded above SNR high threshold. 1 = Received SNR has exceeded above SNR high threshold.
1	2	SNRLINT	**SNR Detect Low.** 0 = Received SNR has not exceeded below SNR low threshold. 1 = Received SNR has exceeded below SNR low threshold.
1	1	RSSIHINT	**RSSI Detect High.** 0 = RSSI has not exceeded above RSSI high threshold. 1 = RSSI has exceeded above RSSI high threshold.
1	0	RSSILINT	**RSSI Detect Low.** 0 = RSSI has not exceeded below RSSI low threshold. 1 = RSSI has exceeded below RSSI low threshold.
2	1	AFCRL	**AFC Rail Indicator.** This bit will be set if the AFC rails.
2	0	VALID	**Valid Channel.** Confirms if the channel is currently valid.
4	7:0	RSSI[7:0]	**Received Signal Strength Indicator.** This byte will contain the receive signal strength at the tuned frequency.
5	7:0	SNR[7:0]	**SNR.** This byte will contain the SNR metric at the tuned frequency.
7	7:0	FREQOFF[7:0]	**Frequency Offset.** Signed frequency offset in kHz.

Command 0x54. WB_SAME_STATUS

Retrieves SAME information, acknowledges SAMEINT interrupts and clears the message buffer. The command indicates whether the start of message, end of message or preamble is detected and if the header buffer is ready. The state of the decoder, message length, and 8 bytes of the message buffer with corresponding confidence level is returned. The byte at address 0 will be the first byte following the header block identifier "ZCZC", typically "-" (Dash). Each byte has an associated confidence metric ranging from 0 (low confidence) to 3 (high confidence).

Available in: Si4707

Command Arguments: Two

Response Bytes: Thirteen

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	1	0	1	0	1	0	0
ARG1	0	0	0	0	0	0	CLRBUF	INTACK
ARG2	READADDR[7:0]							

Arg	Bit	Name	Function
1	7:2	Reserved	Always write to 0.
1	1	CLRBUF	**Clear Buffer** 0 = Message Buffer preserved. 1 = Clears the contents of the SAME Message Buffer. Clears the contents of the SAME Message Buffer if set. The buffer will always be cleared during WB_TUNE_FREQ. If the buffer is not cleared then each message received will be combined with the previously received message to increase the certainty of the message content. After receipt of an End-of-Message, this buffer must be cleared by the user. To prevent different headers from being combined into an incorrect message, the user must clear the buffer before a new header is transmitted. As there is no indication that a new header is about to be transmitted, the user must rely on other events to indicate when to clear the buffer. The buffer should be cleared after receipt of three headers, after the end-of-message marker, when the 1050 Hz alert tone has been detected or 6 seconds after the reception of the last header was completed and no new preamble has been detected. Once the buffer has been cleared, it will remain empty until the next start-of-message is received. Alternatively, the user may clear the buffer after each header is received and rely on a traditional best 2-of-3 voting method. In this case, no message combining is performed.
1	0	INTACK	**Interrupt Acknowledge** 0 = Interrupt status preserved. 1 = Clears SAMEINT.
2	[7:0]	READADDR[7:0]	Byte in the message buffer to start reading from. Note that 8 bytes will always be returned, however the WB_SAME_STATUS:MSGLEN will report the total length of the message and the user must disregard bytes past this length.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	SAMEINT	ASQINT	STCINT
RESP1	X	X	X	X	EOMDET	SOMDET	PREDET	HDRRDY
RESP2	STATE[7:0]							
RESP3	MSGLEN[7:0]							
RESP4	CONF7[1:0]		CONF6[1:0]		CONF5[1:0]		CONF4[1:0]	
RESP5	CONF3[1:0]		CONF2[1:0]		CONF1[1:0]		CONF0[1:0]	
RESP6	DATA0[7:0]							
RESP7	DATA1[7:0]							
RESP8	DATA2[7:0]							
RESP9	DATA3[7:0]							
RESP10	DATA4[7:0]							
RESP11	DATA5[7:0]							
RESP12	DATA6[7:0]							
RESP13	DATA7[7:0]							

RESP	Bit	Name	Function
1	3	EOMDET	**End Of Message Detected** 1 = End of message is detected.
1	2	SOMDET	**Start Of Message Detected** 1 = start of message is detected.
1	1	PREDET	**Preamble Detected** 1 = Preamble is detected.
1	0	HDRRDY	**Header Buffer Ready** 1 = Header buffer is ready.
2	[7:0]	STATE[7:0]	**State Machine Status** 0 = End of message. 1 = Preamble detected. 2 = Receiving SAME header message. 3 = SAME header message complete.

RESP	Bit	Name	Function
3	[7:0]	MSGLEN[7:0]	**SAME Message Length** SAME Message length in bytes. This length excludes the preamble and the header code block identifier "ZCZC". If message combining is used, the value reported is the length of the longest message received.
4	[7:6]	CONF7[1:0]	Confidence Metric for DATA7 represented as a number between 0 (low) and 3 (high).
4	[5:4]	CONF6[1:0]	Confidence Metric for DATA6 represented as a number between 0 (low) and 3 (high).
4	[3:2]	CONF5[1:0]	Confidence Metric for DATA5 represented as a number between 0 (low) and 3 (high).
4	[1:0]	CONF4[1:0]	Confidence Metric for DATA4 represented as a number between 0 (low) and 3 (high).
5	[7:6]	CONF3[1:0]	Confidence Metric for DATA3 represented as a number between 0 (low) and 3 (high).
5	[5:4]	CONF2[1:0]	Confidence Metric for DATA2 represented as a number between 0 (low) and 3 (high).
5	[3:2]	CONF1[1:0]	Confidence Metric for DATA1 represented as a number between 0 (low) and 3 (high).
5	[1:0]	CONF0[1:0]	Confidence Metric for DATA0 represented as a number between 0 (low) and 3 (high).
6	[7:0]	DATA0[7:0]	Byte of message read at address, READADDR + 0
7	[7:0]	DATA1[7:0]	Byte of message read at address, READADDR + 1
8	[7:0]	DATA2[7:0]	Byte of message read at address, READADDR + 2
9	[7:0]	DATA3[7:0]	Byte of message read at address, READADDR + 3
10	[7:0]	DATA4[7:0]	Byte of message read at address, READADDR + 4
11	[7:0]	DATA5[7:0]	Byte of message read at address, READADDR + 5
12	[7:0]	DATA6[7:0]	Byte of message read at address, READADDR + 6
13	[7:0]	DATA7[7:0]	Byte of message read at address, READADDR + 7

Command 0x55. WB_ASQ_STATUS

Returns status information about the 1050kHz alert tone in Weather Band. The commands returns the alert on/off Interrupt and the present state of the alert tone. The command clears the ASQINT bit when INTACK bit of ARG1 is set. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode.

Available in: All

Command arguments: One

Response bytes: Two

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	1	0	1	0	1	0	1
ARG1	0	0	0	0	0	0	0	INTACK

Arg	Bit	Name	Function
1	7:1	Reserved	Always write to 0.
1	0	INTACK	**Interrupt Acknowledge** 0 = Interrupt status preserved. 1 = Clears ASQINT, ALERTOFF_INT, ALERTON_INT

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	SAMEINT	ASQINT	STCINT
RESP1	X	X	X	X	X	X	ALERTOFF_INT	ALERTON_INT
RESP2	X	X	X	X	X	X	X	ALERT

Data	Bit	Name	Function
1	1	ALERTOFF_INT	**ALERTOFF_INT.** 0 = 1050 Hz alert tone has not been detected to be absent since the last WB_TUNE_FREQ or WB_RSQ_STATUS with INTACK = 1. 1 = 1050 Hz alert tone has been detected to be absent since the last WB_TUNE_FREQ or WB_RSQ_STATUS with INTACK = 1.
1	0	ALERTON_INT	**ALERTON_INT.** 0 = 1050 Hz alert tone has not been detected to be present since the last WB_TUNE_FREQ or WB_RSQ_STATUS with INTACK = 1. 1 = 1050 Hz alert tone has been detected to be present since the last WB_TUNE_FREQ or WB_RSQ_STATUS with INTACK = 1.
2	0	ALERT	**ALERT.** 0 = 1050 Hz alert tone is currently not present. 1 = 1050 Hz alert tone is currently present.

Command 0x57. WB_AGC_STATUS

Returns the AGC setting of the device. The command returns whether the AGC is enabled or disabled. This command may only be sent when in powerup mode.

Available in: All

Command arguments: None

Response bytes: One

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	1	0	1	0	1	1	1

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	SAMEINT	ASQINT	STCINT
RESP1	X	X	X	X	X	X	X	READ_RFAGCDIS

RESP	Bit	Name	Function
1	0	READ_RFAGCDIS	This bit indicates whether the RF AGC is disabled or not 0 = RF AGC is enabled. 1 = RF AGC is disabled.

Command 0x58. WB_AGC_OVERRIDE

Overrides AGC setting by disabling the AGC and forcing the LNA to have a certain gain that ranges between 0 (minimum attenuation) and 26 (maximum attenuation). This command may only be sent when in powerup mode.

Available in: All

Command arguments: One

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	1	0	1	1	0	0	0
ARG1	X	X	X	X	X	X	X	RFAGCDIS

ARG	Bit	Name	Function
1	7:1	Reserved	Always write to 0.
1	0	RFAGCDIS	This bit selects whether the RF AGC is disabled or not 0 = RF AGC is enabled. 1 = RF AGC is disabled.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	SAMEINT	ASQINT	STCINT

Command 0x80. GPIO_CTL

Enables output for GPO1, 2, and 3. GPO1, 2, and 3 can be configured for output (Hi-Z or active drive) by setting the GPO1OEN, GPO2OEN, and GPO3OEN bit. The state (high or low) of GPO1, 2, and 3 is set with the GPIO_SET command. To avoid excessive current consumption due to oscillation, GPO pins should not be left in a high impedance state. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode. The default is all GPO pins set for high impedance.

Notes:

1. The use of GPO2 as an interrupt pin will override this GPIO_CTL function for GPO2.
2. GPO1 is not configurable as an output for Si4740/41/42/43/44/45.

Available in: All

Command arguments: One

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	1	0	0	0	0	0	0	0
ARG1	0	0	0	0	GPO3OEN	GPO2OEN	GPO1OEN	0

ARG	Bit	Name	Function
1	7:4	Reserved	Always write 0.
1	3	GPO3OEN	**GPO3 Output Enable.** 0 = Output Disabled (Hi-Z) (default). 1 = Output Enabled.
1	2	GPO2OEN	**GPO2 Output Enable.** 0 = Output Disabled (Hi-Z) (default). 1 = Output Enabled.
1	1	GPO1OEN	**GPO1 Output Enable.** 0 = Output Disabled (Hi-Z) (default). 1 = Output Enabled.
1	0	Reserved	Always write 0.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	SAMEINT	ASQINT	STCINT

Command 0x81. GPIO_SET

Sets the output level (high or low) for GPO1, 2, and 3. GPO1, 2, and 3 can be configured for output by setting the GPO1OEN, GPO2OEN, and GPO3OEN bit in the GPIO_CTL command. To avoid excessive current consumption due to oscillation, GPO pins should not be left in a high impedance state. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is all GPO pins set for high impedance.

Available in: All

Command arguments: One

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	1	0	0	0	0	0	0	1
ARG1	0	0	0	0	GPO3LEVEL	GPO2LEVEL	GPO1LEVEL	0

ARG	Bit	Name	Function
1	7:4	Reserved	Always write 0.
1	3	GPO3LEVEL	**GPO3 Output Level.** 0 = Output low (default). 1 = Output high.
1	2	GPO2LEVEL	**GPO2 Output Level.** 0 = Output low (default). 1 = Output high.
1	1	GPO1LEVEL	**GPO1 Output Level.** 0 = Output low (default). 1 = Output high.
1	0	Reserved	Always write 0.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	RSQINT	SAMEINT	ASQINT	STCINT

5.4.2. WB Receiver Properties

Property 0x0001. GPO_IEN

Configures the sources for the GPO2/IRQ interrupt pin. Valid sources are the lower 8 bits of the STATUS byte, including CTS, ERR, RSQINT, SAMEINT (Si4707 only), ASQINT, and STCINT bits. The corresponding bit is set before the interrupt occurs. The CTS bit (and optional interrupt) is set when it is safe to send the next command. The CTS interrupt enable (CTSIEN) can be set with this property and the POWER_UP command. The state of the CTSIEN bit set during the POWER_UP command can be read by reading the this property and modified by writing this property. This command may only be sent when in powerup mode.

Errata:RSQIEN is non-functional on WB component 2.0.

Available in: All

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	RSQREP	SAMEREP	ASQREP	STCREP	CTSIEN	ERRIEN	0	0	RSQIEN	SAMEIEN	ASQIEN	STCIEN

Bit	Name	Function
15:12	Reserved	Always write to 0.
11	RSQREP	**RSQ Interrupt Repeat.** 0 = No interrupt generated when RSQINT is already set (default). 1 = Interrupt generated even if RSQINT is already set.
10	SAMEREP	**SAME Interrupt Repeat (Si4707 Only).** 0 = No interrupt generated when SAMEINT is already set (default). 1 = Interrupt generated even if SAMEINT is already set.
9	ASQREP	**ASQ Interrupt Repeat.** 0 = No interrupt generated when ASQINT is already set (default). 1 = Interrupt generated even if ASQINT is already set.
8	STCREP	**STC Interrupt Repeat.** 0 = No interrupt generated when STCINT is already set (default). 1 = Interrupt generated even if STCINT is already set.
7	CTSIEN	**CTS Interrupt Enable. After PowerUp, this bit will reflect the CTSIEN bit in ARG1 of PowerUp Command.** 0 = No interrupt generated when CTS is set. 1 = Interrupt generated when CTS is set.
6	ERRIEN	**ERR Interrupt Enable.** 0 = No interrupt generated when ERR is set (default). 1 = Interrupt generated when ERR is set.
5:4	Reserved	Always write to 0.
3	RSQIEN	**RSQ Interrupt Enable** 0 = No interrupt generated when RSQINT is set (default). 1 = Interrupt generated when RSQINT is set.

Bit	Name	Function
2	SAMEIEN	**SAME Interrupt Enable (Si4707 Only).** 0 = No interrupt generated when SAMEINT is set (default). 1 = Interrupt generated when SAMEINT is set.
1	ASQIEN	**ASQ Interrupt Enable** 0 = No interrupt generated when ASQINT is set (default) 1 = Interrupt generated when ASQINT is set
0	STCIEN	**Seek/Tune Complete Interrupt Enable.** 0 = No interrupt generated when TCINT is set (default) 1 = Interrupt generated when TCINT is set

Property 0x0102. DIGITAL_OUTPUT_FORMAT

Configures the digital audio output format. Configuration options include DCLK edge, data format, force mono, and sample precision.

Available in: Si4737/39/43

Default: 0x0000

Note: DIGITAL_OUTPUT_FORMAT is supported in WBRX component 3.0 or later.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	OFALL	OMODE[3:0]				OMONO	OSIZE[1:0]	

Bit	Name	Function
15:8	Reserved	Always write to 0.
7	OFALL	**Digital Output DCLK Edge.** 0 = use DCLK rising edge 1 = use DCLK falling edge
6:3	OMODE[3:0]	**Digital Output Mode.** 0000 = I^2S 0110 = Left-justified 1000 = MSB at second DCLK after DFS pulse 1100 = MSB at first DCLK after DFS pulse
2	OMONO	**Digital Output Mono Mode.** 0 = Use mono/stereo blend (per blend thresholds) 1 = Force mono
1:0	OSIZE[1:0]	**Digital Output Audio Sample Precision.** 0 = 16-bits 1 = 20-bits 2 = 24-bits 3 = 8-bits

Property 0x0104. DIGITAL_OUTPUT_SAMPLE_RATE

Enables digital audio output and configures digital audio output sample rate in samples per second (sps). When DOSR[15:0] is 0, digital audio output is disabled. The over-sampling rate must be set in order to satisfy a minimum DCLK of 1 MHz. To enable digital audio output, program DOSR[15:0] with the sample rate in samples per second. **The system controller must establish DCLK and DFS prior to enabling the digital audio output else the device will not respond and will require reset. The sample rate must be set to 0 before the DCLK/DFS is removed. WB_TUNE_FREQ command must be sent after the POWER_UP command to start the internal clocking before setting this property.**

Note: DIGITAL_OUPTUT_SAMPLE_RATE is supported in WBRX component 3.0 or later.

Available in: Si4737/39/43

Default: 0x0000 (digital audio output disabled)

Units: sps

Range: 32–48 ksps, 0 to disable digital audio output

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOSR[15:0]															

Bit	Name	Function
15:0	DOSR[15:0]	**Digital Output Sample Rate.** 32–48 ksps. 0 to disable digital audio output.

Property 0x0201. REFCLK_FREQ

Sets the frequency of the REFCLK from the output of the prescaler. The REFCLK range is 31130 to 34406 Hz (32768 5% Hz) in 1 Hz steps, or 0 (to disable AFC). For example, an RCLK of 13MHz would require a prescaler value of 400 to divide it to 32500 Hz REFCLK. The reference clock frequency property would then need to be set to 32500 Hz. RCLK frequencies between 31130 Hz and 40 MHz are supported, however, there are gaps in frequency coverage for prescaler values ranging from 1 to 10, or frequencies up to 311300 Hz. The following table summarizes these RCLK gaps.

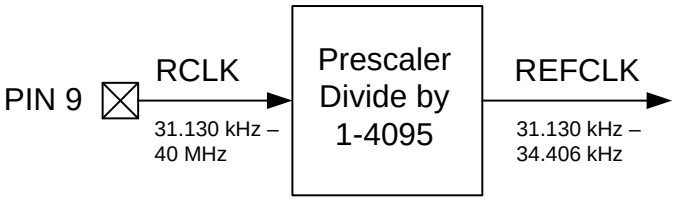


Figure 15. REFCLK Prescaler

Table 20. RCLK Gaps

Prescaler	RCLK Low (Hz)	RCLK High (Hz)
1	31130	34406
2	62260	68812
3	93390	103218
4	124520	137624
5	155650	172030
6	186780	206436
7	217910	240842
8	249040	275248
9	280170	309654
10	311300	344060

The RCLK must be valid 10 ns before and 10 ns after completing the WB_TUNE_FREQ command. In addition, the RCLK must be valid at all times when the carrier is enabled for proper AGC operation. The RCLK may be removed or reconfigured at other times. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode. The default is 32768 Hz.

Available in: All

Default: 0x8000 (32768)

Units: 1 Hz

Step: 1 Hz

Range: 31130-34406

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	REFCLKF[15:0]															

Bit	Name	Function
15:0	REFCLKF[15:0]	**Frequency of Reference Clock in Hz.** The allowed REFCLK frequency range is between 31130 and 34406 Hz (32768 5%), or 0 (to disable AFC).

Property 0x0202. REFCLK_PRESCALE

Sets the number used by the prescaler to divide the external RCLK down to the internal REFCLK. The range may be between 1 and 1023 in 1 unit steps. For example, an RCLK of 13MHz would require a prescaler value of 400 to divide it to 32500 Hz. The reference clock frequency property would then need to be set to 32500 Hz. The RCLK must be valid 10 ns before and 10 ns after completing the WB_TUNE_FREQ command. In addition, the RCLK must be valid at all times when the carrier is enabled for proper AFC operation. The RCLK may be removed or reconfigured at other times. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode. The default is 1.

Available in: All

Default: 0x0001

Step: 1

Range: 1-4095

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	RCLK SEL	REFCLKP[11:0]											

Bit	Name	Function
15:13	Reserved	Always write to 0.
12	RCLKSEL	**RCLKSEL.** 0 = RCLK pin is clock source. 1 = DCLK pin is clock source.
11:0	REFCLKP[11:0]	**Prescaler for Reference Clock.** Integer number used to divide clock frequency down to REFCLK frequency. The allowed REFCLK frequency range is between 31130 and 34406 Hz (32768 +/- 5%), or 0 (to disable AFC).

Property 0x5108. WB_MAX_TUNE_ERROR

Sets the maximum freq error allowed before setting the AFC_RAIL indicator.The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 10 kHz.

Available in: All

Default: 0x000A

Units: kHz

Step: 1

Range: 0–15

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	WBMAXTUNEERR[15:0]															

Bit	Name	Function
15:0	WBMAXTUNEERR	**WB Maximum Tuning Frequency Error.** Maximum tuning error allowed before setting the AFC Rail Indicator ON. Specified in units of kHz. Default is 10 kHz.

Property 0x5200. WB_RSQ_INT_SOURCE

Configures interrupt related to Received Signal Quality metrics. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 0.

Available in: All

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	X	X	X	X	X	X	X	X	X	X	X	X	SNRHIEN	SNRLIEN	RSSIHIEN	RSSILIEN

Bit	Name	Function
3	SNRHIEN	**Interrupt Source Enable: Audio SNR High.** Enable SNR high as the source of interrupt which the threshold is set by WB_RSQ_SNR_HI_THRESHOLD.
2	SNRLIEN	**Interrupt Source Enable: Audio SNR Low.** Enable SNR low as the as the source of interrupt which the threshold is set by WB_RSQ_SNR_LO_THRESHOLD.
1	RSSIHIEN	**Interrupt Source Enable: RSSI High.** Enable RSSI high as the source of interrupt which the threshold is set by WB_RSQ_RSSI_HI_THRESHOLD.
0	RSSILIEN	**Interrupt Source Enable: RSSI Low.** Enable RSSI low as the source of interrupt which the threshold is set by WB_RSQ_RSSI_LO_THRESHOLD.

Property 0x5201. WB_RSQ_SNR_HI_THRESHOLD

Sets high threshold which will trigger the RSQ interrupt if the Audio SNR is above this threshold. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 127dB.

Available in: All

Default: 0x007F

Units: dB

Step: 1

Range: 0-127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	SNRH[15:0]															

Bit	Name	Function
15:0	SNRH	**WB RSQ Audio SNR High Threshold.** Threshold which will trigger the RSQ interrupt if the Audio SNR is above this threshold. Specified in units of dB in 1 dB steps (0…127). Default is 127dB.

Property 0x5202. WB_RSQ_SNR_LO_THRESHOLD

Sets low threshold which will trigger the RSQ interrupt if the Audio SNR is below this threshold. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 0dB.

Available in: All

Default: 0x0000

Units: dB

Step: 1

Range: 0-127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	SNRL[15:0]															

Bit	Name	Function
15:0	SNRL	**WB RSQ Audio SNR Low Threshold.** Threshold which will trigger the RSQ interrupt if the Audio SNR is below this threshold. Specified in units of dB in 1 dB steps (0…127). Default is 0dB.

Property 0x5203. WB_RSQ_RSSI_HI_THRESHOLD

Sets high threshold which will trigger the RSQ interrupt if the RSSI is above this threshold. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 127dB.

Available in: All

Default: 0x007F

Units: dBµV

Step: 1

Range: 0-127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RSSIH[15:0]															

Bit	Name	Function
15:0	RSSIH	**WB RSQ RSSI High Threshold.** Threshold which will trigger the RSQ interrupt if the RSSI is above this threshold. Specified in units of dB in 1 dB steps (0…127). Default is 127dB.

Property 0x5204. WB_RSQ_RSSI_LO_THRESHOLD

Sets low threshold which will trigger the RSQ interrupt if the RSSI is below this threshold. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 0dB.

Available in: All

Default: 0x0000

Units: dBµV

Step: 1

Range: 0-127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RSSIL[15:0]															

Bit	Name	Function
15:0	RSSIL	**WB RSQ RSSI Low Threshold.** Threshold which will trigger the RSQ interrupt if the RSSI is below this threshold. Specified in units of dB in 1 dB steps (0…127). Default is 0dB.

Property 0x5403. WB_VALID_SNR_THRESHOLD

Sets the SNR threshold which the WB_RSQ_STATUS and WB_TUNE_STATUS will consider the channel valid if the received SNR is at or above this value. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 3dB.

Available in: All

Default: 0x0003

Units: dBµV

Step: 1

Range: 0-127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	WB_VALID_SNR_THRESHOLD[15:0]															

Bit	Name	Function
15:0	WB_VALID_SNR_THRESHOLD	**WB Valid SNR Threshold.** SNR value at or above which WB_RSQ_STATUS and WB_TUNE_STATUS will consider the channel VALID. Specified in units of dB in 1 dB steps (0…127). Default is 3 dB.

Property 0x5404. WB_VALID_RSSI_THRESHOLD

Sets the RSSI threshold which the WB_RSQ_STATUS and WB_TUNE_STATUS will consider the channel valid if the received RSSI is at or above this value. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 20dB.

Available in: All

Default: 0x0014

Units: dBµV

Step: 1

Range: 0-127

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	WB_VALID_RSSI_THRESHOLD [15:0]															

Bit	Name	Function
15:0	WB_VALID_RSSI_THRESHOLD	**WB Valid RSSI Threshold.** RSSI value at or above which WB_RSQ_STATUS and WB_TUNE_STATUS will consider the channel VALID. Specified in units of dB in 1 dB steps (0…127). Default is 20 dB.

Property 0x5500. WB_SAME_INTERRUPT_SOURCE

Configures the SAME interrupt sources. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 0.

Available in: Si4707

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	EOMDET	SOMDET	PREDET	HDRRDY

Bit	Name	Function
15:4	Reserved	Always write to 0.
3	EOMDET	Enable EOMDET as the source of SAME Interrupt.
2	SOMDET	Enable SOMDET as the source of SAME Interrupt.
1	PREDET	Enable PREDET as the source of SAME Interrupt.
0	HDRRDY	Enable HDRRDY as the source of SAME Interrupt.

Property 0x5600. WB_ASQ_INT_SOURCE

Configures interrupt related to the 1050kHz alert tone. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 0.

Available in: All

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	X	X	X	X	X	X	X	X	X	X	X	X	X	X	ALERTOFF_IEN	ALERTON_IEN

Bit	Name	Function
1	ALERTOFF_IEN	**Interrupt Source Enable: Alert OFF.** Enable 1050kHz alert tone disappeared as the source of interrupt.
0	ALERTON_IEN	**Interrupt Source Enable: Alert ON.** Enable 1050kHz alert tone appeared as the source of interrupt.

Property 0x4000. RX_VOLUME

Sets the audio output volume. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 63.

Available in: All

Default: 0x003F

Step: 1

Range: 0-63

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	VOL[15:0]															

Bit	Name	Function
15:0	VOL	**Output Volume.** Sets the output volume level, 63 max, 0 min. Default is 63.

Property 0x4001. RX_HARD_MUTE

Mutes the audio output. L and R audio outputs may not be muted independently. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is unmute (0x0000).

Available in: All

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LMUTE	RMUTE

Bit	Name	Function
15:2	Reserved	Always write to 0.
1	LMUTE	Mutes both L and R Audio Outputs.
0	RMUTE	Mutes both L and R Audio Outputs.

5.5. Commands and Properties for the Stereo Audio ADC Mode (Si4704/05/30/31)

The following two tables are the summary of the commands and properties for the Stereo Audio ADC component applicable to Si4704/05/30/31-D62.

Table 21. Stereo Audio ADC Mode Command Summary

Cmd	Name	Description	Devices
0x01	POWER_UP	Power-up device and mode selection. Modes include operational function and audio interface configuration	All
0x10	GET_REV	Returns the revision information on the device.	All
0x11	POWER_DOWN	Power-down device.	All
0x12	SET_PROPERTY	Sets the value of a property.	All
0x13	GET_PROPERTY	Retrieves a property's value.	All
0x14	GET_INT_STATUS	Read interrupt status bits.	All
0x15	PATCH_ARGS*	Reserved command used for patch file down-loads.	All
0x16	PATCH_DATA*	Reserved command used for patch file down-loads.	All
0x61	AUX_ASRC_START	Starts sampling rate conversion.	All
0x65	AUX_ASQ_STATUS	Reports audio signal quality metrics.	All
0x80	GPIO_CNTL	Configures GPO1, 2, and 3 as output or Hi-Z	All
0x81	GPIO_SET	Sets GPO1, 2, and 3 output level (low or high).	All
***Note:** Commands PATCH_ARGS and PATCH_DATA are only used to patch firmware. For information on applying a patch file, see "7.2. Powerup from a Component Patch" on page 233.			

Table 22. Stereo Audio ADC Mode Property Summary

Prop	Name	Description	Default	Available In
0x0001	GPO_IEN	Enables interrupt sources.	0x0000	All
0x0102	DIGITAL_OUTPUT_FORMAT	Configure digital audio outputs.	0x0000	All
0x0104	DIGITAL_OUTPUT_SAMPLE_RATE	Configure digital audio output sample rate.	0x0000	All
0x0201	REFCLK_FREQ	Sets the frequency of the reference clock in Hz. The range is 31130 to 34406 Hz.	0x8000	All
0x0202	REFCLK_PRESCALE	Sets prescaler value for the reference clock.	0x0001	All
0x6600	AUX_ASQ_INTERRUPT_SOURCE	Configure ASQ Interrupt source.	0x0000	All

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CTS	ERR	X	X	X	X	ASQINT	X

Bit	Name	Function
7	CTS	**Clear to Send.** 0 = Wait before sending next command. 1 = Clear to send next command.
6	ERR	**Error.** 0 = No error 1 = Error
5:2	Reserved	Values may vary.
1	ASQINT	**Audio Signal Quality Interrupt.** 0 = Audio signal quality interrupt has not been triggered. 1 = Audio signal quality interrupt has been triggered.
0	Reserved	Values may vary.

5.5.1. Stereo Audio ADC Mode Commands

Command 0x01. POWER_UP

Initiates the boot process to move the device from powerdown to powerup mode. The boot can occur from internal device memory or a system controller downloaded patch. To confirm that the patch is compatible with the internal device library revision, the library revision should be confirmed by issuing the POWER_UP command with FUNC = 15 (query library ID). The device returns the response, including the library revision, and then moves into powerdown mode. The device can then be placed in powerup mode by issuing the POWER_UP command with FUNC = 4 (AUX Input) and the patch may be applied (See Section "7.2. Powerup from a Component Patch" on page 233).

The POWER_UP command configures the state of LIN (pin 15) and RIN (pin 16) for analog audio inputs and GPO2/INT (pin 18) for interrupt operation. POWER_UP command also configures the state of GPO3/DCLK (pin 17), DFS (pin 14), and DOUT (pin 13) for digital audio mode. The command configures GPO2/INT interrupts (GPO2OEN) and CTS interrupts (CTSIEN). If both are enabled, GPO2/INT is driven high during normal operation and low for a minimum of 1 µs during the interrupt. The CTSIEN bit is duplicated in the GPO_IEN property. The command is complete when the CTS bit (and optional interrupt) is set.

Note: To change function (e.g. FM RX to AUX IN or AUX IN to AM RX), issue POWER_DOWN command to stop current function; then, issue POWER_UP to start new function.

Note: Delay at least 500 ms between powerup command and first tune command to wait for the oscillator to stabilize if XOSCEN is set and crystal is used as the RCLK.

Available in: All

Command Arguments: Two

Response Bytes: None (FUNC = 0), Seven (FUNC = 15)

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	0	0	0	0	1
ARG1	CTSIEN	GPO2OEN	PATCH	XOSCEN	FUNC[3:0]			
ARG2	OPMODE[7:0]							

ARG	Bit	Name	Function
1	7	CTSIEN	**CTS Interrupt Enable.** 0 = CTS interrupt disabled. 1 = CTS interrupt enabled.
1	6	GPO2OEN	**GPO2 Output Enable.** 0 = GPO2 output disabled. 1 = GPO2 output enabled.
1	5	PATCH	**Patch Enable.** 0 = Boot normally. 1 = Copy NVM to RAM, but do not boot. After CTS has been set, RAM may be patched.

ARG	Bit	Name	Function
1	4	XOSCEN	**Crystal Oscillator Enable.** **Note:** Set to 0 for Si4740/41/42/43/44/45/49 0 = Use external RCLK (crystal oscillator disabled). 1 = Use crystal oscillator (RCLK and GPO3/DCLK with external 32.768 kHz crystal and OPMODE=00000101). See Si47xx Data Sheet Application Schematic for external BOM details.
1	3:0	FUNC[3:0]	**Function.** 0–3 = Reserved. 4 = AUX IN. 5–14 = Reserved.
2	7:0	OPMODE[7:0]	**Application Setting.** 01011011 = Digital audio outputs (DCLK, DFS, DIO)

Response (FUNC = 4, AUX IN)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	X	ASQINT	X

Response (FUNC = 15, Query Library ID)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	X	ASQINT	X
RESP1	PN[7:0]							
RESP2	FWMAJOR[7:0]							
RESP3	FWMINOR[7:0]							
RESP4	RESERVED[7:0]							
RESP5	RESERVED[7:0]							
RESP6	CHIPREV[7:0]							
RESP7	LIBRARYID[7:0]							

RESP	Bit	Name	Function
1	7:0	PN[7:0]	**Final 2 digits of part number (HEX).**
2	7:0	FWMAJOR[7:0]	**Firmware Major Revision (ASCII).**
3	7:0	FWMINOR[7:0]	**Firmware Minor Revision (ASCII).**
4	7:0	RESERVED[7:0]	**Reserved, various values.**
5	7:0	RESERVED[7:0]	**Reserved, various values.**
6	7:0	CHIPREV[7:0]	**Chip Revision (ASCII).**
7	7:0	LIBRARYID[7:0]	**Library Revision (HEX).**

Command 0x10. GET_REV

Returns the part number, chip revision, firmware revision, patch revision and component revision numbers. The command is complete when the CTS bit (and optional interrupt) is set. This command may only be sent when in powerup mode.

Available in: All

Command arguments: None

Response bytes: Fifteen (Si4705 only), Eight (Si4704/3x)

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	0	0

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	X	ASQINT	X
RESP1	PN[7:0]							
RESP2	FWMAJOR[7:0]							
RESP3	FWMINOR[7:0]							
RESP4	$PATCH_H$[7:0]							
RESP5	$PATCH_L$[7:0]							
RESP6	CMPMAJOR[7:0]							
RESP7	CMPMINOR[7:0]							
RESP8	CHIPREV[7:0]							
RESP10	Reserved							
RESP11	Reserved							
RESP12	Reserved							
RESP13	Reserved							
RESP14	Reserved							
RESP15	CID[7:0] (Si4705 only)							

RESP	Bit	Name	Function
1	7:0	PN[7:0]	**Final 2 digits of Part Number (HEX).**
2	7:0	FWMAJOR[7:0]	**Firmware Major Revision (ASCII).**
3	7:0	FWMINOR[7:0]	**Firmware Minor Revision (ASCII).**
4	7:0	$PATCH_H$[7:0]	**Patch ID High Byte (HEX).**
5	7:0	$PATCH_L$[7:0]	**Patch ID Low Byte (HEX).**

6	7:0	CMPMAJOR[7:0]	**Component Major Revision (ASCII).**
7	7:0	CMPMINOR[7:0]	**Component Minor Revision (ASCII).**
8	7:0	CHIPREV[7:0]	**Chip Revision (ASCII).**
15	7:0	CID[7:0]	**CID (Si4705 only).**

Command 0x11. POWER_DOWN

Moves the device from powerup to powerdown mode. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode. Note that only the POWER_UP command is accepted in powerdown mode. **If the system controller writes a command other than POWER_UP when in powerdown mode, the device does not respond. The device will only respond when a POWER_UP command is written. GPO pins are powered down and not active during this state. For optimal power down current, GPO2 must be either internally driven low through GPIO_CTL command or externally driven low.**

Note: The following describes the state of all the pins when in powerdown mode:

GPIO1, GPIO2, and GPIO3 = 0

DOUT, DFS, RIN, LIN = HiZ

Available in: All

Command arguments: None

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	0	1

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	X	X	X

Command 0x12. SET_PROPERTY

Sets a property shown in Table 22, “Stereo Audio ADC Mode Property Summary,” on page 204. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode. See Figure 30, “CTS and SET_PROPERTY Command Complete tCOMP Timing Model,” on page 243 and Table 53, “Command Timing Parameters for the Stereo Audio ADC Mode,” on page 247.

Available in: All

Command Arguments: Five

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	1	0
ARG1	0	0	0	0	0	0	0	0
ARG2	$PROP_H$[7:0]							
ARG3	$PROP_L$[7:0]							
ARG4	$PROPD_H$[7:0]							
ARG5	$PROPD_L$[7:0]							

ARG	Bit	Name	Function
1	7:0	Reserved	Always write to 0.
2	7:0	$PROP_H$[7:0]	**Property High Byte.** This byte in combination with $PROP_L$ is used to specify the property to modify.
3	7:0	$PROP_L$[7:0]	**Property Low Byte.** This byte in combination with $PROP_H$ is used to specify the property to modify.
4	7:0	$PROPD_H$[7:0]	**Property Value High Byte.** This byte in combination with $PROPD_L$ is used to set the property value.
5	7:0	$PROPD_L$[7:0]	**Property Value Low Byte.** This byte in combination with $PROPD_H$ is used to set the property value.

Command 0x13. GET_PROPERTY

Gets a property as shown in Table 22, “Stereo Audio ADC Mode Property Summary,” on page 204. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode.

Available in: All

Command arguments: Three

Response bytes: Three

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	0	1	1
ARG1	0	0	0	0	0	0	0	0
ARG2	$PROP_H[7:0]$							
ARG3	$PROP_L[7:0]$							

ARG	Bit	Name	Function
1	7:0	Reserved	Always write to 0.
2	7:0	$PROP_H[7:0]$	**Property High Byte.** This byte in combination with $PROP_L$ is used to specify the property to get.
3	7:0	$PROP_L[7:0]$	**Property Low Byte.** This byte in combination with $PROP_H$ is used to specify the property to get.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	X	ASQINT	X
RESP1	0	0	0	0	0	0	0	0
RESP2	$PROPD_H[7:0]$							
RESP3	$PROPD_L[7:0]$							

RESP	Bit	Name	Function
1	7:0	Reserved	Always returns 0.
2	7:0	$PROPD_H[7:0]$	**Property Value High Byte.** This byte in combination with $PROPD_L$ represents the requested property value.
3	7:0	$PROPD_L[7:0]$	**Property Value High Byte.** This byte in combination with $PROPD_H$ represents the requested property value.

Command 0x14. GET_INT_STATUS

Updates bits 6:0 of the status byte. This command should be called after any command that sets the ASQINT bit. When polling this command should be periodically called to monitor the STATUS byte, and when using interrupts, this command should be called after the interrupt is set to update the STATUS byte. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be set when in powerup mode.

Available in: All

Command arguments: None

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	1	0	1	0	0

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	X	ASQINT	X

Command 0x61. AUX_ASRC_START

Starts sample rate conversion in signal processing module. The CTS bit (and optional interrupt) is set when it is safe to send the next command. The ERR bit (and optional interrupt) is set if an invalid argument is sent. Note that only a single interrupt occurs if both the CTS and ERR bits are set. This command may only be sent when in powerup mode.

Available in: All

Command arguments: One

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	1	1	0	0	0	0	1

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	X	ASQINT	X

Command 0x65. AUX_ASQ_STATUS

Returns status information about audio signal quality. The command returns the input signalLEVEL. This command can be used to detect if a signal overload condition is present indicated by OVERLOADINT. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode.

Available in: All

Command arguments: One

Response bytes: Three

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	1	1	0	0	1	0	1
ARG1	0	0	0	0	0	0	0	INTACK

ARG	Bit	Name	Function
1	0	INTACK	**Interrupt Acknowledge.** 0 = Interrupt status preserved. 1 = Clears ASQINT

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	X	ASQINT	X
RESP1	X	X	X	X	X	X	X	OVERLOADINT
RESP2	X	X	X	X	X	X	X	OVERLOAD
RESP3	LEVEL[7:0]							

RESP	Bit	Name	Function
1	0	OVERLOADINT	**Audio Signal Overload Interrupt.** 0 = Audio Input Signal overload has not been detected. 1 = Audio Input Signal overload has been detected.
2	0	OVERLOAD	**Audio Signal Overload.** 0 = Audio Input Signal overload is not present. 1 = Audio Input Signal overload is present.
3	7:0	LEVEL[7:0]	**Audio Input Signal Level.** Line input audio level indicator in FS. Range: –128 to 127

Command 0x80. GPIO_CTL

Enables output for GPO1, 2, and 3. GPO1, 2, and 3 can be configured for output (Hi-Z or active drive) by setting the GPO1OEN, GPO2OEN, and GPO3OEN bit. The state (high or low) of GPO1, 2, and 3 is set with the GPIO_SET command. To avoid excessive current consumption due to oscillation, GPO pins should not be left in a high impedance state. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This command may only be sent when in powerup mode. The default is all GPO pins set for high impedance.

Note: The use of GPO2 as an interrupt pin and/or the use of GPO3 as DCLK digital clock input will override this GPIO_CTL function for GPO2 and/or GPO3 respectively.

Available in: All

Command arguments: One

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	1	0	0	0	0	0	0	0
ARG1	0	0	0	0	GPO3OEN	GPO2OEN	GPO1OEN	0

ARG	Bit	Name	Function
1	7:4	Reserved	Always write 0.
1	3	GPO3OEN	**GPO3 Output Enable.** 0 = Output Disabled (Hi-Z) (default). 1 = Output Enabled.
1	2	GPO2OEN	**GPO2 Output Enable.** 0 = Output Disabled (Hi-Z) (default). 1 = Output Enabled.
1	1	GPO1OEN	**GPO1 Output Enable.** 0 = Output Disabled (Hi-Z) (default). 1 = Output Enabled.
1	0	Reserved	Always write 0.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	X	ASQINT	X

Command 0x81. GPIO_SET

Sets the output level (high or low) for GPO1, 2, and 3. GPO1, 2, and 3 can be configured for output by setting the GPO1OEN, GPO2OEN, and GPO3OEN bit in the GPIO_CTL command. To avoid excessive current consumption due to oscillation, GPO pins should not be left in a high impedance state. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is all GPO pins set for high impedance.

Available in: All

Command arguments: One

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	1	0	0	0	0	0	0	1
ARG1	0	0	0	0	GPO3LEVEL	GPO2LEVEL	GPO1LEVEL	0

ARG	Bit	Name	Function
1	7:4	Reserved	Always write 0.
1	3	GPO3LEVEL	**GPO3 Output Level.** 0 = Output low (default). 1 = Output high.
1	2	GPO2LEVEL	**GPO2 Output Level.** 0 = Output low (default). 1 = Output high.
1	1	GPO1LEVEL	**GPO1 Output Level.** 0 = Output low (default). 1 = Output high.
1	0	Reserved	Always write 0.

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	CTS	ERR	X	X	X	X	ASQINT	X

5.5.2. Stereo Audio ADC Mode Properties

Property 0x0001. GPO_IEN

Configures the sources for the GPO2/$\overline{\text{INT}}$ interrupt pin. Valid sources are the lower 8 bits of the STATUS byte, including CTS, ERR, and ASQINT bits. The corresponding bit is set before the interrupt occurs. The CTS bit (and optional interrupt) is set when it is safe to send the next command. The CTS interrupt enable (CTSIEN) can be set with this property and the POWER_UP command. The state of the CTSIEN bit set during the POWER_UP command can be read by reading this property and modified by writing this property. This property may only be set or read when in powerup mode.

Available in: All

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	ASQIEN	0	CTSIEN	ERRIEN	0	0	0	0	ASQIEN	0

Bit	Name	Function
15:10	Reserved	Always write to 0.
9	ASQREP	**ASQ Interrupt Repeat.** 0 = No interrupt generated when ASQINT is already set (default). 1 = Interrupt generated even if ASQINT is already set.
8	Reserved	Always write to 0.
7	CTSIEN	**CTS Interrupt Enable. After PowerUp, this bit reflects the CTSIEN bit in ARG1 of PowerUp Command.** 0 = No interrupt generated when CTS is set. 1 = Interrupt generated when CTS is set.
6	ERRIEN	**ERR Interrupt Enable.** 0 = No interrupt generated when ERR is set (default). 1 = Interrupt generated when ERR is set.
5:2	Reserved	Always write to 0.
1	ASQIEN	**ASQ Interrupt Enable.** 0 = No interrupt generated when ASQINT is set (default). 1 = Interrupt generated when ASQINT is set.
0	Reserved	Always write to 0.

Property 0x0102. DIGITAL_OUTPUT_FORMAT

Configures the digital audio output format. Configuration options include DCLK edge, data format, force mono, and sample precision.

Available in: All

Default: 0x0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	OFALL	OMODE[3:0]				OMONO	OSIZE[1:0]	

Bit	Name	Function
15:8	Reserved	Always write to 0.
7	OFALL	**Digital Output DCLK Edge.** 0 = use DCLK rising edge 1 = use DCLK falling edge
6:3	OMODE[3:0]	**Digital Output Mode.** 0000 = I^2S 0110 = Left-justified 1000 = MSB at second DCLK after DFS pulse 1100 = MSB at first DCLK after DFS pulse
2	OMONO	**Digital Output Mono Mode.** 0 = Use mono/stereo blend (per blend thresholds) 1 = Force mono
1:0	OSIZE[1:0]	**Digital Output Audio Sample Precision.** 0 = 16-bits 1 = 20-bits 2 = 24-bits 3 = 8-bits

Property 0x0104. DIGITAL_OUTPUT_SAMPLE_RATE

Enables digital audio output and configures digital audio output sample rate in samples per second (sps). When DOSR[15:0] is 0, digital audio output is disabled. The over-sampling rate must be set in order to satisfy a minimum DCLK of 1 MHz. To enable digital audio output, program DOSR[15:0] with the sample rate in samples per second. **The system controller must establish DCLK and DFS prior to enabling the digital audio output else the device will not respond and will require reset. The sample rate must be set to 0 before the DCLK/DFS is removed.**

Available in: All

Default: 0x0000 (digital audio output disabled)

Units: sps

Range: 32–48 ksps, 0 to disable digital audio output

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DOSR[15:0]															

Bit	Name	Function
15:0	DOSR[15:0]	**Digital Output Sample Rate.** 32, 44.1, and 48 ksps. 0 to disable digital audio output.

Property 0x0201. REFCLK_FREQ

Sets the frequency of the REFCLK from the output of the prescaler. The REFCLK range is 31130 to 34406 Hz (32768 ±5% Hz) in 1 Hz steps, or 0 (to disable AFC). For example, an RCLK of 13 MHz would require a prescaler value of 400 to divide it to 32500 Hz REFCLK. The reference clock frequency property would then need to be set to 32500 Hz. RCLK frequencies between 31130 Hz and 40 MHz are supported, however, there are gaps in frequency coverage for prescaler values ranging from 1 to 10, or frequencies up to 311300 Hz. The following table summarizes these RCLK gaps.

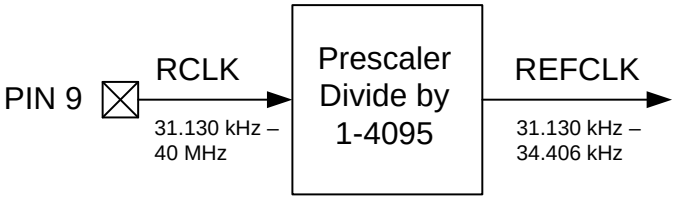


Figure 16. REFCLK Prescaler

Table 23. RCLK Gaps

Prescaler	RCLK Low (Hz)	RCLK High (Hz)
1	31130	34406
2	62260	68812
3	93390	103218
4	124520	137624
5	155650	172030
6	186780	206436
7	217910	240842
8	249040	275248
9	280170	309654
10	311300	344060

The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 32768 Hz.

The RCLK must be valid 10 ns before sending and 20 ns after completing the AUX_ASRC_START command. In addition, the RCLK must be valid at all times for proper AFC operation. The RCLK may be removed or reconfigured at other times.

Available in: All

Default: 0x8000 (32768)

Units: 1 Hz

Step: 1 Hz

Range: 31130–34406

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	REFCLKF[15:0]															

Bit	Name	Function
15:0	REFCLKF[15:0]	**Frequency of Reference Clock in Hz.** The allowed REFCLK frequency range is between 31130 and 34406 Hz (32768 ±5%), or 0 (to disable AFC).

Property 0x0202. REFCLK_PRESCALE

Sets the number used by the prescaler to divide the external RCLK down to the internal REFCLK. The range may be between 1 and 4095 in 1 unit steps. For example, an RCLK of 13 MHz would require a prescaler value of 400 to divide it to 32500 Hz. The reference clock frequency property would then need to be set to 32500 Hz. The RCLK must be valid 10 ns before sending and 20 ns after completing the AUX_ASRC_START command. In addition, the RCLK must be valid at all times for proper AFC operation. The RCLK may be removed or reconfigured at other times.The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in powerup mode. The default is 1.

Available in: All

Default: 0x0001

Step: 1

Range: 1–4095

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	RCLK-SEL	REFCLKP[11:0]											

Bit	Name	Function
15:13	Reserved	Always write to 0.
12	RCLKSEL	0 = RCLK pin is clock source. 1 = DCLK pin is clock source.
11:0	REFCLKP[11:0]	**Prescaler for Reference Clock.** Integer number used to divide clock frequency down to REFCLK frequency. The allowed REFCLK frequency range is between 31130 and 34406 Hz (32768 5%), or 0 (to disable AFC).

Property 0x6600. AUX_ASQ_INTERRUPT_SOURCE

Configures interrupt related to Audio Signal Quality metrics. The CTS bit (and optional interrupt) is set when it is safe to send the next command. This property may only be set or read when in power up mode. The default is 0.

Available in: All

Default: 0x0000

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0X0000															OVER LOADINT

Bit	Name	Function
15:2	Reserved	Always write to 0.
1:0	OVERLOADINT	**Interrupt Source Enable: Overload** 0 = Disable audio signal overload detection interrupt 1 = Enable audio signal overload detection interrupt

6. Control Interface

The bus mode is selected by sampling the state of the GPO1 and GPO2/INT pins on the rising edge of $\overline{RST}$. The GPO1 pin includes a 1 MΩ internal pull-up resistor that is connected while $\overline{RST}$ is low, and the GPO2/INT pin includes an internal 1 MΩ pull-down resistor that is connected while the $\overline{RST}$ pin in low. Therefore, it is only necessary for the system controller to actively drive pins if a mode other than the default 2-wire mode is required, as shown in Table 24. After bus mode selection is complete, the device is placed in powerdown mode. The minimum setup time for GPO1 and GPO2 before $\overline{RST}$ = 1 is 30 ns when actively driven by the system controller and 100 µs if the internal 1 MΩ resistor is allowed to set the default GPO1 (high) and GPO2 (low). Refer to the Si471x data sheet for specific reset timing requirements.

Table 24. Bus Mode Selection

Bus Mode	GPO2/INT	GPO1
3-wire	0	0 (must drive)
SPI	1 (must drive)	1
2-wire	0	1

In powerdown mode, all circuitry is disabled except for the device control interface. The device comes out of powerdown mode when the POWER_UP command is written to the command register. Once in powerup mode, the device accepts additional commands, such as tuning, and the setting of properties, such as power level. The device will not accept commands while in powerdown mode, with the exception of the powerup command. **If the system controller writes a command other than POWER_UP when in powerdown mode, the device does not respond, and a reset is required.**

Setting the $\overline{RST}$ pin low places the device in reset mode. In reset mode, all circuitry is disabled including the device control interface; registers are set to their default settings, and the control bus is disabled.

6.1. 2-Wire Control Interface Mode

Figures 17 and 18 show the 2-wire Control Interface Read and Write Timing Parameters and Diagrams, respectively. Refer to the Si471x data sheet for timing parameter values.

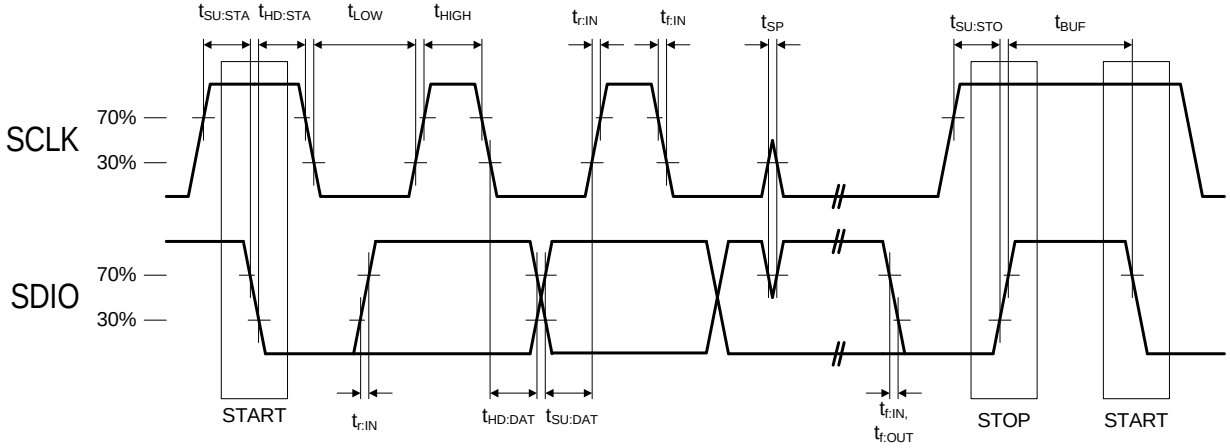


Figure 17. 2-wire Control Interface Read and Write Timing Parameters

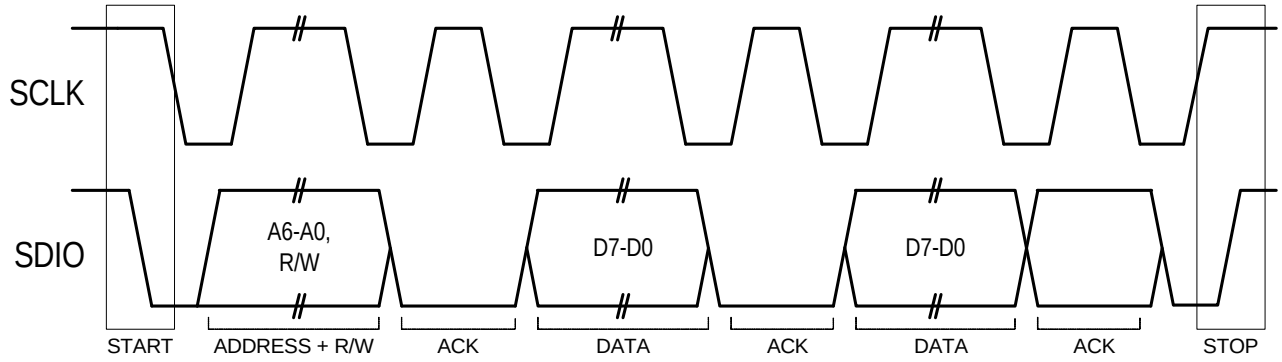


Figure 18. 2-wire Control Interface Read and Write Timing Diagram

2-wire bus mode uses only the SCLK and SDIO pins for signaling. A transaction begins with the START condition, which occurs when SDIO falls while SCLK is high. Next, the system controller drives an 8-bit control word serially on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a seven-bit device address followed by a read/write bit (read = 1, write = 0). The device acknowledges the control word by driving SDIO low on the next falling edge of SCLK.

Although the device responds to only a single device address, this address can be changed with the $\overline{SEN}$ pin (note that the $\overline{SEN}$ pin is not used for signaling in 2-wire mode). When $\overline{SEN}$ = 0, the seven-bit device address is 0010001b. When $\overline{SEN}$ = 1, the address is 1100011b.

For write operations, the system controller next sends a data byte on SDIO, which is captured by the device on rising edges of SCLK. The device acknowledges each data byte by driving SDIO low for one cycle on the next falling edge of SCLK. The system controller may write up to 8 data bytes in a single 2-wire transaction. The first byte is a command, and the next seven bytes are arguments. **Writing more than 8 bytes results in unpredictable device behavior.**

For read operations, after the device has acknowledged the control byte, it will drive an eight-bit data byte on SDIO, changing the state of SDIO on the falling edges of SCLK. The system controller acknowledges each data byte by driving SDIO low for one cycle on the next falling edge of SCLK. If a data byte is not acknowledged by the system controller, the transaction will end. The system controller may read up to 16 data bytes in a single 2-wire transaction. These bytes contain the status byte and response data from the device.

A 2-wire transaction ends with the STOP condition, which occurs when SDIO rises while SCLK is high.

Table 25 demonstrates the command and response procedure implemented in the system controller to use the 2-wire bus mode. In this example the TX_TUNE_FREQ command is demonstrated.

Table 25. Command and Response Procedure - 2-Wire Bus Mode

Action	Data	Description
CMD	0x30	TX_TUNE_FREQ
ARG1	0x00	
ARG2	0x27	Set Station to 101.1 MHz
ARG3	0x7E	(0x277E = 10110 with 10 kHz step size)
STATUS	→0x80	Reply Status. Clear-to-send high.

To send the TX_TUNE_FREQ command and arguments, the system controller sends the START condition, followed by the 8-bit control word, which consists of a seven-bit device address (0010001b SEN = 0 or 1100011b SEN = 1) and the write bit (0b) indicated by ADDR+W = 00100010b = 0x22. In this example, SEN = 0 resulting in the control word ADDR+W = 00100010b = 0x22. If instead SEN = 1, the resulting control word would be ADDR+W = 11000110b = 0xC6. The device acknowledges the control word by setting SDIO = 0, indicated by ACK = 0. The system controller then sends the CMD byte, 0x30, and again the device acknowledges by setting ACK = 0. The system controller and device repeat this process for the ARG1, ARG2, and ARG3 bytes. Commands may take up to seven argument bytes, and this flexibility should be designed into the 2-wire bus mode implementation. Alternatively, all seven argument bytes may be sent for all commands, but unusual arguments must be 0x00. **Unpredictable device behavior will result if more than seven arguments are sent.**

START	ADDR+W	ACK	CMD	ACK	ARG1	ACK	ARG2	ACK	ARG3	ACK	STOP
START	0x22	0	0x30	0	0x00	0	0x27	0	0x7E	0	STOP

To read the status and response from the device, the system controller sends the START condition, followed by the eight-bit control word, which consists of the seven bit device address and the read bit (1b). In this example, SEN = 0 and the write control word is ADDR+R = 00100011b = 0x23. If SEN = 1, the write control word would be ADDR+R = 11000111b = 0xC7. The device acknowledges the control word by setting ACK = 0. Next the system controller reads the STATUS byte. In this example, the STATUS byte is 0x00, indicating that the CTS bit, bit 8, has not been set. The response bytes are not ready for reading and that the device is not ready to accept another command. The system controller sets SDIO = 1, indicated by NACK = 1, to signal to the device the 2-wire transfer will end. The system controller should set the STOP condition. This process is repeated until the STATUS byte indicates that CTS bit is set, 0x80 in this example.

START	ADDR+R	ACK	STATUS	NACK	STOP
START	0x23	0	0x00	1	STOP

When the STATUS byte returns CTS bit set, 0x80 in this example, the system controller may read the response bytes from the device. The controller sets ACK = 0 to indicate to the device that additional bytes will be read. The RESP1 byte is read by the system controller, followed by the system controller setting ACK = 0. This is repeated for RESP2. RESP3 is read by the system controller followed by the system controller setting NACK = 1, indicating that RESP3 is the last byte to be read. The system controller then sets the STOP condition. Responses may be up to 15 bytes in length (RESP1–RESP15) depending on the command. It is acceptable to read all 15 response bytes. However, unused response bytes return random data and must be ignored. Note that the TX_TUNE_FREQ command returns only the STATUS byte and response bytes are shown only for completeness.

START	ADDR+R	ACK	STATUS	ACK	RESP1	ACK	RESP2	ACK	RESP3	NACK	STOP
START	0x23	0	0x80	0	0x00	0	0x00	0	0x00	1	STOP

6.2. 3-Wire Control Interface Mode

Figures 19 and 20 show the 3-wire Control Interface Read and Write Timing Parameters and Diagrams, respectively. Refer to the Si471x data sheet for timing parameter values.

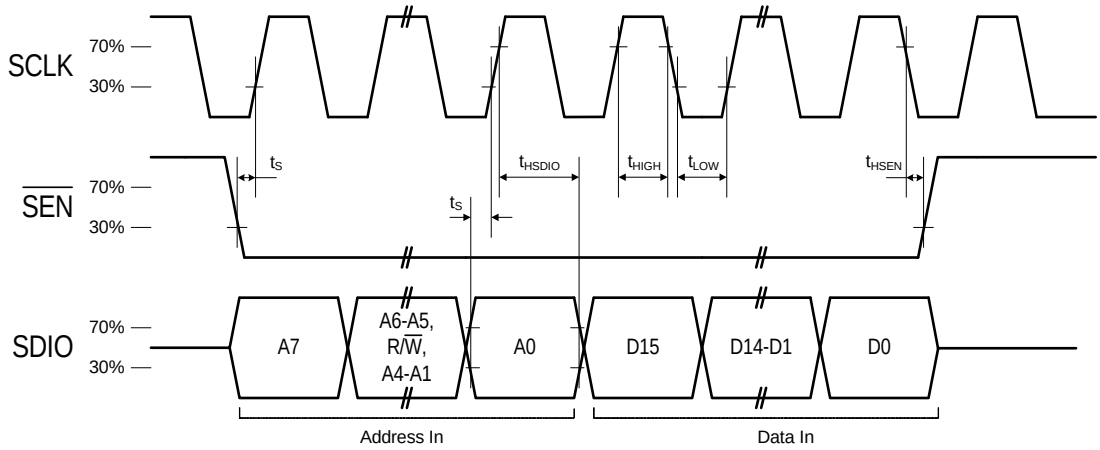


Figure 19. 3-Wire Control Interface Write Timing Parameters

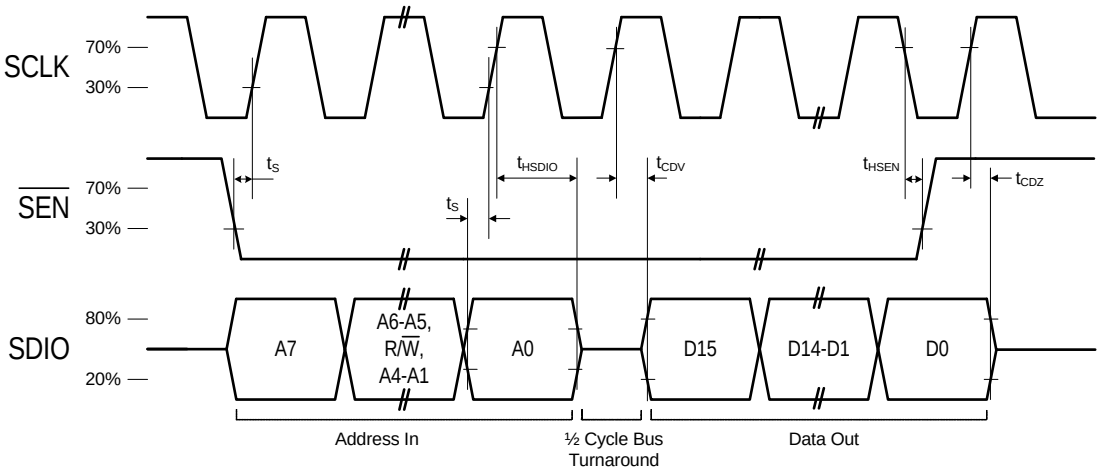


Figure 20. 3-Wire Control Interface Read Timing Parameters

3-wire bus mode uses the SCLK, SDIO and $\overline{\text{SEN}}$ pins. A transaction begins when the system controller drives $\overline{\text{SEN}}$ low. Next, the system controller drives a 9-bit control word on SDIO, which is captured by the device on rising edges of SCLK. The control word is comprised of a three bit chip address (A7:A5 = 101b), a read/write bit (write = 0, read = 1), the chip address (A4 = 0), and a four bit register address (A3:A0).

For write operations, the control word is followed by a 16-bit data word, which is captured by the device on rising edges of SCLK. For read operations, the control word is followed by a delay of one-half SCLK cycle for bus turn-around. Next, the device drives the 16-bit read data word serially on SDIO, changing the state of SDIO on each rising edge of SCLK.

For read operations, the control word is followed by a delay of one-half SCLK cycle for bus turn-around. Next, the device drives the 16-bit read data word serially on SDIO, changing the state of SDIO on each rising edge of SCLK.

A transaction ends when the system controller sets $\overline{\text{SEN}}$ = 1, then pulses SCLK high and low one final time. SCLK may either stop or continue to toggle while $\overline{\text{SEN}}$ is high. In 3-wire mode, commands are sent by first writing each argument to register(s) 0xA1–0xA3, then writing the command word to register 0xA0. A response is retrieved by reading registers 0xA8–0xAF.

Table 26. Register Map for 3-Wire Mode

3w Addr	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A0h	COMMAND1	CMD								ARG1							
A1h	COMMAND2	ARG2								ARG3							
A2h	COMMAND3	ARG4								ARG5							
A3h	COMMAND4	ARG6								ARG7							
A4h	Reserved1	Reserved								Reserved							
A5h	Reserved2	Reserved								Reserved							
A6h	Reserved3	Reserved								Reserved							
A7h	Reserved4	Reserved								Reserved							
A8h	STATUS/ RESPONSE1	CTS	ERR			RSDINT	RDSINT	ASQINT	STCINT	RESP1							
A9h	RESPONSE2	RESP2								RESP3							
AAh	RESPONSE3	RESP4								RESP5							
ABh	RESPONSE4	RESP6								RESP7							
ACh	RESPONSE5	RESP8								RESP9							
ADh	RESPONSE6	RESP10								RESP11							
AEh	RESPONSE7	RESP12								RESP13							
AFh	RESPONSE8	RESP14								RESP15							

In 3-wire mode, the control registers are accessed as 16-bit entities (2 byte). In Table 26, the full 8-bit 3-wire address is shown, including the chip's fixed base address (A7:A4 = 1010b). The first two bytes in a command stream uses register COMMAND1. The CMD byte occupies register COMMAND1[15:8], while ARG1 occupies register COMMAND1[7:0]. Commands with an odd number of bytes must have the lower 8 bits of the register containing the final argument byte filled with 0x00. Registers which are not specified by the command must either not be written, or must be filled with 0x0000 (user's discretion). Writing register COMMAND1 causes the command to execute. As a consequence, all registers containing applicable argument bytes must be written (in any order) prior to writing register COMMAND1. For example, when sending the SET_PROPERTY command, write registers COMMAND2..COMMAND3 first, then register COMMAND1. Note that ARG1 is part of register COMMAND1 and must be written at the same time as CMD. The contents of registers STATUS/RESPONSE1..RESPONSE8 are not valid until the CTS bit (STATUS/RESPONSE1[15]) is set. RESPONSE1[13:8] is updated after sending the GET_INT_STATUS command. Response bytes which are not specified in the response byte stream are not guaranteed to be 0x00 and should be ignored. For example, GET_PROPERTY has 4 bytes of response data in registers RESPONSE1..RESPONSE2. The contents of registers RESPONSE3..RESPONSE8 are meaningless and not guaranteed to be 0x0000. Likewise, for commands which have an odd number of response bytes, or a single status byte, the least significant byte (bits 7:0) of the final register is meaningless, and not guaranteed to be 0x00.

Table 27 demonstrates the command and response procedure implemented in the system controller to use the 3-wire bus mode. In this example the TX_TUNE_FREQ command is demonstrated.

Table 27. Command and Response Procedure—3-Wire Bus Mode

Action	Data	Description
CMD	0x30	TX_TUNE_FREQ.
ARG1	0x00	
ARG2	0x27	Set Station to 101.1 MHz
ARG3	0x7E	(0x277E = 10110 with 10 kHz step size)
STATUS	→0x80	Reply Status. Clear-to-send high.

To send the TX_TUNE_FREQ command and arguments, the system controller sets $\overline{SEN}$ = 0. Next, the controller drives the 9-bit control word on SDIO, consisting of the device address (A7:A5 = 101b), the write bit (0b), the device address (A4 = 0), and the register address for the COMMAND2 register (A3:A0 = 0001b). The control word is followed by a 16-bit data word, consisting of ARG2 followed by ARG3. The system controller then sets $\overline{SEN}$ = 1 and pulses the SCLK high and then low one final time. For commands requiring additional arguments, in the COMMAND3 (ARG3, ARG4) and COMMAND4 (ARG5, ARG6) registers, the system controller would send these next.

$\overline{SEN}$	CTL	ARG2	ARG3	$\overline{SEN}$	SCLK
1 → 0	101000001b	0x27	0x7E	0 → 1	Pulse

Next the system controller initiates the command by setting $\overline{SEN}$ = 0 and driving the 9-bit control word on SDIO, consisting of the device address (A7:A5 = 101b), the write bit (0b), the device address (A4 = 0), and the register address for the COMMAND1 register (A3:A0 = 0000b). The control word is followed by a 16-bit data word, consisting of the CMD byte followed by ARG1 byte. The system controller then sets $\overline{SEN}$ = 1 and pulses the SCLK high and then low one final time.

$\overline{SEN}$	CTL	CMD	ARG1	$\overline{SEN}$	SCLK
1 → 0	101000000b	0x30	0x00	0 → 1	Pulse

To read the status and response from the device, the system controller sets $\overline{SEN}$ = 0. Next, the controller drives the 9-bit control word 101101000b on SDIO, consisting of the device address (A7:A5 = 101b), the read bit (1b), the device address (A4 = 0), and the register address for the STATUS/RESPONSE1 register (A3:A0 = 1000b). The control word is followed by a 16-bit data word, consisting of STATUS followed by RESPONSE1. The system controller then sets $\overline{SEN}$ = 1 and pulses the SCLK high and then low one final time. In this example, the STATUS byte is 0x00, indicating that the CTS bit, bit 8, has not been set and that the response bytes are not ready for reading and that the device is not ready to accept another command. RESP1 will be random until the CTS bit is set. This process should be repeated until the STATUS byte indicates that CTS bit is set, 0x80 in this example.

$\overline{SEN}$	CTL	STATUS	RESP1	$\overline{SEN}$	SCLK
1 → 0	101101000b	0x00	0x00	0 → 1	Pulse

When the STATUS byte indicates that the CTS bit has been set, 0x80 in this example, the system controller may read the RESPONSE bytes from the device in any order.

$\overline{SEN}$	CTL	STATUS	RESP1	$\overline{SEN}$	SCLK
1 → 0	101101000b	0x80	0x00	0 → 1	Pulse

6.3. SPI Control Interface Mode

Figures 21 and 22 show the SPI Control Interface Read and Write Timing Parameters and Diagrams, respectively. Refer to the Si471x data sheet for timing parameter values.

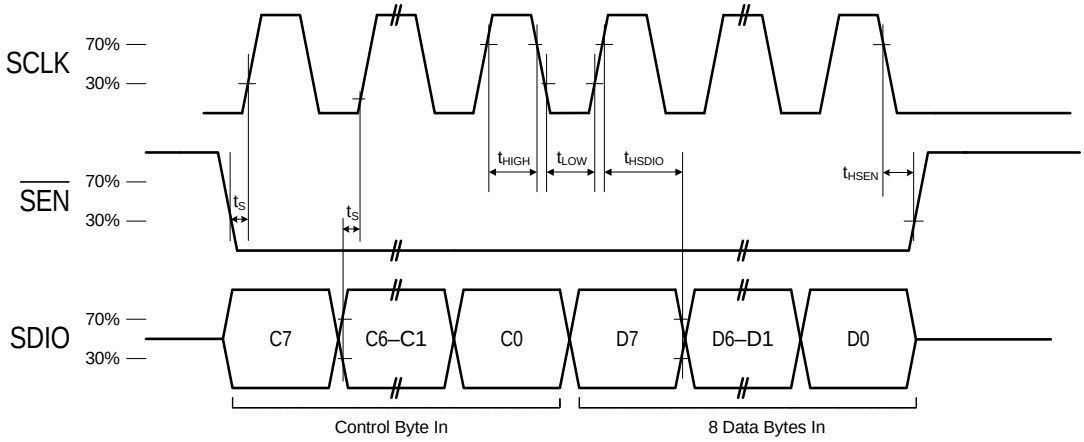


Figure 21. SPI Control Interface Write Timing Parameters

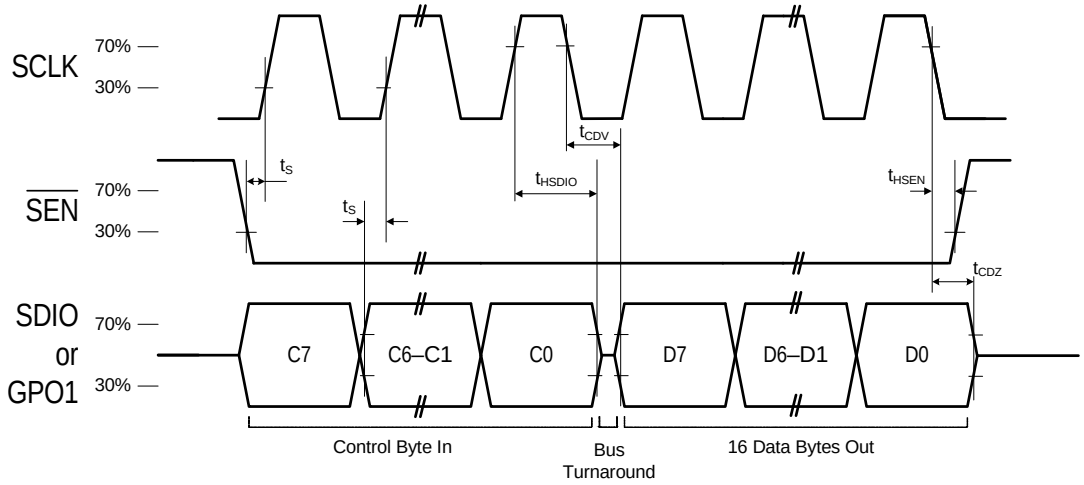


Figure 22. SPI Control Interface Read Timing Parameters

SPI bus mode uses the SCLK, SDIO and $\overline{\text{SEN}}$ pins for read/write operations. The system controller can choose to receive read data from the device on either SDIO or GPO1. A transaction begins when the system controller drives $\overline{\text{SEN}}$ = 0. The system controller then pulses SCLK eight times, while driving an 8-bit control byte serially on SDIO. The device captures the data on rising edges of SCLK. The control byte must have one of five values:

- 0x48 = write a command (controller drives 8 additional bytes on SDIO)
- 0x80 = read a response (device drives one additional byte on SDIO)
- 0xC0 = read a response (device drives 16 additional bytes on SDIO)
- 0xA0 = read a response (device drives one additional byte on GPO1)
- 0xE0 = read a response (device drives 16 additional bytes on GPO1)

For write operations, the system controller must drive exactly 8 data bytes (a command and arguments) on SDIO after the control byte. The data is captured by the device on the rising edge of SCLK.

For read operations, the controller must read exactly one byte (STATUS) after the control byte or exactly 16 data bytes (STATUS and RESP1–RESP15) after the control byte. The device changes the state of SDIO (or GPO1, if specified) on the falling edge of SCLK. Data must be captured by the system controller on the rising edge of SCLK.

Keep $\overline{SEN}$ low until all bytes have transferred. A transaction may be aborted at any time by setting $\overline{SEN}$ high and toggling SCLK high and then low. Commands will be ignored by the device if the transaction is aborted.

Table 28 demonstrates the command and response procedure that would need to be implemented in the system controller to use the SPI bus mode. In this example the TX_TUNE_FREQ command is demonstrated.

Table 28. Command and Response Procedure - SPI Bus Mode

Action	Data	Description
CMD	0x30	TX_TUNE_FREQ
ARG1	0x00	
ARG2	0x27	Set Station to 101.1 MHz
ARG3	0x7E	(0x277E = 10110 with 10 kHz step size)
STATUS	→0x80	Reply Status. Clear-to-send high.

To send the TX_TUNE_FREQ command and arguments, the system controller sets $\overline{SEN}$ = 0, sends the control byte 0x48, followed by the CMD byte and seven argument bytes, ARG1-ARG7, followed by setting $\overline{SEN}$ = 1. Note that all seven argument bytes must be sent by the controller or the command will fail. Unused arguments must be written as 0x00.

$\overline{SEN}$	CTL	CMD	ARG1	ARG2	ARG3	ARG4	ARG5	ARG6	ARG7	$\overline{SEN}$
1 → 0	0x48	0x30	0x00	0x27	0x7E	0x00	0x00	0x00	0x00	0 → 1

To read the status and response from the device, the system controller sets $\overline{SEN}$ = 0 and sends the control byte 0x80 to read the response on SDIO (or the control byte 0xA0 to read the response on GPO1). Next the system controller reads the STATUS byte. In this example, the STATUS byte is 0x00, indicating that the CTS bit, bit 8, has not been set and that the response bytes are not ready for reading. The device is not ready to accept another command. The system controller sets $\overline{SEN}$ = 1 to end the transfer. This process should be repeated until the STATUS byte indicates that CTS bit is set, 0x80 in this example.

$\overline{SEN}$	CTL	STATUS	$\overline{SEN}$
1 → 0	0x80	0x00	0 → 1

When the STATUS byte indicates that the CTS bit has been set, 0x80 in this example, the system controller may read the response bytes from the device. To read the status and response from the device, the system controller sets $\overline{SEN}$ = 0 and sends the control byte 0xC0 to read the response on SDIO (or the control byte 0xE0 to read the response on GPO1). Note that all 16 response bytes must be read from the device. Unused response bytes are random and should be ignored. Note that the TX_TUNE_FREQ command returns only the STATUS byte and RESP1–RESP15 bytes are shown only for completeness.

$\overline{SEN}$	CTL	STATUS	RESP1	RESP2	RESP3	RESP4	RESP5	RESP6	RESP7	RESP8	RESP9	RESP10	RESP11	RESP12	RESP13	RESP14	RESP15	$\overline{SEN}$
1 → 0	0xC0	0x80	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0 → 1

7. Powerup

There are two procedures for booting the device to move it from powerdown mode to the powerup mode. The first and most common is a boot from internal device memory. The second is a boot from a firmware patch that is written from the system controller to the device.

To power up the device:

1. Supply VDD and VIO while keeping the $\overline{RST}$ = 0.
   The minimum VDD and VIO rise time is 25 µs, and VDD and VIO must be stable 250 µs before setting $\overline{RST}$ = 1.
   Power supplies may be sequenced in any order.
   $\overline{RST}$ is in the VIO supply domain and therefore $\overline{RST}$ = 0 must be maintained before VIO is supplied.
2. Set GPO1 and GPO2 for the desired bus mode.
   The minimum setup time for GPO1 and GPO2 before $\overline{RST}$ = 1 is 30 ns when actively driven by the system controller and 100 µs if the internal 1 MΩ resistor is allowed to set the default GPO1 (high) and GPO2 (low).
3. Set $\overline{RST}$ = 1.
4. Write POWER_UP to the command register.
   The POWER_UP command instructs the device to boot from internal memory, see Section “7.1. Powerup from Device Memory”, or from a firmware patch sent from the system controller, see Section “7.2. Powerup from a Component Patch”. After CTS = 1, the device is ready to commence normal operation and accept additional commands. The POWER_UP command configures the state of DIN (pin 13, Si4732 pin 16), DFS (pin 14, Si4732 pin 1), and RIN (pin 15 on Si471x/2x and pin 16 on Si4704/05/3x-D62) and LIN (pin 16 on Si471x/2x and pin 15 on Si4704/05/3x-D62) for analog or digital audio modes and GPO2/INT for interrupt operation. Prior to this command these pins are set to high impedance. The GPIO_CTL and GPIO_SET commands configure the state of GPO2/INT and GPO3. Prior to this command these pins are set to high impedance.
5. Provide RCLK.
   Note that the RCLK buffer is in the VIO supply domain and may therefore be supplied at any time after VIO is supplied. The RCLK must be valid 10 ns before any command that enables the TX carrier, such as the TX_TUNE_FREQ command, and for 10 ns after any command that disables the carrier, such as the TX_TUNE_POWER command with a value of 0x00. The RCLK is required for proper AGC operation when the carrier is enabled. The RCLK may be removed or reconfigured when the carrier is disabled.

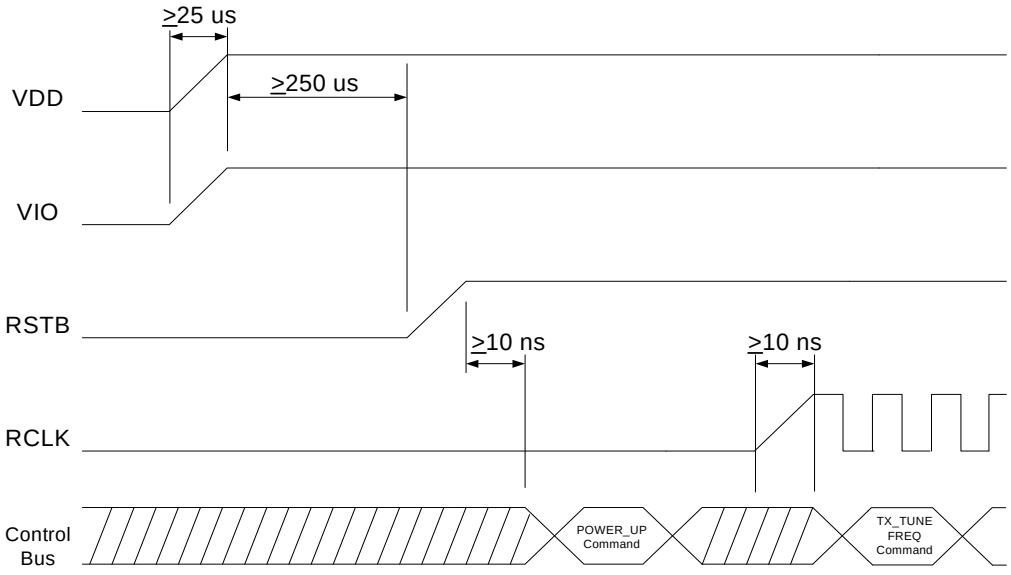


Figure 23. Device Power Up Timing

7.1. Powerup from Device Memory

Table 29. Using the POWER_UP Command for the FM Transmitter

Action	Data	Description
CMD	0x01	POWER_UP
ARG1	0x02	Set to FM Transmit.
ARG2	0x50	Set to Analog Line Input.
RESP1	→0x80	Reply Status. Clear-to-send high.

1. Send the POWER_UP command by writing the CMD field with value 0x01.
2. Send argument 1 of the power up command 0x02 (no patch, CTS and GPO2 interrupts disabled, FM transmit selected). Optionally various interrupts such as the CTS interrupt can be enabled by varying this argument, see Section “5. Commands and Properties”.
3. Send argument 2 of the power up command 0x50 (analog input selected)
4. Poll the CTS bit until it has been set high, or until a CTS interrupt is received if CTS interrupt is enabled.

Table 30. Using the POWER_UP command for the FM Receiver

Action	Data	Description
CMD	0x01	POWER_UP
ARG1	0x00	Set to FM Receive.
ARG2	0x05	Set to Analog Out.
STATUS	→0x80	Reply Status. Clear-to-send high.

1. Send the POWER_UP command by writing the CMD field with value 0x01.
2. Send ARG1, 0x00 (no patch, CTS and GPO2 interrupts disabled, FM receive selected). Optionally various interrupts such as the CTS interrupt can be enabled by varying this argument, see Section “5. Commands and Properties”.
3. Send ARG2, 0x05 (analog output is selected)
4. Poll the CTS bit until it has been set high, or until a CTS interrupt is received (if CTS interrupt is enabled).

Table 31. Using the POWER_UP Command for the AM/SW/LW Receiver

Action	Data	Description
CMD	0x01	POWER_UP
ARG1	0x01	Set to AM/SW/LW Receive.
ARG2	0x05	Set to Analog Out.
STATUS	→0x80	Reply Status. Clear-to-send high.

1. Send the POWER_UP command by writing the CMD field with value 0x01.
2. Send ARG1, 0x01 (no patch, CTS and GPO2 interrupts disabled, AM/SW/LW receive selected). Optionally various interrupts such as the CTS interrupt can be enabled by varying this argument, see Section “5. Commands and Properties”.
3. Send ARG2, 0x05 (analog output selected)
4. Poll the CTS bit until it has been set high, or until a CTS interrupt is received (if CTS interrupt is enabled).

Table 32. Using the POWER_UP Command for the FM Transmitter

Action	Data	Description
CMD	0x01	POWER_UP
ARG1	0x03	Set to Weather Band Receive.
ARG2	0x05	Set to Analog Out.
STATUS	→0x80	Reply Status. Clear-to-send high.

1. Send the POWER_UP command by writing the CMD field with value 0x01.
2. Send ARG1, 0x03 (no patch, CTS and GPO2 interrupts disabled, weather band receive selected). Optionally various interrupts such as the CTS interrupt can be enabled by varying this argument. See Section “5. Commands and Properties”.
3. Send ARG2, 0x05 (analog output selected).
4. Poll the CTS bit until it has been set high or until a CTS interrupt is received (if CTS interrupt is enabled).

7.2. Powerup from a Component Patch

The device has the ability to receive component patches from the system controller to modify sections or all of the device memory.

7.2.1. Patching Capabilities

In order to support interim updates to the device component, patches can be applied to the component by the system controller via a download mechanism. Patches can be provided by Skyworks Solutions to customers to address field issues, errata, or adjust device behavior. Patches are unique to a particular device firmware version and cannot be generated by customers.

Patches can be used to replace a portion of the component (to address errata for example) or to download an entirely new component image (to allow a customer to test a new component release on their device prior to receiving programmed parts).

Patches are tagged with a unique identification to allow them to be tracked and are encrypted requiring the customer to use a tag when downloading to allow the Si47xx to decrypt the patch.

Prior to downloading a partial patch, the user must confirm that the device contains the correct firmware and library to support the patch.

7.2.1.1. Examples

An FM transmitter component patch for Si471x firmware 2.0 with library R4 does not support Si471x firmware 1.0 with library R0.

For a programmatic indication, the POWER_UP command can be used to confirm the device library and firmware version. For a visual indication, the marking on the device can be used to confirm the firmware version. Tables 33 through 38 summarize the library and firmware mapping and compatibility.

Table 33. Si4704/05 Firmware, Library, and Component Compatibility

Part #	Firmware	Library	FMRX Component	AUXIN Component
Si4704/05-B20	2.0	R8	2.0	N/A
Si4704/05-C40	4.0	R10	5.0	N/A
Si4704/05-D50	5.0	R11	7.0	N/A
Si4704/05-D60	6.0	R11	7.0	N/A
Si4704/05-D62	6.2	R11	7.0	1.0

Table 34. Si4706 Firmware, Library, and Component Compatibility

Part #	Firmware	Library	FMRX Component
Si4706-B20	2.0	R8	3.0
Si4706-C30	3.0	R10	5.1
Si4706-D50	5.0	R11	7.0

Table 35. Si4707 Firmware, Library, and Component Compatibility

Part #	Firmware	Library	WBRX Component
Si4707-B20	2.0	R9	1.0

Table 36. Si4710/11/12/13 Firmware, Library, and Component Compatibility

Part #	Firmware	Library	FMTX Component
Si4710-A10	1.0	R0	1.0
Si4710/11/12/13-A20	2.0	R4	2.0
Si4710/11/12/13-B30	3.0	R8	3.0
Si4710/11/12/13-B31	3.1	R8	3.1

Table 37. Si4720/21 Firmware, Library, and Component Compatibility

Part #	Firmware	Library	FMTX Component	FMRX Component
Si4720-A10	1.0	R4	2.0	1.0
Si4720/21-B20	2.0	R8	3.0	2.0

Table 38. Si4730/31 Firmware, Library, and Component Compatibility

Part #	Firmware	Library	FMRX Component	AM_SW_LW RX Component	AUXIN Component
Si4730-A10	1.0	R4	1.0	1.0	N/A
Si4730/31-B20	2.0	R9	2.0	2.0	N/A
Si4730/31-C40	4.0	R10	6.0	5.0	N/A
Si4730/31-D50	5.0	R11	7.0	6.0	N/A
Si4730/31-D60	6.0	R11	7.0	6.0	N/A
Si4730/31-D62	6.2	R11	7.0	6.0	1.0

Table 39. Si4740/41/42/43/44/45 Firmware, Library, and Component Compatibility

Part #	Firmware	Library	FMRX Component	AMRX Component	WBRX Component
Si4740/41-C10	1.0	R10	4.0	3.0	N/A
Si4742/43-C10	1.0	R10	4.0	3.0	3.0

Table 39. Si4740/41/42/43/44/45 Firmware, Library, and Component Compatibility

Si4744/45-C10	1.0	R10	4.0	3.0	N/A

Table 40. Si4749 Firmware, Library, and Component Compatibility

Part #	Firmware	Library	FMRX Component
Si4749-C10	1.0	R10	4.0

Table 41. Si4734/35 Firmware, Library, and Component Compatibility

Part #	Firmware	Library	FMRX Component	AM_SW_LWRX Component
Si4734/35-B20	2.0	R9	2.0	2.1
Si4734/35-C40	4.0	R10	6.0	5.0
Si4734/35-D50	5.0	R11	7.0	6.0
Si4734/35-D60	6.0	R11	7.0	6.0

Table 42. Si4736/37 Firmware, Library, and Component Compatibility

Part #	Firmware	Library	FMRX Component	AM_SW_LWRX Component	WBRX Component
Si4736/37-B20	2.0	R9	2.0	2.0	1.0
Si4736/37-C40	4.0	R10	6.0	5.0	5.0

Table 43. Si4738/39 Firmware, Library, and Component Compatibility

Part #	Firmware	Library	FMRX Component	WBRX Component
Si4738/39-B20	2.0	R9	2.0	1.0
Si4738/39-C40	4.0	R10	6.0	5.0

Table 44. Si4784/85 Firmware, Library, and Component Compatibility

Part #	Firmware	Library	FMRX Component
Si4784/85-B20	2.0	R8	2.0
Si4784/85-D50	5.0	R11	7.0

Table 45. Si4732 Firmware, Library, and Component Compatibility

Part #	Firmware	Library	FMRX Component	AM_SW_LWRX Component
Si4732-A10	1.0	R11	7.0	6.0

7.2.2. Patching Procedure

Patching is accomplished by sending a series of commands to the device. These commands are sent in the same manner as any other device commands and can be sent over any of the command busses (2-wire, 3-wire, SPI).

The first command that is sent to the device is the POWER_UP command to confirm that the patch is compatible with the internal device library revision. The device moves into the powerup mode, returns the reply, and moves into the powerdown mode. The POWER_UP command is sent to the device again to configure the mode of the device and additionally is used to start the patching process. When applying the patch, the PATCH bit in ARG1 of the POWER_UP command must be set to 1 to begin the patching process.

Once the POWER_UP command is sent and the device is placed in patch mode, the patch file can be sent to the device. The patch file typically has a .csg extension. It is formatted into 8 columns, consisting of a leading command (0x15 or 0x16), and 7 arguments. The controlling system must send each line of 8 bytes, wait for a CTS, then send the next set of 8, etc., until the entire patch has been sent. An example showing the first few lines and final line of a patch file is shown below.

The patch download mechanism is verified with a checksum embedded in the patch download. If the checksum fails, the part issues an error code, ERR (bit 6 of the one byte reply that is available after each 8-byte transfer), and halts. The part must be reset to recover from this error condition.

The following is an example of a patch file.

```
# Copyright 2006 Skyworks Solutions, Inc.
# Patch generated 21:09 August 09 2006
# fmtx version 0.0 alpha
0x15,0x00,0x0B,0x1D,0xBB,0x14,0xC4,0xA1
0x16,0x98,0x81,0xD9,0x71,0xED,0x0E,0xAC
.
.
[up to 1979 additional lines]
.
.
0x15,0x00,0x00,0x00,0x00,0x00,0x49,0xFD
```

A full memory patch requires 15856 bytes of system controller memory, however, most patches require significantly less memory. In 2-wire mode, a full memory patch download requires approximately 500 ms at a 400 kHz clock rate. The following is an example of the commands required to boot the device from powerdown mode using the patch file in the previous example. The device has completed the boot process when the CTS bit is set high after the last byte in the file is transferred and is ready to accept additional commands and proceed with normal operation.

Table 46 provides an example of using the POWER_UP command with patching enabled. The table is broken into three columns. The first column lists the action taking place: command (CMD), argument (ARG), status (STATUS) or response (RESP). The second column lists the data byte or bytes in hexadecimal that are being sent or received. An arrow preceding the data indicates data being sent from the device to the system controller. The third column describes the action.

Table 46. Example POWER_UP Command with Patching Enabled

Action	Data	Description
CMD	0x01	POWER_UP
ARG1	0xCF	Set to Read Library ID, Enable Interrupts.
ARG2	0x50	Set to Analog Line Input.
STATUS	→0x80	Reply Status. Clear-to-send high.
RESP1	→0x0D	Part Number, HEX (0x0D = Si4713)
RESP2	→0x32	Firmware Major Rev, ASCII (0x32 = 2)
RESP3	→0x30	Firmware Minor Rev, ASCII (0x30 = 0)
RESP4	→0x00	Reserved
RESP5	→0x00	Reserved
RESP6	→0x41	Chip Rev, ASCII (0x41 = revA)
RESP7	→0x04	Library ID, HEX (0x04 = library 4)
CMD	0x01	POWER_UP
ARG1	0xE2	Set to FM Transmit, set patch enable, enable interrupts.
ARG2	0x50	Set to Analog Line Input.
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x15	Reserved for Patch.
ARG1	0x00	
ARG2	0x0B	
ARG3	0x1D	
ARG4	0xBB	
ARG5	0x14	
ARG6	0xC4	
ARG7	0xA1	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x16	Reserved for Patch.
ARG1	0x98	
ARG2	0x81	
ARG3	0xD9	
ARG4	0x71	
ARG5	0xED	
ARG6	0x0E	
ARG7	0xAC	
STATUS	→0x80	Reply Status. Clear-to-send high.
. . [up to 1979 additional lines] .		
CMD	0x15	Reserved for Patch.
ARG1	0x00	
ARG2	0x00	
ARG3	0x00	
ARG4	0x00	
ARG5	0x00	
ARG6	0x49	
ARG7	0xFD	
STATUS	→0x80	Reply Status. Clear-to-send high.

8. Powerdown

The procedure for moving the device from powerup to powerdown modes requires writing the POWER_DOWN command.

Table 47. Using the POWER_DOWN command

Action	Data	Description
CMD	0x11	POWER_DOWN
STATUS	→0x80	Reply Status. Clear-to-send high.

To Power Down the device and remove VDD and VIO (optional):

1. Write TX_TUNE_POWER to the command register to disable the carrier.
2. Set RCLK = 0 (optional).
   Note that the RCLK buffer is in the VIO supply domain and may therefore be supplied at any time that VIO is supplied. The RCLK must be valid 10 ns before and 10 ns after sending the TX_TUNE_MEASURE, TX_TUNE_FREQ, and TX_TUNE_POWER commands. In addition, the RCLK must be valid at all times when the carrier is enabled for proper AGC operation. The RCLK may be removed or reconfigured at other times. The RCLK is required for proper AGC operation when the carrier is enabled. The RCLK may be removed or reconfigured when the carrier is disabled.
3. Write POWER_DOWN to the command register.
   Note that all register contents will be lost.
4. Set $\overline{RST}$ = 0.
   Note that $\overline{RST}$ must be held high for 10 ns after the completion of the POWER_DOWN command.
5. Remove VDD (optional).
6. Remove VIO (optional).
   Note that VIO must not be removed without removing VDD. **Unexpected device operation may result.**

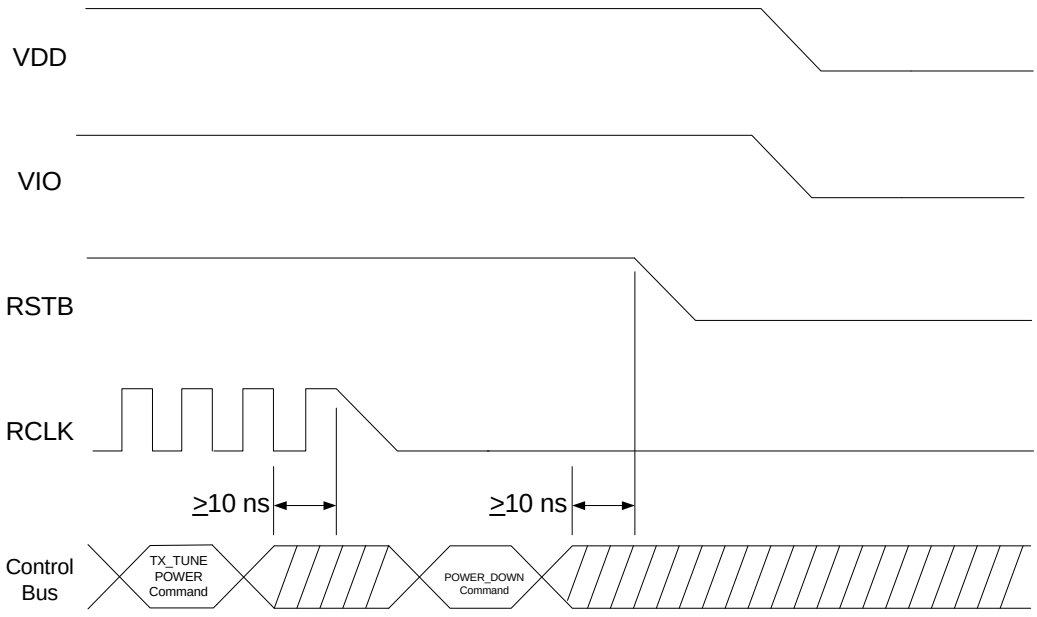


Figure 24. Device Power Down Timing

9. Digital Audio Interface

The digital audio interface operates in slave mode and supports 3 different audio data formats:

- I^2S
- Left-Justified
- DSP Mode

In I^2S mode, the MSB is captured on the second rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order down to the LSB. The Left Channel is transferred first when the DFS is low, and the Right Channel is transferred when the DFS is high.

In Left-Justified mode, the MSB is captured on the first rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order down to the LSB. The Left Channel is transferred first when the DFS is high, and the Right Channel is transferred when the DFS is low.

In DSP mode, the DFS becomes a pulse with a width of 1 DCLK period. The Left Channel is transferred first, followed right away by the Right Channel. There are two options in transferring the digital audio data in DSP mode: the MSB of the left channel can be transferred on the first rising edge of DCLK following the DFS pulse or on the second rising edge.

In all audio formats, depending on the word size, DCLK frequency and sample rates, there may be unused DCLK cycles after the LSB of each word before the next DFS transition and MSB of the next word.

The number of audio bits can be configured for 8, 16, 20, or 24 bits.

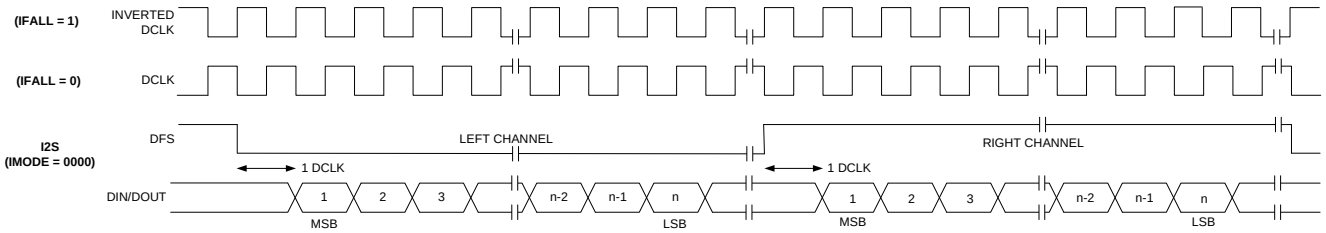


Figure 25. I^2S Digital Audio Format

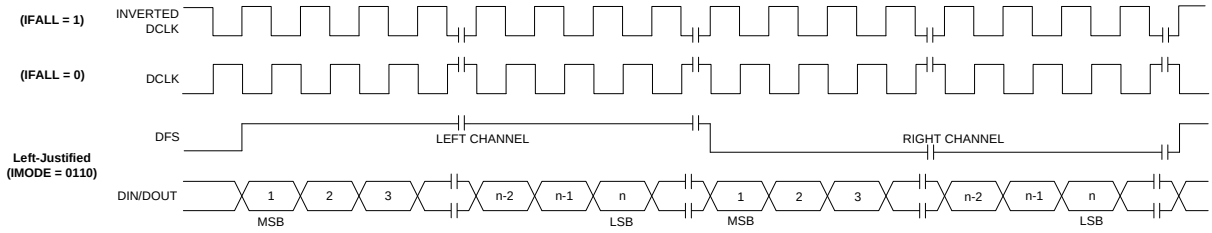


Figure 26. Left-Justified Digital Audio Format

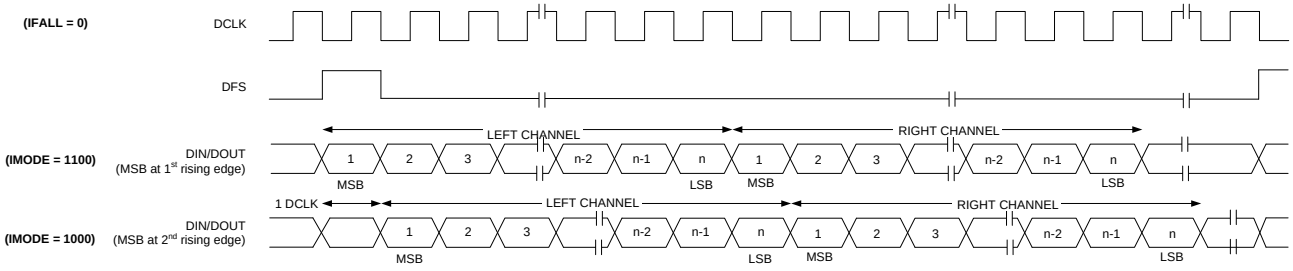


Figure 27. DSP Digital Audio Format

There are two additional properties each for FM Transmitter and AM/FM/SW/LW Receiver associated with using

digital audio input/output. Note that digital audio is not supported in WB Receiver.

For FM Transmitter:

1. Property 0x0101: DIGITAL_INPUT_FORMAT
2. Property 0x0103: DIGITAL_INPUT_SAMPLE_RATE

For AM/FM/SW/LW Receiver:

1. Property 0x0102: DIGITAL_OUTPUT_FORMAT
2. Property 0x0104: DIGITAL_OUTPUT_SAMPLE_RATE

The procedure for using a digital audio is as follow:

1. When the device is powered up, the default value for DIGITAL_INPUT_SAMPLE_RATE or DIGITAL_OUTPUT_SAMPLE_RATE is 0 (disable digital audio in/out).
2. User then must supply DCLK and DFS prior to setting the DIGITAL_INPUT_SAMPLE_RATE or DIGITAL_OUTPUT_SAMPLE_RATE property.
3. This procedure can be applied anytime after the chip is powered up.
4. User may also change or disable DCLK/DFS during operation. Prior to changing or disabling DCLK/DFS, user has to set the DIGITAL_INPUT_SAMPLE_RATE or DIGITAL_OUTPUT_SAMPLE_RATE property to 0. After changing or re-enabling DCLK/DFS, user then can set the sample rate property again.
5. The property DIGITAL_INPUT_FORMAT and DIGITAL_OUTPUT_FORMAT does not have a condition, thus it can be set anywhere after power up.

Notes:

1. Failure to provide DCLK and DFS prior to setting the sample rate property may cause the chip to go into an unknown state and user must reset the chip.

2. The DIGITAL_INPUT_SAMPLE_RATE or DIGITAL_OUTPUT_SAMPLE_RATE is the audio sampling rate (DFS rate) and is valid between 32kHz and 48kHz.

The following table is a programming example of how to use digital audio.

Table 48. Digital Audio Programming Example

Action	Data	Description
		Action: POWER UP CHIP (look at respective programming example of power up in digital mode).
		Action: User can send other commands or properties here.
		Action: Supply DCLK and DFS.
CMD ARG1 ARG2 (PROP) ARG3 (PROP) ARG4 (PROPD) ARG5 (PROPD) STATUS	0x12 0x00 0x01 0x03 or 0x04 0xBB 0x80 →0x80	SET_PROPERTY DIGITAL_INPUT_SAMPLE_RATE or DIGITAL_OUTPUT_SAMPLE_RATE Sample rate = 0xBB80 = 48000Hz Reply Status. Clear-to-send high.
CMD ARG1 ARG2 (PROP) ARG3 (PROP) ARG4 (PROPD) ARG5 (PROPD) STATUS	0x12 0x00 0x01 0x01 or 0x02 0x00 0x00 →0x80	SET_PROPERTY DIGITAL_INPUT_FORMAT or DIGITAL_OUTPUT_FORMAT Mode: I2S, stereo, 16bit, sample on rising edge of DCLK Reply Status. Clear-to-send high.
		Action: User can send other commands or properties here.

Table 48. Digital Audio Programming Example

		Action: User needs to change or disable DCLK/DFS.
CMD ARG1 ARG2 (PROP) ARG3 (PROP) ARG4 (PROPD) ARG5 (PROPD) STATUS	0x12 0x00 0x01 0x03 or 0x04 0x00 0x00 →0x80	SET_PROPERTY DIGITAL_INPUT_SAMPLE_RATE or DIGITAL_OUTPUT_SAMPLE_RATE Sample rate = 0 (disable digital audio) Reply Status. Clear-to-send high.
		Action: User now is allowed to change or disabling DCLK/DFS.
		Action: DCLK/DFS has been changed or re-enabled.
CMD ARG1 ARG2 (PROP) ARG3 (PROP) ARG4 (PROPD) ARG5 (PROPD) STATUS	0x12 0x00 0x01 0x03 or 0x04 0xBB 0x80 →0x80	SET_PROPERTY DIGITAL_INPUT_SAMPLE_RATE or DIGITAL_OUTPUT_SAMPLE_RATE Sample rate = 0xBB80 = 48000Hz Reply Status. Clear-to-send high.
		Action: User can send other commands or properties here.

10. Timing

There are two indicators: CTS (Clear to Send) and STC (Seek/Tune Complete) to indicate that a command has been accepted and execution completed by the part.

After sending every command, the CTS bit will be set indicating that the command has been accepted by the part and it is ready to receive the next command. The CTS bit, on most commands, also indicates that the command has completed execution. These commands are:

1. POWER_UP, POWER_DOWN, GET_REV, GET_PROPERTY, GPIO_CTL, GPIO_SET
2. On FM Transmitter component: TX_TUNE_STATUS, TX_ASQ_STATUS, TX_RDS_BUFF, TX_RDS_PS
3. On FM Receive component: FM_TUNE_STATUS, FM_RSQ_STATUS, FM_RDS_STATUS
4. On AM/SW/LW Receive component: AM_TUNE_STATUS, AM_RSQ_STATUS
5. On WB Receive component: WB_TUNE_STATUS, WB_RSQ_STATUS, WB_ASQ_STATUS

The CTS timing model is shown in Figure 28 and the timing parameters for each command are shown in Table 49.

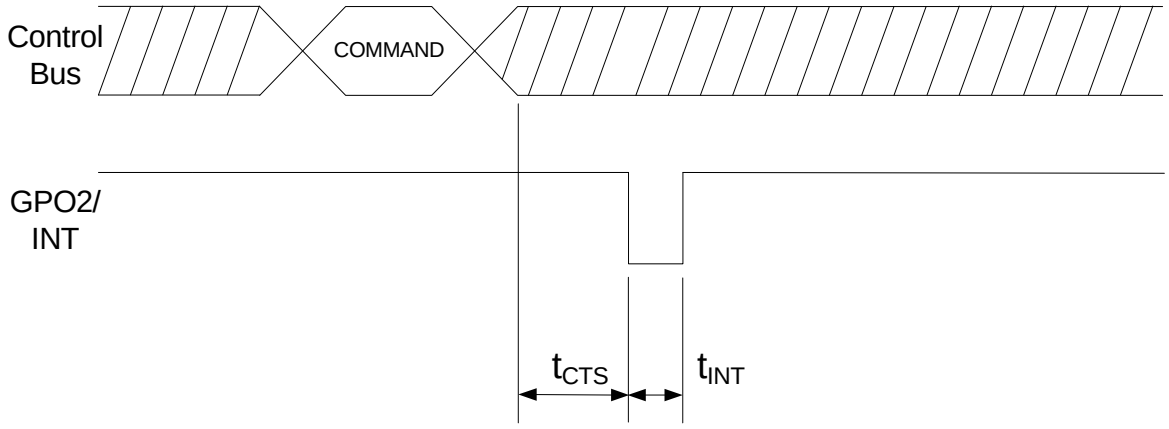


Figure 28. CTS Timing Model

In addition to CTS bit, there are a few commands (e.g. TX_TUNE_FREQ or FM_TUNE_FREQ) that use the STC bit to indicate that the command has completed execution. It is highly recommended that user waits for the STC bit before sending the next command. When interrupt is not used, user can poll the status of this STC bit by sending the GET_INT_STATUS command until the STC bit has been set before sending the next command.

Commands that use STC bit to indicate execution has been completed:

1. On FM Transmitter component: TX_TUNE_FREQ, TX_TUNE_POWER, TX_TUNE_MEASURE
2. On FM Receive component: FM_TUNE_FREQ, FM_SEEK_START
3. On AM/SW/LW Receive component: AM_TUNE_FREQ, AM_SEEK_START
4. On WB Receive component: WB_TUNE_FREQ

The CTS and STC timing model is shown in Figure 29 and the timing parameters for each command are shown in Table 49.

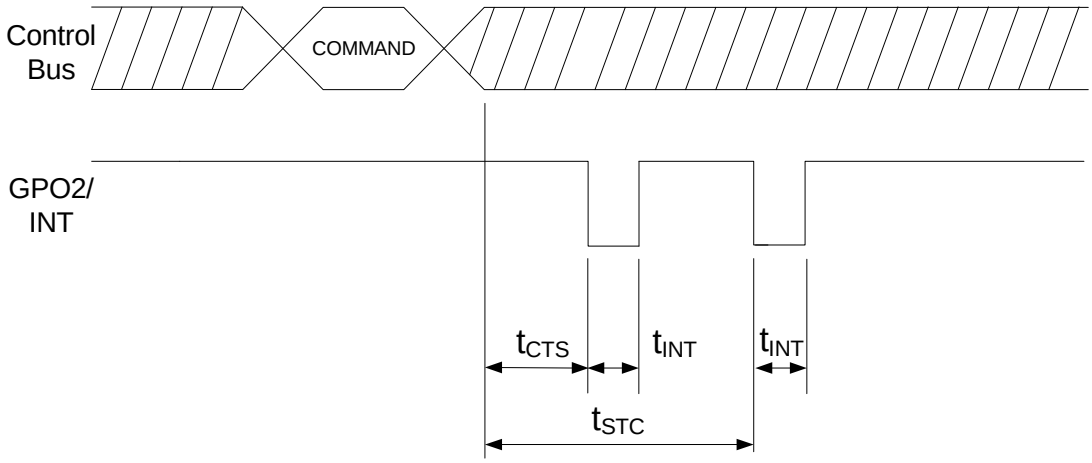


Figure 29. CTS and STC Timing Model

The SET_PROPERTY command does not have an indicator telling when the command has completed execution, rather the timing is guaranteed and it is called t_{COMP}. The CTS and SET_PROPERTY command completion timing model t_{COMP} is shown in Figure 30 and the timing parameters for each command are shown in Table 49.

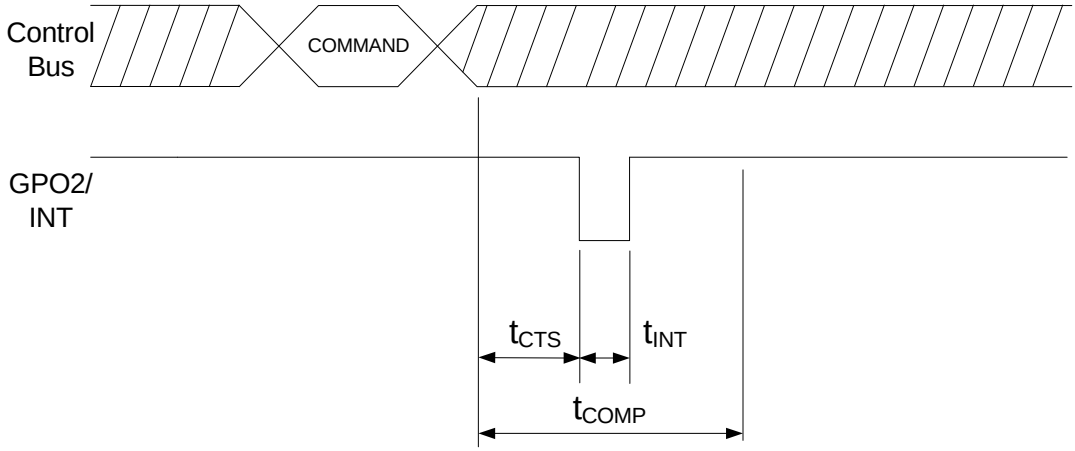


Figure 30. CTS and SET_PROPERTY Command Complete t_{COMP} Timing Model

Table 49. Command Timing Parameters for the FM Transmitter

Command	t_{CTS}	t_{STC}	t_{COMP}	t_{INT}
POWER_UP	110 ms	—	—	1 µs
POWER_DOWN	300 µs	—	—	
GET_REV		—	—	
GET_PROPERTY		—	—	
GET_INT_STATUS		—	—	
PATCH_ARGS		—	—	
PATCH_DATA		—	—	
TX_ASQ_STATUS		—	—	
TX_RDS_BUFF		—	—	
TX_RDS_PS		—	—	
TX_TUNE_STATUS		—	—	
TX_TUNE_FREQ		100 ms	—	
TX_TUNE_MEASURE		100 ms	—	
TX_TUNE_POWER		20 ms	—	
SET_PROPERTY		—	10 ms	
GPIO_CTL		—	—	
GPIO_SET		—	—	

Table 50. Command Timing Parameters for the FM Receiver

Command	t_{CTS}	t_{STC}	t_{COMP}	t_{INT}
POWER_UP	110 ms	—	—	1 µs
POWER_DOWN	300 µs	—	—	
GET_REV		—	—	
GET_PROPERTY		—	—	
GET_INT_STATUS		—	—	
PATCH_ARGS		—	—	
PATCH_DATA		—	—	
FM_RSQ_STATUS		—	—	
FM_RDS_STATUS		—	—	
FM_TUNE_STATUS		—	—	
FM_TUNE_FREQ		60 ms[1]	—	
FM_SEEK_START		60 ms[2]	—	
SET_PROPERTY		—	10 ms	
FM_AGC_STATUS		—	—	
FM_AGC_OVERRIDE		—	—	
GPIO_CTL		—	—	
GPIO_SET		—	—	

Notes:

1. t_{STC} for FM_TUNE_FREQ / FM_SEEK_START commands is 80 ms on FMRX component 2.0 and earlier.
2. t_{STC} is seek time per channel. Total seek time depends on bandwidth, channel spacing, and number of channels to next valid channel.
   Worst case seek time complete for FM_SEEK_START is:

$$\left(\left(\frac{\text{FM\_SEEK\_BAND\_TOP} - \text{FM\_SEEK\_BAND\_BOTTOM}}{\text{FM\_SEEK\_FREQ\_SPACING}}\right) + 1\right) \times t_{STC}$$

   for USA FM:

$$\left(\left(\frac{10790 - 8750}{20}\right) + 1\right) \times 60\ \text{ms} = 6.2\ \text{s}$$

Table 51. Command Timing Parameters for the AM Receiver

Command	t_{CTS}	t_{STC}	t_{COMP}	t_{INT}
POWER_UP	110 ms	—	—	1 µs
POWER_DOWN	300 µs	—	—	
GET_REV		—	—	
GET_PROPERTY		—	—	
GET_INT_STATUS		—	—	
PATCH_ARGS		—	—	
PATCH_DATA		—	—	
AM_RSQ_STATUS		—	—	
AM_TUNE_STATUS		—	—	
AM_TUNE_FREQ		80 ms	—	
AM_SEEK_START		80 ms*	—	
SET_PROPERTY		—	10 ms	
GPIO_CTL		—	—	
GPIO_SET		—	—	

***Note:** t_{STC} is seek time per channel. The worst-case seek time per channel is 200 ms.Total seek time depends on bandwidth, channel spacing, and number of channels to next valid channel.

Worst case seek time complete for AM_SEEK_START is:

$$\left(\left(\frac{\text{AM\_SEEK\_BAND\_TOP} - \text{AM\_SEEK\_BAND\_BOTTOM}}{\text{AM\_SEEK\_FREQ\_SPACING}}\right) + 1\right) \times t_{STC}$$

for USA AM:

$$\left(\left(\frac{1710 - 520}{10}\right) + 1\right) \times 200\ \text{ms} = 24.0\ \text{s}$$

Table 52. Command Timing Parameters for the WB Receiver

Command	t_{CTS}	t_{STC}	t_{COMP}	t_{INT}
POWER_UP	110 ms	—	—	1 µs
POWER_DOWN	300 µs	—	—	
GET_REV		—	—	
GET_PROPERTY		—	—	
GET_INT_STATUS		—	—	
PATCH_ARGS		—	—	
PATCH_DATA		—	—	
WB_RSQ_STATUS		—	—	
WB_ASQ_STATUS		—	—	
WB_TUNE_STATUS		—	—	
WB_TUNE_FREQ		250 ms	—	
SET_PROPERTY		—	10 ms	
WB_AGC_STATUS		—	—	
WB_AGC_OVERRIDE		—	—	
GPIO_CTL		—	—	
GPIO_SET		—	—	

Table 53. Command Timing Parameters for the Stereo Audio ADC Mode

Command	t_{CTS}	t_{COMP}	t_{INT}
POWER_UP	110 ms	—	1 µs
POWER_DOWN	300 µs	—	
GET_REV		—	
GET_PROPERTY		—	
GET_INT_STATUS		—	
AUX_ASRC_START		—	
AUX_ASQ_STATUS		—	
GPIO_CTL		—	
GPIO_SET		—	
SET_PROPERTY		10 ms	

11. FM Transmitter

The FM Transmitter audio signal chain involves Audio Dynamic Range Control, Pre-emphasis and Limiter function. Understanding what these three function blocks do in the signal chain will help user in maximizing the volume out of the FM Transmitter.

11.1. Audio Dynamic Range Control for FM Transmitter

The audio dynamic range control can be used to reduce the dynamic range of the audio signal. Audio dynamic range reduction increases the transmit volume by decreasing the peak amplitudes of audio signals and increasing the root mean square content of the audio signal. In other words, it amplifies signals below the threshold by a fixed gain and compresses audio signals above the threshold by the ratio of Threshold/(Gain + Threshold). Figure 31 shows an example transfer function of an audio dynamic range controller with the threshold set at –40 dBFS and a Gain = 20 dB relative to an uncompressed transfer function.

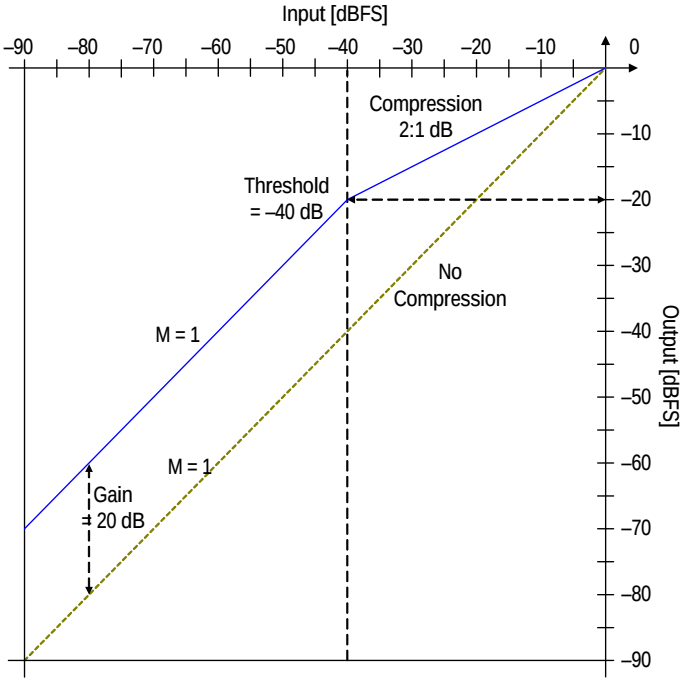


Figure 31. Audio Dynamic Range Transfer Function

For input signals below the threshold of –40 dBFS, the output signal is amplified or gained up by 20 dB relative to an uncompressed signal. Audio inputs above the threshold are compressed by a 2 to 1 dB ratio, meaning that every 2 dB increase in audio input level above the threshold results in an audio output increase of 1 dB. In this example, the input dynamic range of 90 dB is reduced to an output dynamic range of 70 dB. The FM Transmitter includes digital audio dynamic range control with programmable gain, threshold, attack rate, and release rate. The total dynamic range reduction is set by the gain value and the audio output compression above the threshold is equal to Threshold/(Gain + Threshold) in dB. The gain specified cannot be larger than the absolute value of the threshold. This feature can also be disabled if audio compression is not desired. Figure 32 shows the time domain characteristics of the audio dynamic range controller. The attack rate sets the speed with which the audio dynamic range controller responds to changes in the input level, and the release rate sets the speed with which the audio dynamic range controller returns to no compression once the audio input level drops below the threshold. When using the audio dynamic range control, care must be taken to configure the device such that the sum of the threshold and gain is zero, or less, as not to distort or overmodulate.

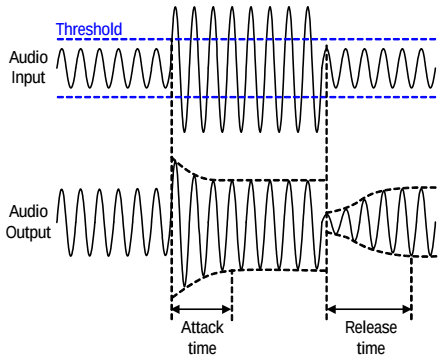


Figure 32. Time Domain Characteristics of the Audio Dynamic Range Controller

11.2. Audio Pre-emphasis for FM Transmitter

Pre-emphasis and de-emphasis are techniques used to improve the signal-to-noise ratio of an FM stereo broadcast by reducing the effects of high-frequency noise. A pre-emphasis filter is applied to the broadcast to accentuate the high audio frequencies and a de-emphasis filter is used by the receiver to attenuate high frequencies and restore a flat frequency response. Depending on the region, a time constant of either 50 or 75 µs is used. The frequency response of both of these filters is shown in Figure 33. For a 75 µs filter, a 15 kHz tone is amplified by ~17 dB. For a 50 µs filter, a 15 kHz tone is amplified by ~13.5 dB. The pre-emphasis time constant is programmable to off, 50 or 75 µs and is setting the TX_PREEMPHASIS property. When using the pre-emphasis filter, care must be taken to account for amplification at high frequencies as not to distort or overmodulate.

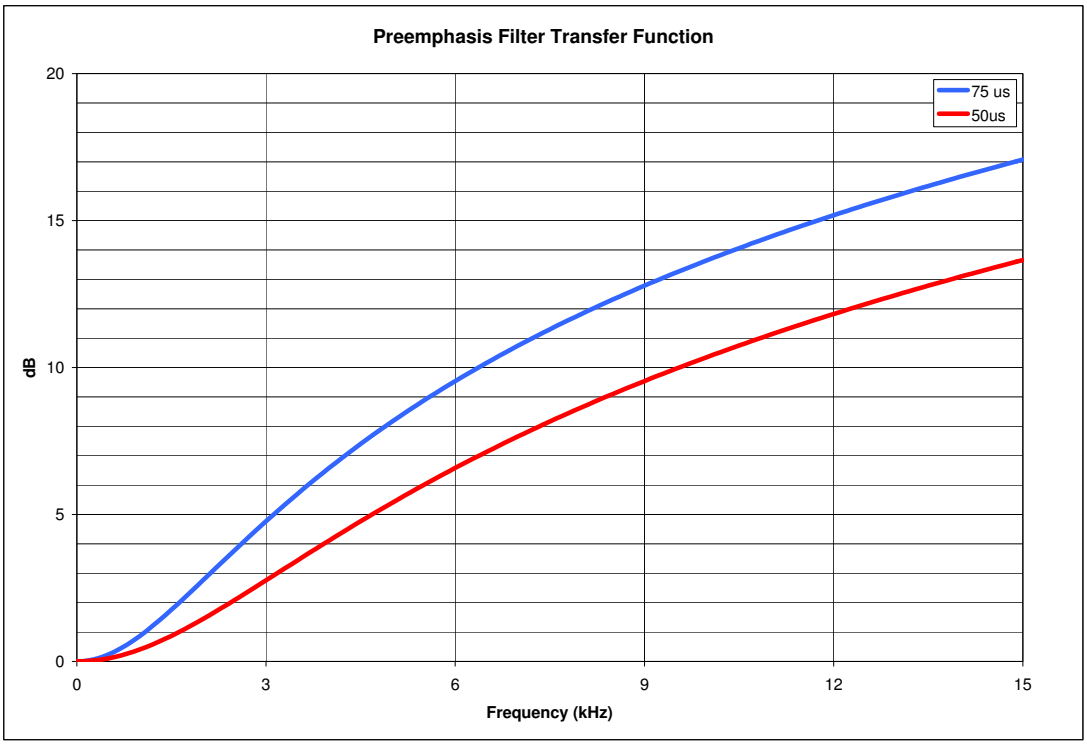


Figure 33. Pre-emphasis Filter Response

11.3. Audio Limiter for FM Transmitter

A limiter is available to prevent overmodulation by dynamically attenuating the audio level such that the maximum audio deviation does not exceed the level set by the TX_AUDIO_DEVIATION property. The limiter is useful when trying to maximize the audio volume, minimize receiver-generated distortion and prevent overmodulation that may result in violating FCC and ETSI modulation limits. The OVERMOD bit is set by the device when the peak voltage prior to the limiter exceeds the level set by the TX_AUDIO_DEVIATION property. When the limiter is enabled, the OVERMOD bit is an indication that the limiter has dynamically attenuated the audio level. The limiter attack time is instantaneous (within on sample period) and the release time is adjustable with the TX_LIMITER_RELEASE_TIME property.

Note: Limiter is enabled by default.

11.4. Maximizing Audio Volume for FM Transmitter

The audio input chain is shown in Figure 34:

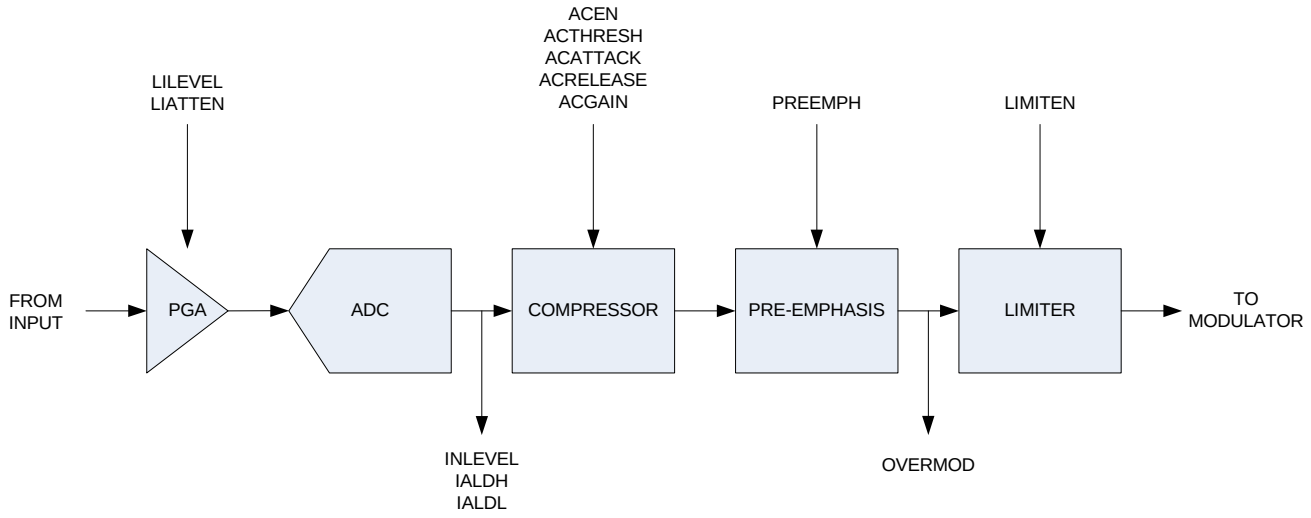


Figure 34. Audio Input Chain

To maximize audio volume:

1. **Set the input line attenuation, line level and audio deviation.**

   The input line attenuation should be set to the lowest setting that is above the maximum level provided by the audio source, either 190, 301, 416 or 636 mV_{PK}.

   The line level should be set to the maximum source audio level plus headroom. When the limiter is enabled, 2 dB of headroom is recommended. 2 dB of headroom is recommended so that the limiter will not be engaged the entire time it is enabled. When the limiter is disabled and 50 µs pre-emphasis is selected, 13.5 dB of headroom is required. When the limiter is disabled and 75 µs pre-emphasis is selected, 17 dB of headroom is required. Table 54 summarizes these settings:

Table 54. Line Input Headroom

Pre-emphasis	Limiter On (dB)	Limiter Off (dB)
Off	0	0
50 µs	0	13.5
75 µs	0	17

The audio deviation should be set as high as possible, with the constraint that the sum of the audio, pilot and RDS deviation must be 75 kHz or less. Typical settings are 66.25 kHz audio deviation, 6.75 kHz pilot deviation and 2 kHz RDS deviation.

Example 1:
An application providing a 150 mV_{PK} input to the device on RIN/LIN would set Line Attenuation = 00, resulting in a maximum permissible input level of 190 mV_{PK} on LIN/RIN and an input resistance of 396 kΩ. With 50 µs pre-emphasis and the limiter disabled, the Line Level would be set to 150 mV_{PK} and the source level would be adjusted down by 13.5 dB to 30 mV_{PK} to compensate for pre-emphasis. With the limiter enabled, the input source can be maintained at 150 mV_{PK}, but the line level should be set at 188 mV_{PK} to give 2 dB headroom.

Example 2:
An application providing a 1 V_{PK} input to the device on RIN/LIN would set Line Attenuation = 11, resulting in a maximum permissible input level of 636 mV_{PK} on LIN/RIN and an input resistance of 60 kΩ. An external series resistor on LIN and RIN inputs of 58 kΩ would create a resistive voltage divider that would keep the maximum line level on RIN/LIN below 509 mV_{PK} to give a 2 dB headroom. With input signal at 509 mV_{PK}, 75 µs pre-emphasis and the limiter enabled, the Line Level can be set to 636 mV_{PK}.

2. **Enable the audio dynamic range control**
In general the greater the sum of threshold and gain, the greater the perceived audio volume. The following examples demonstrate minimal and aggressive compression schemes. When using the audio dynamic range control, care must be taken to configure the device such that the sum of the threshold and gain is zero, or less, as not to distort or overmodulate. In practice, the sum of the threshold and gain will be less than zero to minimize the possibility for distortion.

Example 1 (minimal compression):
SETPROPERTY: TX_ACOMP_THRESHOLD = –40 dBFS
SETPROPERTY: TX_ACOMP_ATTACK_TIME = 5 ms
SETPROPERTY: TX_ACOMP_RELEASE_TIME = 100 ms
SETPROPERTY: TX_ACOMP_GAIN = 15 dB

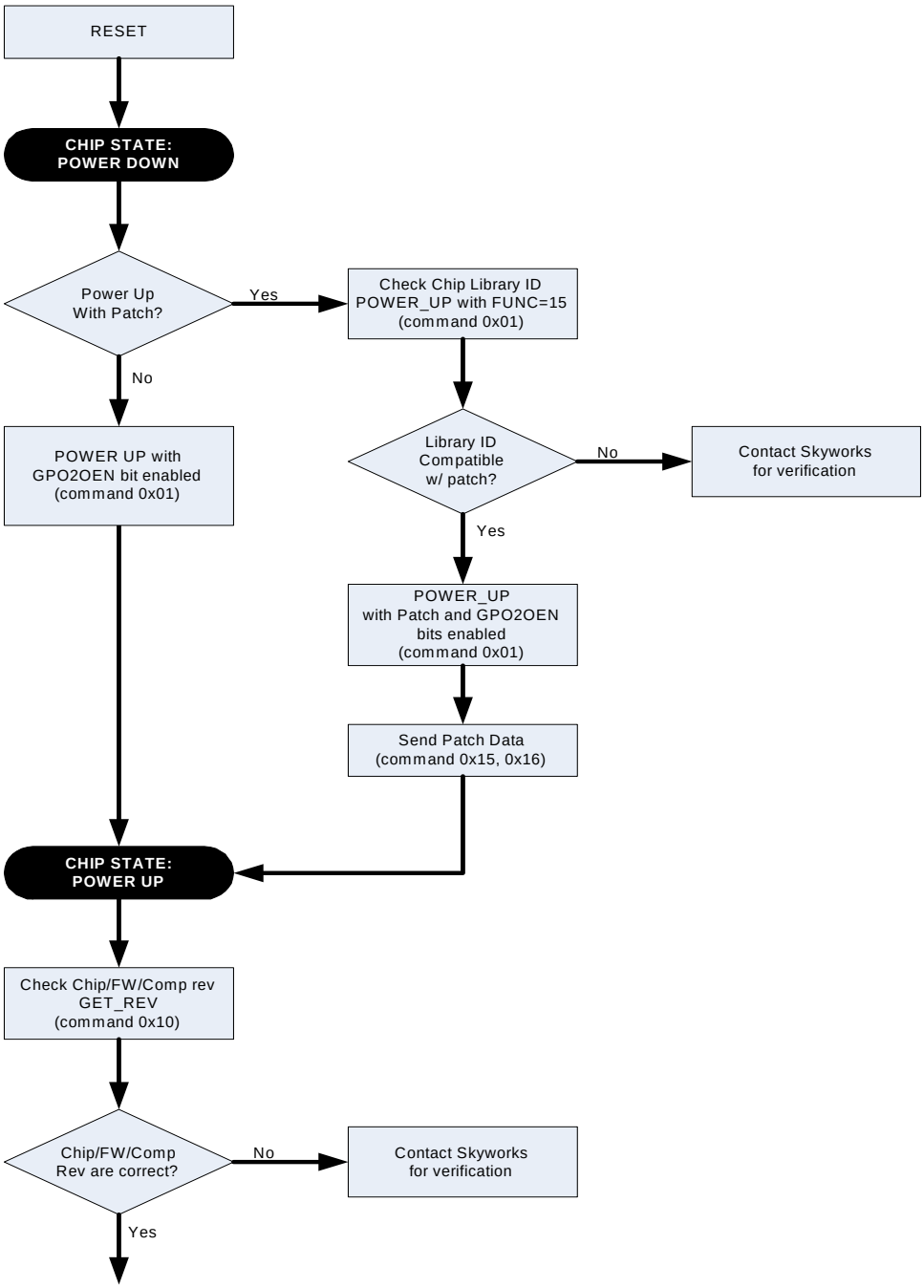
Example 2 (aggressive compression):
SETPROPERTY: TX_ACOMP_THRESHOLD = –15 dBFS
SETPROPERTY: TX_ACOMP_ATTACK_TIME = 0.5 ms
SETPROPERTY: TX_ACOMP_RELEASE_TIME = 1000 ms
SETPROPERTY: TX_ACOMP_GAIN = 5 dB

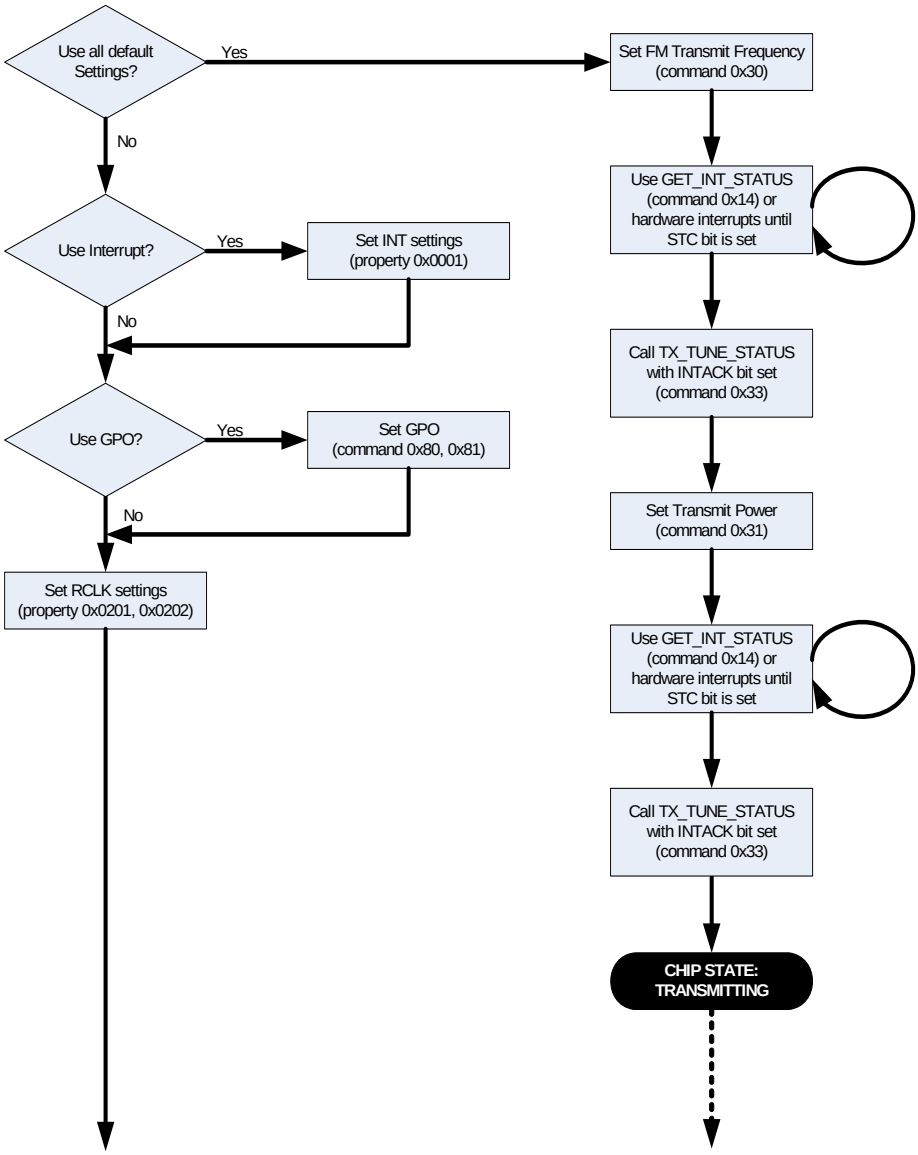
12. Programming Examples

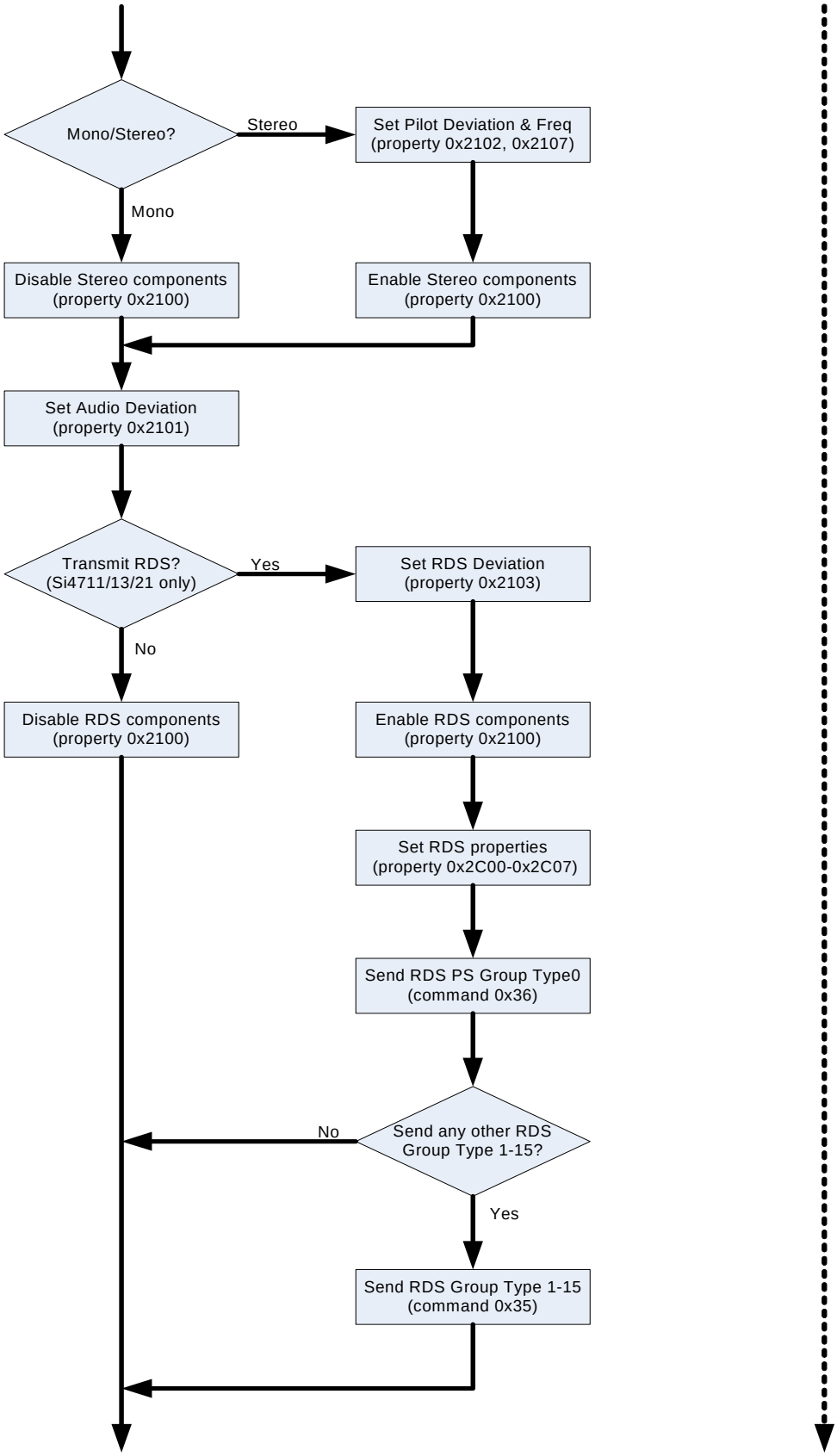
This section contains the programming example for each of the function: FM Transmit, FM Receive, AM/SW/LW Receive, and WB Receive. Before each of the example, an overview of how to program the device is shown as a flowchart. Skyworks Solutions also provides the actual software (example code) and it can be downloaded from skyworksinc.com as AN332SW.

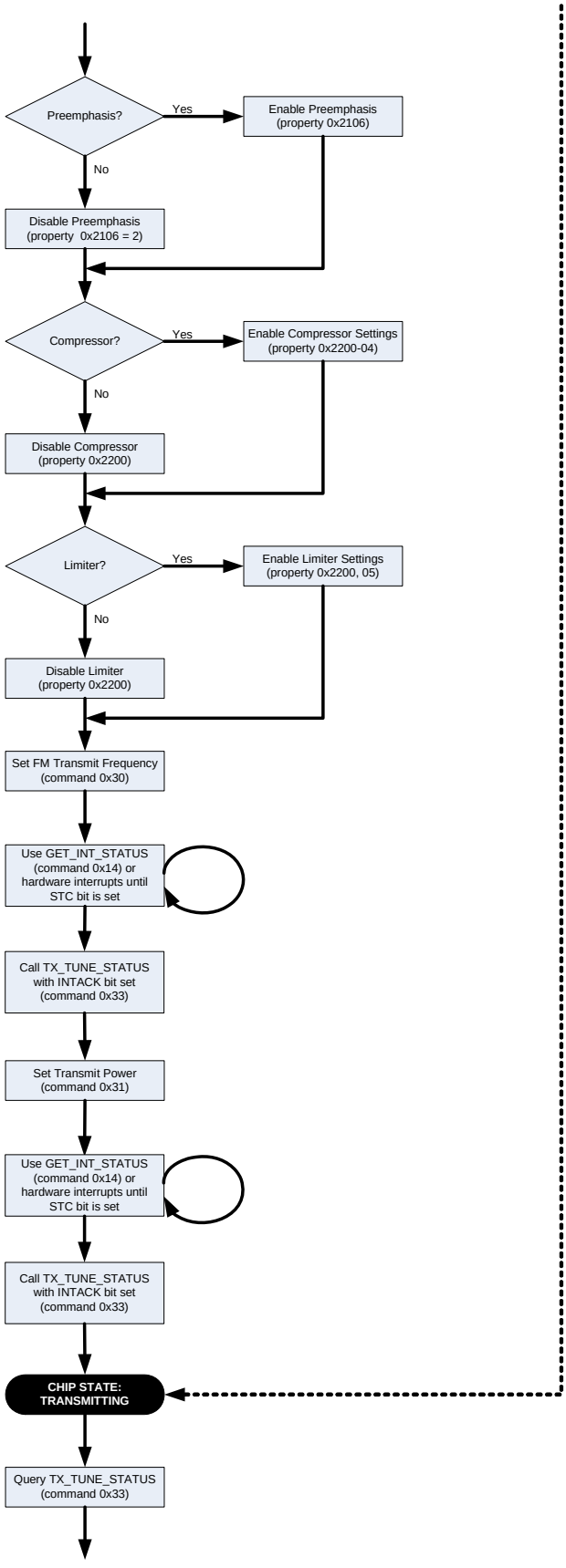
12.1. Programming Example for the FM/RDS Transmitter

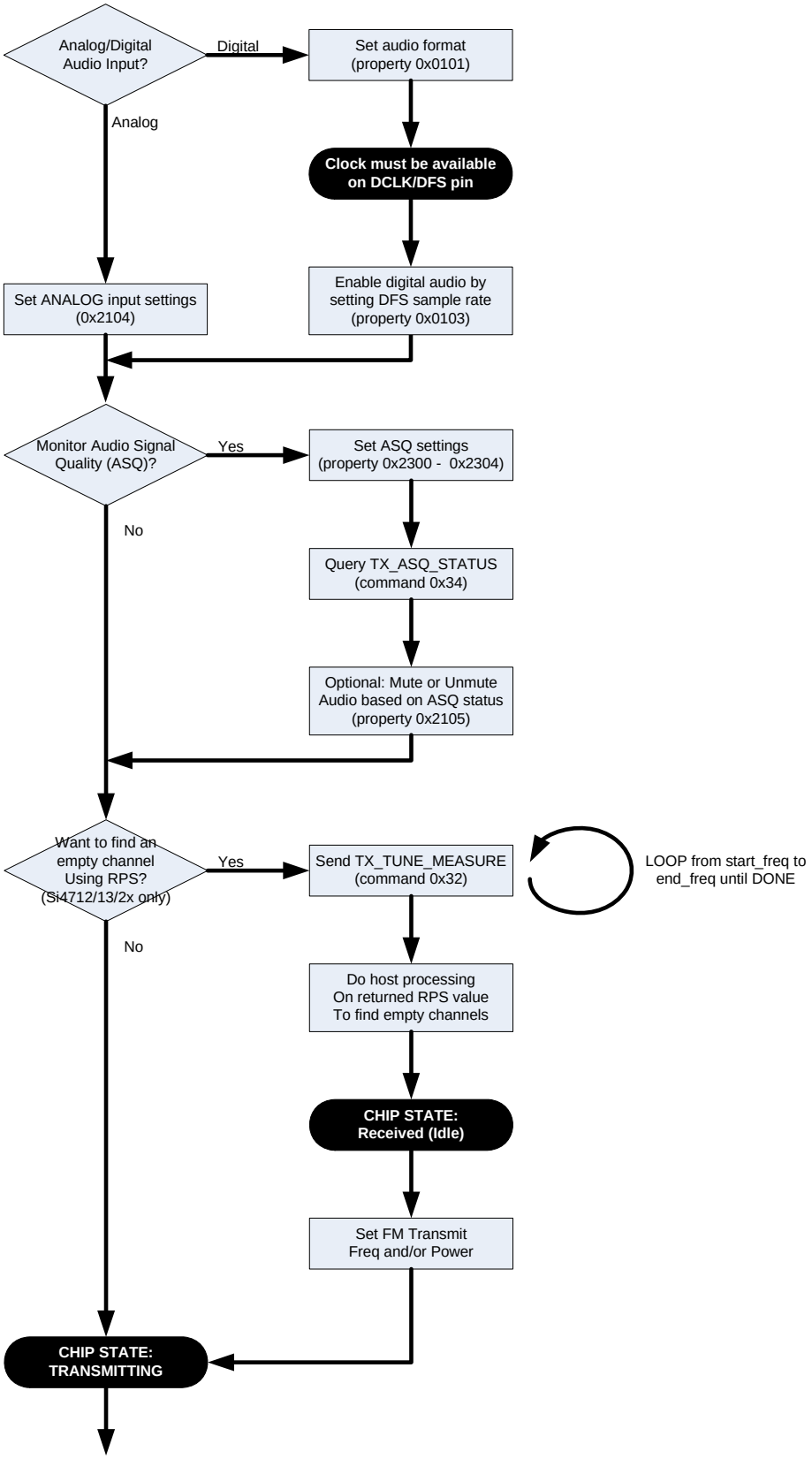
The following flowchart is an overview of how to program the FM/RDS transmitter.




Use all default Settings?
Yes
No
Use Interrupt?
Yes
Set INT settings (property 0x0001)
No
Use GPO?
Yes
Set GPO (command 0x80, 0x81)
No
Set RCLK settings (property 0x0201, 0x0202)
Set FM Transmit Frequency (command 0x30)
Use GET_INT_STATUS (command 0x14) or hardware interrupts until STC bit is set
Call TX_TUNE_STATUS with INTACK bit set (command 0x33)
Set Transmit Power (command 0x31)
Use GET_INT_STATUS (command 0x14) or hardware interrupts until STC bit is set
Call TX_TUNE_STATUS with INTACK bit set (command 0x33)
CHIP STATE: TRANSMITTING


Mono/Stereo?
Stereo
Set Pilot Deviation & Freq
(property 0x2102, 0x2107)
Mono
Disable Stereo components
(property 0x2100)
Enable Stereo components
(property 0x2100)
Set Audio Deviation
(property 0x2101)
Transmit RDS?
(Si4711/13/21 only)
Yes
Set RDS Deviation
(property 0x2103)
No
Disable RDS components
(property 0x2100)
Enable RDS components
(property 0x2100)
Set RDS properties
(property 0x2C00-0x2C07)
Send RDS PS Group Type0
(command 0x36)
No
Send any other RDS
Group Type 1-15?
Yes
Send RDS Group Type 1-15
(command 0x35)


Preemphasis?
Yes
Enable Preemphasis (property 0x2106)
No
Disable Preemphasis (property 0x2106 = 2)
Compressor?
Yes
Enable Compressor Settings (property 0x2200-04)
No
Disable Compressor (property 0x2200)
Limiter?
Yes
Enable Limiter Settings (property 0x2200, 05)
No
Disable Limiter (property 0x2200)
Set FM Transmit Frequency (command 0x30)
Use GET_INT_STATUS (command 0x14) or hardware interrupts until STC bit is set
Call TX_TUNE_STATUS with INTACK bit set (command 0x33)
Set Transmit Power (command 0x31)
Use GET_INT_STATUS (command 0x14) or hardware interrupts until STC bit is set
Call TX_TUNE_STATUS with INTACK bit set (command 0x33)
CHIP STATE: TRANSMITTING
Query TX_TUNE_STATUS (command 0x33)


Analog/Digital Audio Input?
Digital
Set audio format (property 0x0101)
Analog
Clock must be available on DCLK/DFS pin
Enable digital audio by setting DFS sample rate (property 0x0103)
Set ANALOG input settings (0x2104)
Monitor Audio Signal Quality (ASQ)?
Yes
Set ASQ settings (property 0x2300 - 0x2304)
No
Query TX_ASQ_STATUS (command 0x34)
Optional: Mute or Unmute Audio based on ASQ status (property 0x2105)
Want to find an empty channel Using RPS? (Si4712/13/2x only)
Yes
Send TX_TUNE_MEASURE (command 0x32)
LOOP from start_freq to end_freq until DONE
No
Do host processing On returned RPS value To find empty channels
CHIP STATE: Received (Idle)
Set FM Transmit Freq and/or Power
CHIP STATE: TRANSMITTING

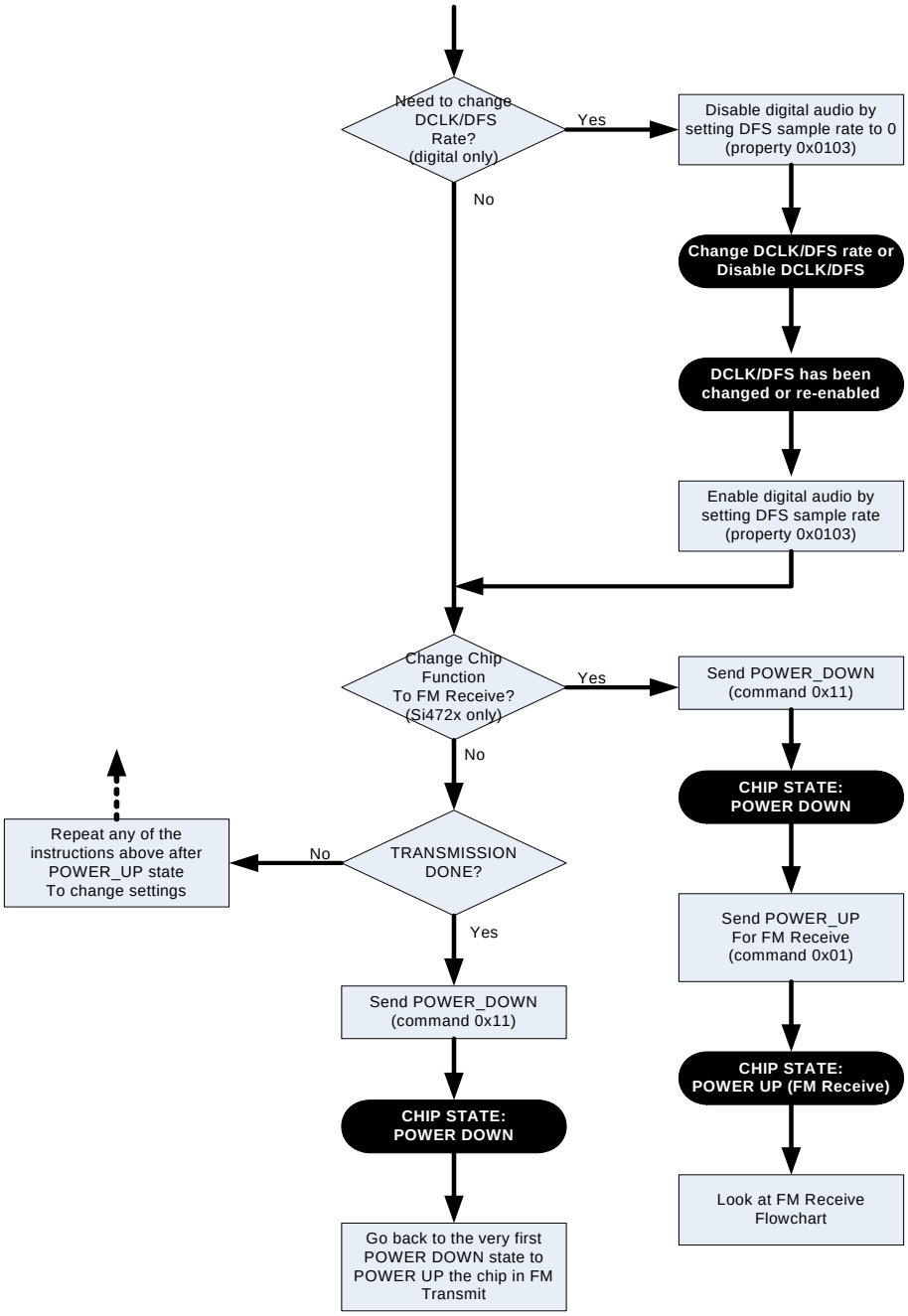


Table 55 provides an example of programming for the FM/RDS Transmitter. The table is broken into three columns. The first column lists the action taking place: command (CMD), argument (ARG), status (STATUS) or response (RESP). For SET_PROPERTY commands, the property (PROP) and property data (PROPD) are indicated. The second column lists the data byte or bytes in hexadecimal that are being sent or received. An arrow preceding the data indicates data being sent from the device to the system controller. The third column describes the action.

Note that in some cases the default properties may be acceptable and no modification is necessary. Refer to Section "5. Commands and Properties" on page 7 for a full description of each command and property.

Note: If hardware interrupts are required, the GPO2OEN flag (0x40 ARG1) must be set in the POWER_UP command.

Table 55. Programming Example for the FM/RDS Transmitter

Action	Data	Description
		Action: To power up in analog mode, go to “Powerup in Analog Mode” (bypass “Powerup in Digital Mode”).
Powerup in Digital Mode		
CMD	0x01	POWER_UP (See Table 28 for patching procedure)
ARG1	0xC2	Set to FM Transmit. Enable interrupts.
ARG2	0x0F	Set to Digital Audio Input
STATUS	→0x80	Reply Status. Clear-to-send high.
		Action: Go to “Configuration“ (bypass “Powerup in Analog Mode” section).
Powerup in Analog Mode		
CMD	0x01	POWER_UP (See Table 28 for patching procedure)
ARG1	0xC2	Set to FM Transmit. Enable interrupts.
ARG2	0x50	Set to Analog Line Input
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x21	TX_LINE_INPUT_LEVEL
ARG3 (PROP)	0x04	
ARG4 (PROPD)	0x21	Input Range = 419mV$_{PK}$, 74kΩ
ARG5 (PROPD)	0x5E	Max peak input level = 350mV$_{PK}$ = 0x15E
STATUS	→0x80	Reply Status. Clear-to-send high
Configuration		
CMD	0x10	GET_REV
ARG1	0x00	
STATUS	→0x80	Reply Status. Clear-to-send high.
RESP1	→0x0D	Part Number, HEX (0x0D = Si4713)
RESP2	→0x32	Firmware Major Rev, ASCII (0x32 = 2)
RESP3	→0x30	Firmware Minor Rev, ASCII (0x3 = 0)
RESP4	→0xE4	Patch ID MSB, example only
RESP5	→0xD6	Patch ID LSB, example only
RESP6	→0x32	Component Firmware Major Rev, ASCII (0x32 = 2)
RESP7	→0x30	Component Firmware Minor Rev, ASCII (0x30 = 0)
RESP8	→0x41	Chip Rev, ASCII (0x41 = revA)
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x00	GPO_IEN
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0x00	Set STCIEN, ERRIEN, CTSIEN
ARG5 (PROPD)	0xC1	
STATUS	→0x80	Reply Status. Clear-to-send high.

Table 55. Programming Example for the FM/RDS Transmitter (Continued)

Action	Data	Description
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x02	REFCLK_FREQ
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0x7E	REFCLK = 32500 Hz
ARG5 (PROPD)	0xF4	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x02	RCLK_PRESCALE
ARG3 (PROP)	0x02	
ARG4 (PROPD)	0x01	Divide by 400
ARG5 (PROPD)	0x90	(example RCLK = 13 MHz, REFCLK = 32500 Hz)
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x21	TX_LINE_INPUT_LEVEL_MUTE
ARG3 (PROP)	0x05	
ARG4 (PROPD)	0x00	Sets Left and Right channel mute.
ARG5 (PROPD)	0x00	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x21	TX_PREEMPHASIS
ARG3 (PROP)	0x06	
ARG4 (PROPD)	0x00	50 µs
ARG5 (PROPD)	0x01	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x21	TX_PILOT_FREQUENCY
ARG3 (PROP)	0x07	
ARG4 (PROPD)	0x4A	Sets the pilot or tone generator frequency.
ARG5 (PROPD)	0x38	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x21	TX_AUDIO_DEVIATION
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0x1A	68.25 kHz = 6825d = 0x1AA9
ARG5 (PROPD)	0xA9	
STATUS	→0x80	Reply Status. Clear-to-send high.

Table 55. Programming Example for the FM/RDS Transmitter (Continued)

Action	Data	Description
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x21	TX_PILOT_DEVIATION
ARG3 (PROP)	0x02	
ARG4 (PROPD)	0x02	6.75 kHz = 675d = 0x2A3
ARG5 (PROPD)	0xA3	
STATUS	→0x80	Reply Status. Clear-to-send high.
Tuning		
CMD	0x31	TX_TUNE_POWER
ARG1	0x00	
ARG2	0x00	Set transmit voltage to 115 dBµV = 115d = 0x73
ARG3	0x73	
ARG4	0x00	Set antenna tuning capacitor to auto.
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x30	TX_TUNE_FREQ
ARG1	0x00	
ARG2	0x27	Set frequency to 101.1 MHz = 10110d = 0x277E
ARG3	0x7E	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x14	GET_INT_STATUS
STATUS	→0x81	Reply Status. Clear-to-send high. STCINT = 1.
CMD	0x33	TX_TUNE_STATUS
ARG1	0x01	Clear STC interrupt.
STATUS	→0x80	Reply Status. Clear-to-send high.
RESP1	→0x00	
RESP2	→0x27	Frequency = 0x277E = 10110d = 101.1 MHz
RESP3	→0x7E	
RESP4	→0x00	Transmit voltage = 0x73 = 115d = 115 dBµV
RESP5	→0x73	
RESP6	→0xAB	Tuning capacitor = 191 (range = 0–191)
RESP7	→0x00	Received noise level = 0x00
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x21	TX_COMPONENT_ENABLE
ARG3 (PROP)	0x00	
ARG4 (PROPD)	0x00	Enable (Stereo) LMR and Pilot
ARG5 (PROPD)	0x03	
STATUS	→0x80	Reply Status. Clear-to-send high.
		Action: In analog mode, go to “Audio Dynamic Range Control (Compressor) and Limiter” (bypass “Input Settings in Digital Mode”).
Input Settings in Digital Mode		
		Action: Ensure that DCLK and DFS are already supplied.

Table 55. Programming Example for the FM/RDS Transmitter (Continued)

Action	Data	Description
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x01	DIGITAL_INPUT_SAMPLE_RATE
ARG3 (PROP)	0x03	
ARG4 (PROPD)	0xBB	Sample rate = 48000 Hz = 0xBB80
ARG5 (PROPD)	0x80	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x01	DIGITAL_INPUT_FORMAT
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0x00	Mode: I2S, stereo, 16bit, sample on rising edge of DCLK.
ARG5 (PROPD)	0x00	
STATUS	→0x80	Reply Status. Clear-to-send high.
		Action: The rest of the programming is the same as analog.
Audio Dynamic Range Control (Compressor) and Limiter		
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x22	TX_ACOMP_THRESHOLD
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0xFF	Threshold = –40 dBFS = 0xFFD8
ARG5 (PROPD)	0xD8	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x22	TX_ACOMP_GAIN
ARG3 (PROP)	0x04	
ARG4 (PROPD)	0x00	Gain = 15 dB = 0xF
ARG5 (PROPD)	0x0F	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x22	TX_ACOMP_RELEASE_TIME
ARG3 (PROP)	0x03	
ARG4 (PROPD)	0x00	Release time = 1000 ms = 4
ARG5 (PROPD)	0x04	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x22	TX_ACOMP_ATTACK_TIME
ARG3 (PROP)	0x02	
ARG4 (PROPD)	0x00	Attack time = 1.5 ms = 2
ARG5 (PROPD)	0x02	
STATUS	→0x80	Reply Status. Clear-to-send high.

Table 55. Programming Example for the FM/RDS Transmitter (Continued)

Action	Data	Description
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x22	TX_ACOMP_ENABLE
ARG3 (PROP)	0x00	
ARG4 (PROPD)	0x00	Enable the limiter and compressor.
ARG5 (PROPD)	0x03	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x22	TX_LIMITER_RELEASE_TIME
ARG3 (PROP)	0x05	
ARG4 (PROPD)	0x00	Sets the limiter release time to 13 (39.38 ms)
ARG5 (PROPD)	0x0D	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x23	TX_ASQ_LOW_LEVEL
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0x00	–50 dB = 0x00CE
ARG5 (PROPD)	0xCE	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x23	TX_ASQ_DURATION_LOW
ARG3 (PROP)	0x02	
ARG4 (PROPD)	0x27	10000 ms = 0x2710
ARG5 (PROPD)	0x10	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x23	TX_ASQ_HIGH_LEVEL
ARG3 (PROP)	0x03	
ARG4 (PROPD)	0x00	–20 dB = 0x00EC
ARG5 (PROPD)	0xEC	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x23	TX_ASQ_DURATION_HIGH
ARG3 (PROP)	0x04	
ARG4 (PROPD)	0x13	
ARG5 (PROPD)	0x88	5000 ms = 0x1388
STATUS	→0x80	Reply Status. Clear-to-send high.

Table 55. Programming Example for the FM/RDS Transmitter (Continued)

Action	Data	Description
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x23	TX_ASQ_INTERRUPT_SELECT
ARG3 (PROP)	0x00	
ARG4 (PROPD)	0x00	
ARG5 (PROPD)	0x07	Enable overmodulation, high and low thresholds.
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x14	GET_INT_STATUS
STATUS	→0x82	Reply Status. Clear-to-send high. ASQINT = 1. **Note**: Allow sufficient time after configuring audio thresholds before checking status. This example assumes no audio input.
CMD	0x34	TX_ASQ_STATUS
ARG1	0x01	Clear ASQINT
STATUS	→0x80	Reply Status. Clear-to-send high.
RESP1	→0x01	Low flag set.
RESP2	→0x27	Read Frequency (MSB)
RESP3	→0x7E	Read Frequency (LSB)
RESP4	→0xC9	Input Level (dBFS) = 0xC9 = –55 dB
Received Noise Level (Si4712/13/20/21 Only)		
CMD	0x32	TX_TUNE_MEASURE
ARG1	0x00	
ARG2	0x27	Set frequency to 101.1 MHz = 10110d = 0x277E
ARG3	0x7E	
ARG4	0x00	Set antenna tuning capacitor to auto.
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x14	GET_INT_STATUS
STATUS	→0x81	Reply Status. Clear-to-send high. STCINT = 1.
CMD	0x33	TX_TUNE_STATUS
ARG1	0x01	Clear STC interrupt.
STATUS	→0x80	Reply Status. Clear-to-send high.
RESP1	→0x00	
RESP2	→0x27	Frequency = 0x277E = 10110d = 101.1 MHz
RESP3	→0x7E	
RESP4	→0x00	Transmit Voltage = 0x00 = 0 dBµV (off)
RESP5	→0x00	
RESP6	→0xAB	Tuning capacitor = 191 (range = 0–191)
RESP7	→0x32	Received Noise Level = 0x32 = 50d = 50 dBµV
Tuning		
CMD	0x31	TX_TUNE_POWER
ARG1	0x00	
ARG2	0x00	Set transmit voltage to 115 dBµV = 115d = 0x73
ARG3	0x73	
ARG4	0x00	Set antenna tuning capacitor to auto.
STATUS	→0x80	Reply Status. Clear-to-send high.

Table 55. Programming Example for the FM/RDS Transmitter (Continued)

Action	Data	Description
CMD	0x30	TX_TUNE_FREQ
ARG1	0x00	
ARG2	0x27	Set frequency to 101.1 MHz = 10110d = 0x277E
ARG3	0x7E	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x14	GET_INT_STATUS
STATUS	→0x81	Reply Status. Clear-to-send high. STCINT = 1.
CMD	0x33	TX_TUNE_STATUS
ARG1	0x01	Clear STC interrupt.
STATUS	→0x80	Reply Status. Clear-to-send high.
RESP1	→0x00	
RESP2	→0x27	Frequency = 0x277E = 10110d = 101.1 MHz
RESP3	→0x7E	
RESP4	→0x00	Transmit voltage = 0x73 = 115d = 115 dBµV
RESP5	→0x73	
RESP6	→0xAB	Tuning capacitor = 191 (range = 0–191)
RESP7	→0x32	Received noise level = 0x32 (last value)
RDS (Si4711/13/21 Only)		
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x21	TX_AUDIO_DEVIATION
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0x19	66.25 kHz = 6625d = 0x19E1
ARG5 (PROPD)	0xE1	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x21	TX_RDS_DEVIATION
ARG3 (PROP)	0x03	(Si4711/13/21 Only)
ARG4 (PROPD)	0x00	2 kHz = 200d = 0xC8
ARG5 (PROPD)	0xC8	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x2C	TX_RDS_INTERRUPT_SOURCE
ARG3 (PROP)	0x00	(Si4711/13/21 Only)
ARG4 (PROPD)	0x00	RDS FIFO MT
ARG5 (PROPD)	0x01	
STATUS	→0x80	Reply Status. Clear-to-send high.

Table 55. Programming Example for the FM/RDS Transmitter (Continued)

Action	Data	Description
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x2C	TX_RDS_PI
ARG3 (PROP)	0x01	(Si4711/13/21 Only)
ARG4 (PROPD)	0x40	Sets the RDS PI Code
ARG5 (PROPD)	0xA7	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x2C	TX_RDS_PS_MIX
ARG3 (PROP)	0x02	(Si4711/13/21 Only)
ARG4 (PROPD)	0x00	Sets 50% mix of group 1A (program service) and other buffer/FIFO
ARG5 (PROPD)	0x03	groups.
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x2C	TX_RDS_PS_MISC (Default)
ARG3 (PROP)	0x03	(Si4711/13/21 Only)
ARG4 (PROPD)	0x10	Sets RDSD0 (stereo) and RDSMS (music).
ARG5 (PROPD)	0x08	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x2C	TX_RDS_PS_REPEAT_COUNT
ARG3 (PROP)	0x04	(Si4711/13/21 Only)
ARG4 (PROPD)	0x00	Sets program service repeat count to 3.
ARG5 (PROPD)	0x03	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x2C	TX_RDS_PS_MESSAGE_COUNT
ARG3 (PROP)	0x05	(Si4711/13/21 Only)
ARG4 (PROPD)	0x00	Sets PS message count to 3.
ARG5 (PROPD)	0x03	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x2C	TX_RDS_PS_AF
ARG3 (PROP)	0x06	(Si4711/13/21 Only)
ARG4 (PROPD)	0xE1	Sets alternative frequency to 87.7 MHz.
ARG5 (PROPD)	0x02	
STATUS	→0x80	Reply Status. Clear-to-send high.

Table 55. Programming Example for the FM/RDS Transmitter (Continued)

Action	Data	Description
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x2C	TX_RDS_FIFO_SIZE
ARG3 (PROP)	0x07	(Si4711/13/21 Only)
ARG4 (PROPD)	0x00	Sets FIFO size to 3 blocks (value must be one larger than fifo size).
ARG5 (PROPD)	0x04	Reply Status. Clear-to-send high.
STATUS	→0x80	
CMD	0x36	TX_RDS_PS (Si4711/13/21 Only)
ARG1	0x00	PSID = 0
ARG2	0x53	Set text “SILA”
ARG3	0x49	Complete text is
ARG4	0x4C	“SILABS SI471X RDS DEMO”
ARG5	0x41	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x36	TX_RDS_PS (Si4711/13/21 Only)
ARG1	0x01	PSID = 1
ARG2	0x42	Set text “BS”
ARG3	0x53	Complete text is
ARG4	0x20	“SILABS SI471X RDS DEMO”
ARG5	0x20	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x36	TX_RDS_PS (Si4711/13/21 Only)
ARG1	0x02	PSID = 2
ARG2	0x53	Set text “SI47”
ARG3	0x49	Complete text is
ARG4	0x34	“SILABS SI471X RDS DEMO”
ARG5	0x37	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x36	TX_RDS_PS (Si4711/13/21 Only)
ARG1	0x03	PSID = 3
ARG2	0x31	Set text “1X”
ARG3	0x58	Complete text is
ARG4	0x20	“SILABS SI471X RDS DEMO”
ARG5	0x20	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x36	TX_RDS_PS (Si4711/13/21 Only)
ARG1	0x04	PSID = 4
ARG2	0x52	Set text “RDS”
ARG3	0x44	Complete text is
ARG4	0x53	“SILABS SI471X RDS DEMO”
ARG5	0x20	
STATUS	→0x80	Reply Status. Clear-to-send high.

Table 55. Programming Example for the FM/RDS Transmitter (Continued)

Action	Data	Description
CMD	0x36	TX_RDS_PS (Si4711/13/21 Only)
ARG1	0x05	PSID = 5
ARG2	0x44	Set text “DEMO”
ARG3	0x45	Complete text is
ARG4	0x4D	“SILABS SI471X RDS DEMO”
ARG5	0x4F	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x35	TX_RDS_BUFF (Si4711/13/21 Only)
ARG1	0x06	Set LDBUFF and MTBUFF
ARG2	0x20	Set Group 2A, Text Location 0
ARG3	0x00	Set text “SILI”
ARG4	0x53	
ARG5	0x49	Complete text is
ARG6	0x4C	“Skyworks Solutions SI471X RDS DEMO”
ARG7	0x49	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x35	TX_RDS_BUFF (Si4711/13/21 Only)
ARG1	0x04	Set LDBUFF
ARG2	0x20	Set Group 2A, Text Location 1
ARG3	0x01	Set text “CON”
ARG4	0x43	
ARG5	0x4F	Complete text is
ARG6	0x4E	“Skyworks Solutions SI471X RDS DEMO”
ARG7	0x20	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x35	TX_RDS_BUFF (Si4711/13/21 Only)
ARG1	0x04	Set LDBUFF
ARG2	0x20	Set Group 2A, Text Location 2
ARG3	0x02	Set text “LABO”
ARG4	0x4C	
ARG5	0x41	Complete text is
ARG6	0x42	“Skyworks Solutions SI471X RDS DEMO”
ARG7	0x4F	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x35	TX_RDS_BUFF (Si4711/13/21 Only)
ARG1	0x04	Set LDBUFF
ARG2	0x20	Set Group 2A, Text Location 3
ARG3	0x03	Set text “RATO”
ARG4	0x52	
ARG5	0x41	Complete text is
ARG6	0x54	“Skyworks Solutions SI471X RDS DEMO”
ARG7	0x4F	
STATUS	→0x80	Reply Status. Clear-to-send high.

Table 55. Programming Example for the FM/RDS Transmitter (Continued)

Action	Data	Description
CMD	0x35	TX_RDS_BUFF (Si4711/13/21 Only)
ARG1	0x04	Set LDBUFF
ARG2	0x20	Set Group 2A, Text Location 4
ARG3	0x04	Set text “RIES”
ARG4	0x52	
ARG5	0x49	Complete text is
ARG6	0x45	“Skyworks Solutions SI471X RDS DEMO”
ARG7	0x53	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x35	TX_RDS_BUFF (Si4711/13/21 Only)
ARG1	0x04	Set LDBUFF
ARG2	0x20	Set Group 2A, Text Location 5
ARG3	0x05	Set text “SI4”
ARG4	0x20	
ARG5	0x53	Complete text is
ARG6	0x49	“Skyworks Solutions SI471X RDS DEMO”
ARG7	0x34	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x35	TX_RDS_BUFF (Si4711/13/21 Only)
ARG1	0x04	Set LDBUFF
ARG2	0x20	Set Group 2A, Text Location 6
ARG3	0x06	Set text “71X”
ARG4	0x37	
ARG5	0x31	Complete text is
ARG6	0x58	“Skyworks Solutions SI471X RDS DEMO”
ARG7	0x20	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x35	TX_RDS_BUFF (Si4711/13/21 Only)
ARG1	0x04	Set LDBUFF
ARG2	0x20	Set Group 2A, Text Location 7
ARG3	0x07	Set text “RDS”
ARG4	0x52	
ARG5	0x44	Complete text is
ARG6	0x53	“Skyworks Solutions SI471X RDS DEMO”
ARG7	0x20	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x35	TX_RDS_BUFF (Si4711/13/21 Only)
ARG1	0x04	Set LDBUFF
ARG2	0x20	Set Group 2A, Text Location 8
ARG3	0x08	Set text “DEMO”
ARG4	0x44	
ARG5	0x45	Complete text is
ARG6	0x4D	“Skyworks Solutions SI471X RDS DEMO”
ARG7	0x4F	
STATUS	→0x80	Reply Status. Clear-to-send high.

Table 55. Programming Example for the FM/RDS Transmitter (Continued)

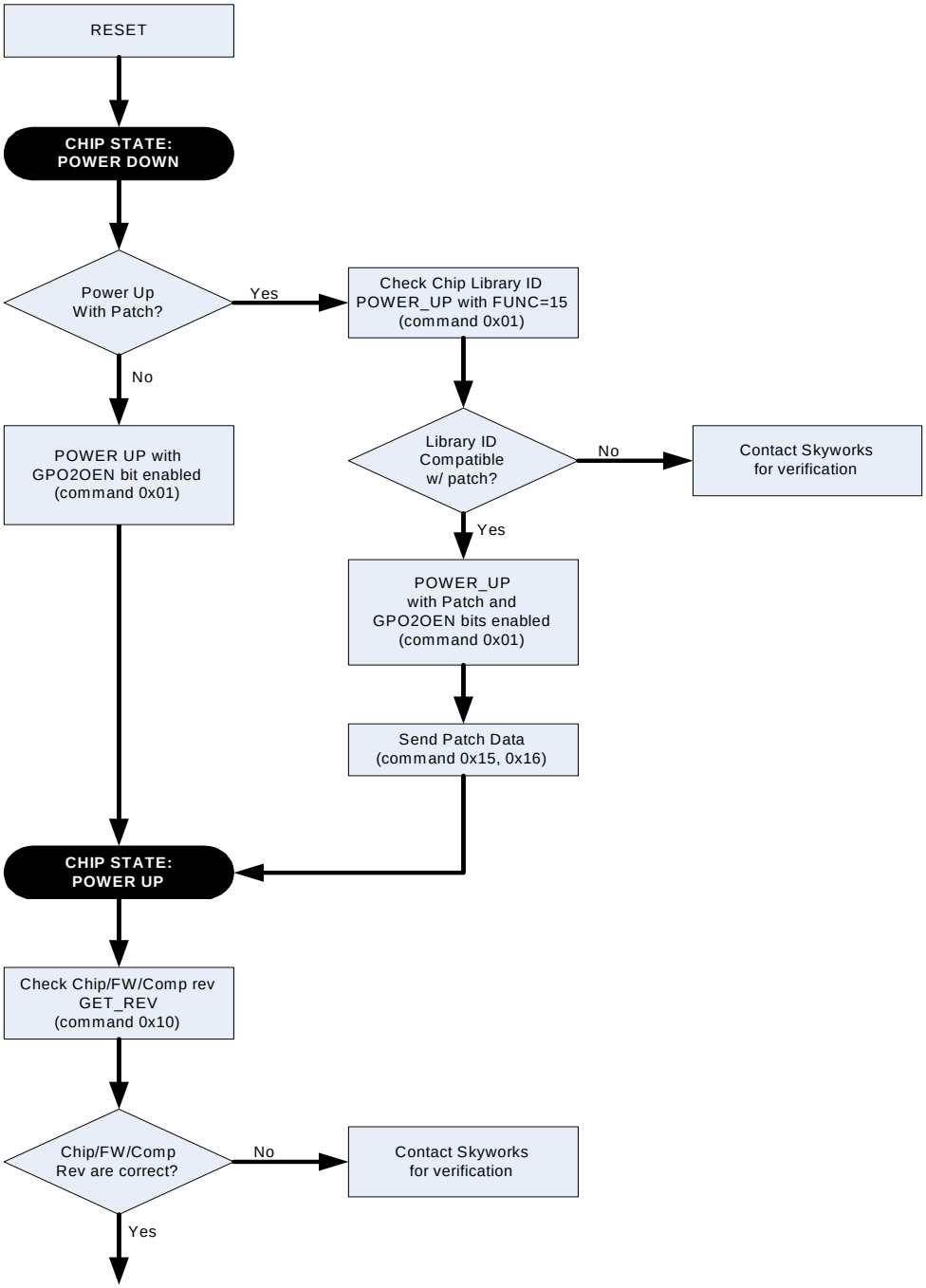
Action	Data	Description
CMD	0x35	TX_RDS_BUFF (Si4711/13/21 Only)
ARG1	0x84	Set FIFO and LDBUFF
ARG2	0x40	Set Group 4A (real time clock)
ARG3	0x01	Set time
ARG4	0xA7	Sunday 2/18/2007
ARG5	0x0B	12:53 (GMT -6:00)
ARG6	0x2D	
ARG7	0x6C	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x21	TX_COMPONENT_ENABLE
ARG3 (PROP)	0x00	(Si4711/13/21 Only)
ARG4 (PROPD)	0x00	Enable (Stereo) LMR, Pilot and RDS.
ARG5 (PROPD)	0x07	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x14	GET_INT_STATUS
STATUS	→0x84	Reply Status. Clear-to-send high. RDSINT = 1
CMD	0x35	TX_RDS_BUFF (Si4711/13/21 Only)
ARG1	0x01	Clear RDSINT
ARG2	0x00	
ARG3	0x00	
ARG4	0x00	
ARG5	0x00	
ARG6	0x00	
ARG7	0x00	
STATUS	→0x80	Reply Status. Clear-to-send high.
RESP1	→0x00	No FIFO Overflow.
RESP2	→0x5E	Circular buffer available = 94
RESP3	→0x1E	Circular buffer used = 30
RESP4	→0x03	FIFO available = 0
RESP5	→0x00	FIFO used = 3
CMD	0x11	POWER_DOWN
STATUS	→0x80	Reply Status. Clear-to-send high.

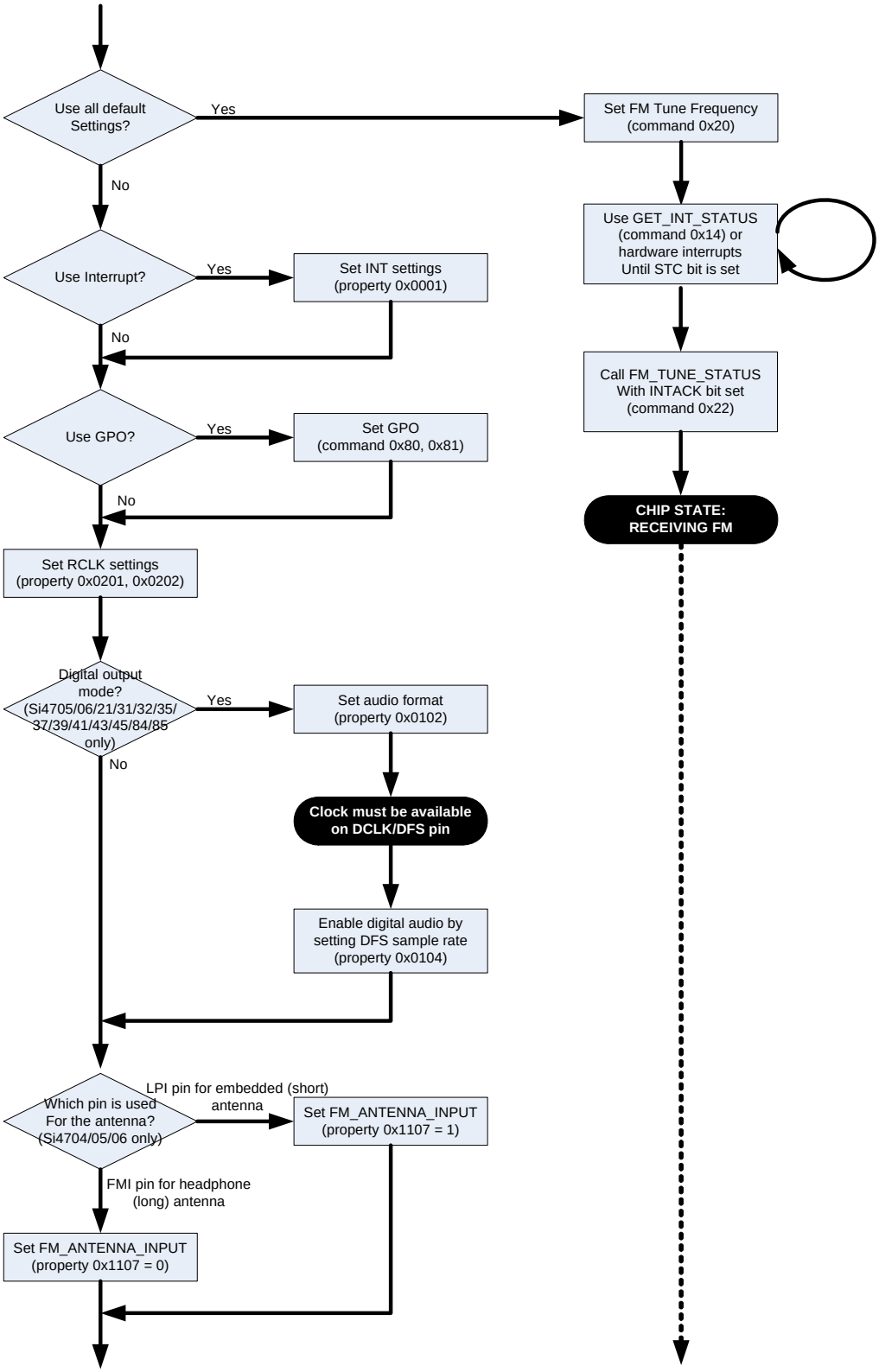
The device sets the CTS bit (and optional interrupt) to indicate that it is ready to accept the next command. The CTS bit also indicates that the POWER_UP, GET_REV, POWER_DOWN, GET_PROPERTY, GET_INT_STATUS, and TX_TUNE_STATUS commands have completed execution.

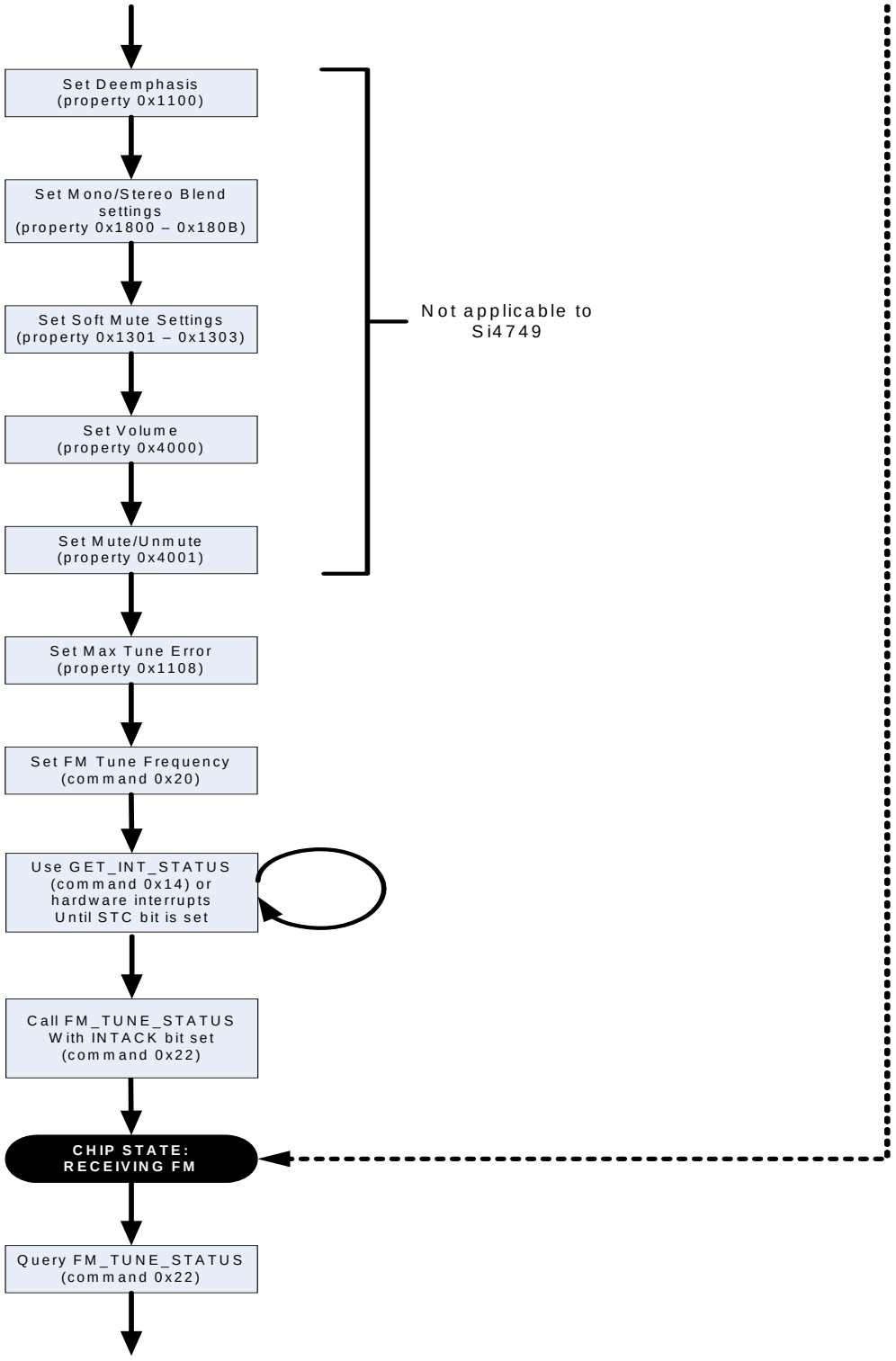
When performing a TX_TUNE_FREQ, TX_TUNE_POWER, or TX_TUNE_MEASURE CTS will indicate that the device is ready to accept the next command even though the operation is not complete. GET_INT_STATUS or hardware interrupts should be used to query for the STC bit to be set prior to performing other commands. Use TX_TUNE_STATUS to clear the STC bit after it has been set.

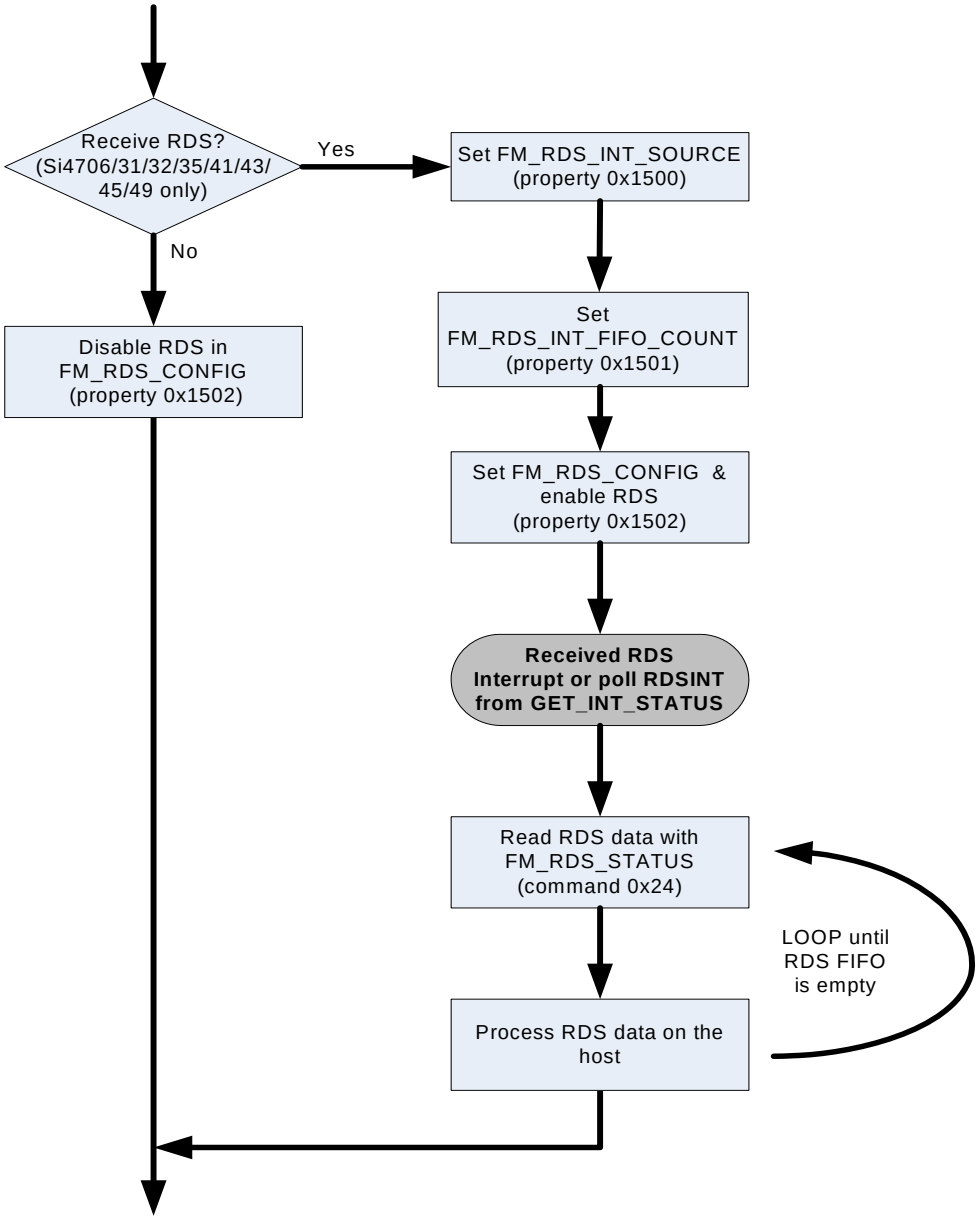
12.2. Programming Example for the FM/RDS Receiver

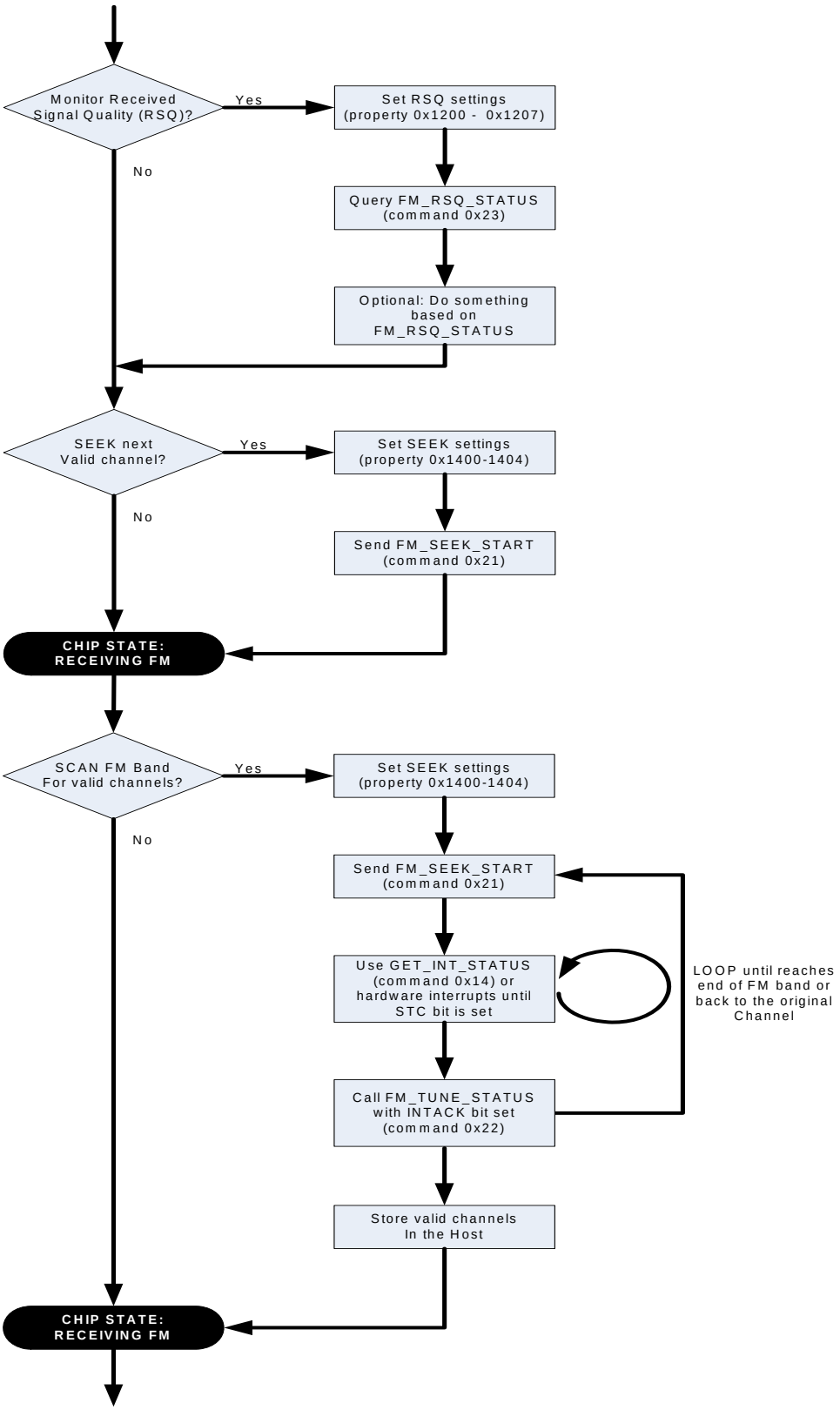
The following is a flowchart showing the overview of how to program the FM/RDS Receiver.




Use all default Settings?
Yes
Set FM Tune Frequency (command 0x20)
No
Use GET_INT_STATUS (command 0x14) or hardware interrupts Until STC bit is set
Use Interrupt?
Yes
Set INT settings (property 0x0001)
No
Call FM_TUNE_STATUS With INTACK bit set (command 0x22)
Use GPO?
Yes
Set GPO (command 0x80, 0x81)
No
CHIP STATE: RECEIVING FM
Set RCLK settings (property 0x0201, 0x0202)
Digital output mode? (Si4705/06/21/31/32/35/ 37/39/41/43/45/84/85 only)
Yes
Set audio format (property 0x0102)
No
Clock must be available on DCLK/DFS pin
Enable digital audio by setting DFS sample rate (property 0x0104)
Which pin is used For the antenna? (Si4704/05/06 only)
LPI pin for embedded (short) antenna
Set FM_ANTENNA_INPUT (property 0x1107 = 1)
FMI pin for headphone (long) antenna
Set FM_ANTENNA_INPUT (property 0x1107 = 0)


Set Deemphasis
(property 0x1100)
Set Mono/Stereo Blend
settings
(property 0x1800 – 0x180B)
Set Soft Mute Settings
(property 0x1301 – 0x1303)
Set Volume
(property 0x4000)
Set Mute/Unmute
(property 0x4001)
Not applicable to
Si4749
Set Max Tune Error
(property 0x1108)
Set FM Tune Frequency
(command 0x20)
Use GET_INT_STATUS
(command 0x14) or
hardware interrupts
Until STC bit is set
Call FM_TUNE_STATUS
With INTACK bit set
(command 0x22)
CHIP STATE:
RECEIVING FM
Query FM_TUNE_STATUS
(command 0x22)


Receive RDS?
(Si4706/31/32/35/41/43/
45/49 only)
Yes
No
Set FM_RDS_INT_SOURCE
(property 0x1500)
Set
FM_RDS_INT_FIFO_COUNT
(property 0x1501)
Set FM_RDS_CONFIG &
enable RDS
(property 0x1502)
Disable RDS in
FM_RDS_CONFIG
(property 0x1502)
Received RDS
Interrupt or poll RDSINT
from GET_INT_STATUS
Read RDS data with
FM_RDS_STATUS
(command 0x24)
LOOP until
RDS FIFO
is empty
Process RDS data on the
host


Monitor Received Signal Quality (RSQ)?
Yes
Set RSQ settings (property 0x1200 - 0x1207)
No
Query FM_RSQ_STATUS (command 0x23)
Optional: Do something based on FM_RSQ_STATUS
SEEK next Valid channel?
Yes
Set SEEK settings (property 0x1400-1404)
No
Send FM_SEEK_START (command 0x21)
CHIP STATE: RECEIVING FM
SCAN FM Band For valid channels?
Yes
Set SEEK settings (property 0x1400-1404)
No
Send FM_SEEK_START (command 0x21)
Use GET_INT_STATUS (command 0x14) or hardware interrupts until STC bit is set
LOOP until reaches end of FM band or back to the original Channel
Call FM_TUNE_STATUS with INTACK bit set (command 0x22)
Store valid channels In the Host
CHIP STATE: RECEIVING FM

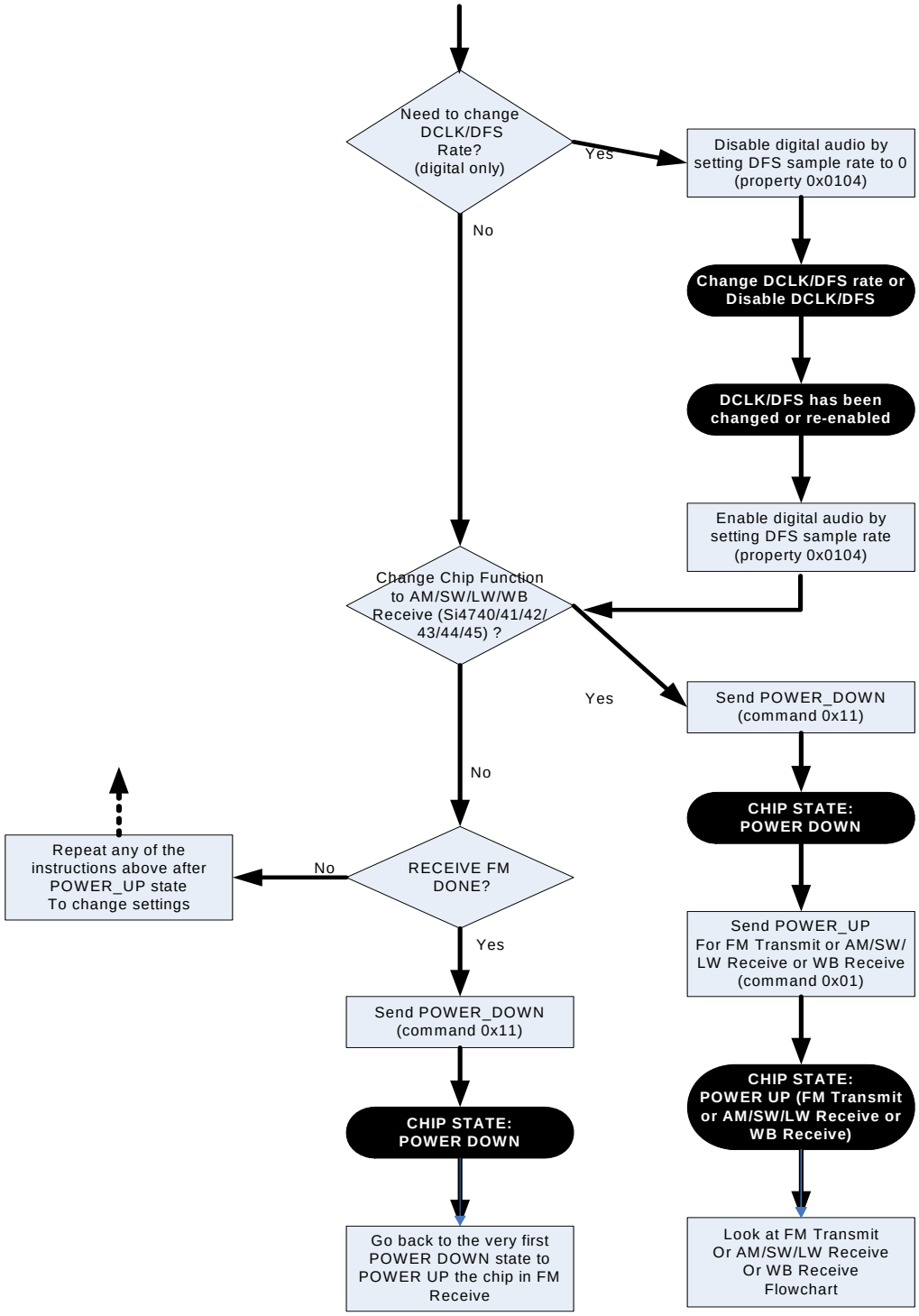

Need to change DCLK/DFS Rate? (digital only)
Yes
Disable digital audio by setting DFS sample rate to 0 (property 0x0104)
No
Change DCLK/DFS rate or Disable DCLK/DFS
DCLK/DFS has been changed or re-enabled
Enable digital audio by setting DFS sample rate (property 0x0104)
Change Chip Function to AM/SW/LW/WB Receive (Si4740/41/42/43/44/45) ?
Yes
Send POWER_DOWN (command 0x11)
No
CHIP STATE: POWER DOWN
Repeat any of the instructions above after POWER_UP state To change settings
No
RECEIVE FM DONE?
Yes
Send POWER_UP For FM Transmit or AM/SW/LW Receive or WB Receive (command 0x01)
Send POWER_DOWN (command 0x11)
CHIP STATE: POWER UP (FM Transmit or AM/SW/LW Receive or WB Receive)
CHIP STATE: POWER DOWN
Go back to the very first POWER DOWN state to POWER UP the chip in FM Receive
Look at FM Transmit Or AM/SW/LW Receive Or WB Receive Flowchart

Table 56 provides an example for the FM/RDS Receiver. The table is broken into three columns. The first column lists the action taking place: command (CMD), argument (ARG), status (STATUS) or response (RESP). For SET_PROPERTY commands, the property (PROP) and property data (PROPD) are indicated. The second column lists the data byte or bytes in hexadecimal that are being sent or received. An arrow preceding the data indicates data being sent from the device to the system controller. The third column describes the action.

In some cases the default properties may be acceptable and no modification is necessary. Refer to Section “5. Commands and Properties” for a full description of each command and property.

Table 56. Programming Example for the FM/RDS Receiver

Action	Data	Description
Powerup in Digital Mode		
CMD ARG1 ARG2 STATUS	0x01 0xC0 0xB0 →0x80	POWER_UP Set to FM Receive. Enable interrupts. Set to Digital Audio Output Reply Status. Clear-to-send high.
		Action: Ensure that DCLK and DFS are already supplied
CMD ARG1 ARG2 (PROP) ARG3 (PROP) ARG4 (PROPD) ARG5 (PROPD) STATUS	0x12 0x00 0x01 0x04 0xBB 0x80 →0x80	SET_PROPERTY DIGITAL_OUTPUT_SAMPLE_RATE Sample rate = 48000 Hz = 0xBB80 Reply Status. Clear-to-send high.
CMD ARG1 ARG2 (PROP) ARG3 (PROP) ARG4 (PROPD) ARG5 (PROPD) STATUS	0x12 0x00 0x01 0x02 0x00 0x00 →0x80	SET_PROPERTY DIGITAL_OUTPUT_FORMAT Mode: I2S, stereo, 16bit, sample on rising edge of DCLK. Reply Status. Clear-to-send high.
		Action: Go to Configuration (bypass “Powerup in analog mode” section). The rest of the programming is the same as analog.
Powerup in Analog Mode		
CMD ARG1 ARG2 STATUS	0x01 0xC0 0x05 →0x80	POWER_UP Set to FM Receive. Enable interrupts. Set to Analog Audio Output Reply Status. Clear-to-send high.
Configuration		

Table 56. Programming Example for the FM/RDS Receiver (Continued)

Action	Data	Description
CMD	0x10	GET_REV
STATUS	→0x80	Reply Status. Clear-to-send high.
RESP1	→0x1F	Part Number, HEX (0x1F = 31 dec. = Si4731)
RESP2	→0x32	Firmware Major Rev, ASCII (0x32 = 2)
RESP3	→0x30	Firmware Minor Rev, ASCII (0x30 = 0)
RESP4	→0x85	Patch ID MSB, example only
RESP5	→0xC5	Patch ID LSB, example only
RESP6	→0x32	Component Firmware Major Rev, ASCII (0x32 = 2)
RESP7	→0x30	Component Firmware Minor Rev, ASCII (0x30 = 0)
RESP8	→0x42	Chip Rev, ASCII (0x42 = revB)
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x00	GPO_IEN
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0x00	Set STCIEN, ERRIEN, CTSIEN, RSQIEN
ARG5 (PROPD)	0xC9	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x02	REFCLK_FREQ
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0x7E	REFCLK = 32500 Hz
ARG5 (PROPD)	0xF4	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x02	REFCLK_PRESCALE
ARG3 (PROP)	0x02	
ARG4 (PROPD)	0x01	Divide by 400
ARG5 (PROPD)	0x90	(example RCLK = 13 MHz, REFCLK = 32500 Hz)
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x40	RX_VOLUME
ARG3 (PROP)	0x00	
ARG4 (PROPD)	0x00	Output Volume = 63
ARG5 (PROPD)	0x3F	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x11	FM_DEEMPHASIS
ARG3 (PROP)	0x00	
ARG4 (PROPD)	0x00	50 µs
ARG5 (PROPD)	0x01	
STATUS	→0x80	Reply Status. Clear-to-send high.

Table 56. Programming Example for the FM/RDS Receiver (Continued)

Action	Data	Description
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x40	RX_HARD_MUTE
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0x00	Enable L and R audio outputs
ARG5 (PROPD)	0x00	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x18	FM_BLEND_RSSI_STEREO_THRESHOLD
ARG3 (PROP)	0x00	
ARG4 (PROPD)	0x00	Threshold = 49dB µV = 0x0031
ARG5 (PROPD)	0x31	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x18	FM_BLEND_RSSI_MONO_THRESHOLD
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0x00	Threshold = 30 dBµV = 0x001E
ARG5 (PROPD)	0x1E	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x11	FM_MAX_TUNE_ERROR
ARG3 (PROP)	0x08	
ARG4 (PROPD)	0x00	Threshold = 40 kHz = 0x0028
ARG5 (PROPD)	0x28	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x12	FM_RSQ_INT_SOURCE
ARG3 (PROP)	0x00	
ARG4 (PROPD)	0x00	Enable blend, SNR high, SNR low, RSSI high and RSSI low interrupts.
ARG5 (PROPD)	0x8F	Reply Status. Clear-to-send high.
STATUS	→0x80	
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x12	FM_RSQ_SNR_HI_THRESHOLD
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0x00	Threshold = 30 dB = 0x001E
ARG5 (PROPD)	0x1E	
STATUS	→0x80	Reply Status. Clear-to-send high.Clear-to-send high.

Table 56. Programming Example for the FM/RDS Receiver (Continued)

Action	Data	Description
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x12	FM_RSQ_SNR_LO_THRESHOLD
ARG3 (PROP)	0x02	
ARG4 (PROPD)	0x00	Threshold = 6 dB = 0x0006
ARG5 (PROPD)	0x06	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x12	FM_RSQ_RSSI_HI_THRESHOLD
ARG3 (PROP)	0x03	
ARG4 (PROPD)	0x00	Threshold = 50 dBµV = 0x0032
ARG5 (PROPD)	0x32	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x12	FM_RSQ_RSSI_LO_THRESHOLD
ARG3 (PROP)	0x04	
ARG4 (PROPD)	0x00	Threshold = 24 dBµV = 0x0018
ARG5 (PROPD)	0x18	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x12	FM_RSQ_BLEND_THRESHOLD
ARG3 (PROP)	0x07	
ARG4 (PROPD)	0x00	Pilot = 1, Threshold = 50% = 0x0032
ARG5 (PROPD)	0xB2	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x13	FM_SOFT_MUTE_MAX_ATTENUATION
ARG3 (PROP)	0x02	
ARG4 (PROPD)	0x00	Attenuation = 10 dB = 0x000A
ARG5 (PROPD)	0x0A	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x13	FM_SOFT_MUTE_SNR_THRESHOLD
ARG3 (PROP)	0x03	
ARG4 (PROPD)	0x00	Threshold = 6 dB = 0x0006
ARG5 (PROPD)	0x06	
STATUS	→0x80	Reply Status. Clear-to-send high.

Table 56. Programming Example for the FM/RDS Receiver (Continued)

Action	Data	Description
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x14	FM_SEEK_BAND_BOTTOM
ARG3 (PROP)	0x00	
ARG4 (PROPD)	0x22	Bottom Freq = 88.1 MHz = 0x226A
ARG5 (PROPD)	0x6A	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x14	FM_SEEK_BAND_TOP
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0x2A	Top Freq = 107.9 MHz = 0x2A26
ARG5 (PROPD)	0x26	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x14	FM_SEEK_FREQ_SPACING
ARG3 (PROP)	0x02	
ARG4 (PROPD)	0x00	Freq Spacing = 200 kHz = 0x0014
ARG5 (PROPD)	0x14	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x14	FM_SEEK_TUNE_SNR_THRESHOLD
ARG3 (PROP)	0x03	
ARG4 (PROPD)	0x00	Threshold = 6 dB = 0x0006
ARG5 (PROPD)	0x06	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x14	FM_SEEK_TUNE_RSSI_THRESHOLD
ARG3 (PROP)	0x04	
ARG4 (PROPD)	0x00	Threshold = 20 dBµV = 0x0014
ARG5 (PROPD)	0x14	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x20	FM_TUNE_FREQ
ARG1	0x00	
ARG2	0x27	Set frequency to 102.3 MHz = 0x27F6
ARG3	0xF6	
ARG4	0x00	Set antenna tuning capacitor to auto.
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x14	GET_INT_STATUS
STATUS	→0x81	Reply Status. Clear-to-send high. STCINT = 1.

Table 56. Programming Example for the FM/RDS Receiver (Continued)

Action	Data	Description
CMD	0x22	FM_TUNE_STATUS
ARG1	0x01	Clear STC interrupt.
STATUS	→0x80	Reply Status. Clear-to-send high.
RESP1	→0x01	Valid Frequency.
RESP2	→0x27	Frequency = 0x27F6 = 102.3 MHz
RESP3	→0xF6	
RESP4	→0x2D	RSSI = 45 dBµV
RESP5	→0x33	SNR = 51 dB
RESP6	→0x00	
RESP7	→0x00	Antenna tuning capacitor = 0 (range = 0–191)
CMD	0x23	FM_RSQ_STATUS
ARG1	0x01	Clear RSQINT
STATUS	→0x80	Reply Status. Clear-to-send high.
RESP1	→0x00	No blend, SNR high, low, RSSI high or low interrupts.
RESP2	→0x01	Soft mute is not engaged, no AFC rail, valid frequency.
RESP3	→0xD9	Pilot presence, 89% blend
RESP4	→0x2D	RSSI = 45 dBµV
RESP5	→0x33	SNR = 51 dB
RESP6	→0x00	
RESP7	→0x00	Freq offset = 0 kHz
CMD	0x21	FM_SEEK_START
ARG1	0x0C	Seek Up and Wrap.
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x14	GET_INT_STATUS
STATUS	→0x81	Reply Status. Clear-to-send high. STCINT = 1.
CMD	0x22	FM_TUNE_STATUS
ARG1	0x01	Clear STC interrupt.
STATUS	→0x80	Reply Status. Clear-to-send high.
RESP1	→0x01	Valid Frequency.
RESP2	→0x28	Frequency = 0x286E = 103.5 MHz
RESP3	→0x6E	
RESP4	→0x22	RSSI = 34 dBµV
RESP5	→0x2C	SNR = 44 dB
RESP6	→0x00	
RESP7	→0x00	Antenna tuning capacitor = 0 (range = 0–191)
RDS (Si4706/31/32/35/41/43/45/49 Only)		
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2(PROP)	0x15	FM_RDS_INT_SOURCE
ARG3(PROP)	0x00	Enable RDSRECV interrupt (set RDSINT bit when RDS has filled the
ARG4(PROPD)	0x00	FIFO by the amount set on FM_RDS_INTERRUPT_FIFO_COUNT
ARG5(PROPD)	0x01	Reply Status. Clear-to-send high
STATUS	→0x80	

Table 56. Programming Example for the FM/RDS Receiver (Continued)

Action	Data	Description
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2(PROP)	0x15	FM_RDS_INT_FIFO_COUNT
ARG3(PROP)	0x01	
ARG4(PROPD)	0x00	Set the minimum number of RDS groups stored in the RDS FIFO before RDSRECV is set
ARG5(PROPD)	0x04	
STATUS	→0x80	Reply Status. Clear-to-send high
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2(PROP)	0x15	FM_RDS_CONFIG
ARG3(PROP)	0x02	
ARG4(PROPD)	0xEF	Set Block Error A,B,C,D to 3,2,3,3
ARG5(PROPD)	0x01	Enable RDS
STATUS	→0x80	Reply Status. Clear-to-send high
CMD	0x14	GET_INT_STATUS
STATUS	→0x84	Reply Status. Clear-to-send high. RDSINT = 1
CMD	0x24	FM_RDS_STATUS
ARG1	0x01	Clear RDS interrupt.
STATUS	→0x84	Reply Status. Clear-to-send (CTS) high. RDS interrupt (RDSINT) high. Seek/Tune Complete (STCINT) high.
RESP1	→0x01	Interrupt source: RDS received.
RESP2	→0x01	RDS Synchronized. No lost data.
RESP3	→0x17	RDS FIFO Used: 0x17 = 23.
RESP4	→0x40	Block A: 0x40A7 → PI Code: 0x40A7 (KSLB).
RESP5	→0xA7	
RESP6	→0x20	Block B: 0x2000 → Group Type: 2A (Radio Text RT)
RESP7	→0x00	→ PTY: 00000b (Undefined) → Address code: 0000b = 0 (char 1,2,3,4)
RESP8	→0x53	Block C: 0x5349 →SI
RESP9	→0x49	
RESP10	→0x4C	Block D: 0x4C49 →LI
RESP11	→0x49	
RESP12	→0x00	BLE: 0 (No Error) Current RT: “SILI”

Table 56. Programming Example for the FM/RDS Receiver (Continued)

Action	Data	Description
CMD	0x24	FM_RDS_STATUS
ARG1	0x01	Clear RDS interrupt.
STATUS	→0x80	Reply Status. Clear-to-send (CTS) high. Seek/Tune Complete (STCINT) high.
RESP1	→0x01	Interrupt source: RDS received.
RESP2	→0x01	RDS Synchronized. No lost data.
RESP3	→0x16	RDS FIFO Used: 0x16 = 22.
RESP4	→0x40	Block A: 0x40A7 → PI Code: 0x40A7 (KSLB).
RESP5	→0xA7	
RESP6	→0x00	Block B: 0x000C → Group Type: 0A (Program Service PS)
RESP7	→0x0C	→ PTY: 00000b (Undefined) → Address code: 00b = 0 (char 1,2)
RESP8	→0xE1	Block C (ignored)
RESP9	→0x02	
RESP10	→0x53	Block D: 0x5349 →SI
RESP11	→0x49	
RESP12	→0x00	BLE: 0 (No Error) Current PS: “SI” Complete Scrolling PS: “SILABS RDS DEMO”
CMD	0x24	FM_RDS_STATUS
ARG1	0x01	Clear RDS interrupt.
STATUS	→0x80	Reply Status. Clear-to-send (CTS) high. Seek/Tune Complete (STCINT) high.
RESP1	→0x01	Interrupt source: RDS received.
RESP2	→0x01	RDS Synchronized. No lost data.
RESP3	→0x15	RDS FIFO Used: 0x15 = 21.
RESP4	→0x40	Block A: 0x40A7 → PI Code: 0x40A7 (KSLB).
RESP5	→0xA7	
RESP6	→0x20	Block B: 0x2001 → Group Type: 2A (Radio Text RT)
RESP7	→0x01	→ PTY: 00000b (Undefined) → Address code: 0001b = 1 (char 5,6,7,8)
RESP8	→0x43	Block C: 0x434F →CO
RESP9	→0x4F	
RESP10	→0x4E	Block D: 0x4E20 →N
RESP11	→0x20	
RESP12	→0x00	BLE: 0 (No Error) Current RT: “SILICON”

Table 56. Programming Example for the FM/RDS Receiver (Continued)

Action	Data	Description
CMD	0x24	FM_RDS_STATUS
ARG1	0x01	Clear RDS interrupt.
STATUS	→0x80	Reply Status. Clear-to-send (CTS) high. Seek/Tune Complete (STCINT) high.
RESP1	→0x01	Interrupt source: RDS received.
RESP2	→0x01	RDS Synchronized. No lost data.
RESP3	→0x15	RDS FIFO Used: 0x15 = 21 (FIFO receives another group while querying)
RESP4	→0x40	Block A: 0x40A7 → PI Code: 0x40A7 (KSLB).
RESP5	→0xA7	
RESP6	→0x00	Block B: 0x000C → Group Type: 0A (Program Service PS)
RESP7	→0x09	→ PTY: 00000b (Undefined) → Address code: 01b = 1 (char 3,4)
RESP8	→0xE1	Block C (ignored)
RESP9	→0x02	
RESP10	→0x4C	Block D: 0x4C41 →LA
RESP11	→0x41	
RESP12	→0x00	BLE: 0 (No Error) Current PS: “SILA” Complete Scrolling PS: “SILABS RDS DEMO”
CMD	0x24	FM_RDS_STATUS
ARG1	0x01	Clear RDS interrupt.
STATUS	→0x80	Reply Status. Clear-to-send (CTS) high. Seek/Tune Complete (STCINT) high.
RESP1	→0x01	Interrupt source: RDS received.
RESP2	→0x01	RDS Synchronized. No lost data.
RESP3	→0x14	RDS FIFO Used: 0x14 = 20.
RESP4	→0x40	Block A: 0x40A7 → PI Code: 0x40A7 (KSLB).
RESP5	→0xA7	
RESP6	→0x20	Block B: 0x2002 → Group Type: 2A (Radio Text RT)
RESP7	→0x02	→ PTY: 00000b (Undefined) → Address code: 0002b = 2 (char 9,10,11,12)
RESP8	→0x4C	Block C: 0x4C41 →LA
RESP9	→0x41	
RESP10	→0x42	Block D: 0x424F →BO
RESP11	→0x4F	
RESP12	→0x00	BLE: 0 (No Error) Current RT: “SILICON LABO”

Table 56. Programming Example for the FM/RDS Receiver (Continued)

Action	Data	Description
CMD	0x24	FM_RDS_STATUS
ARG1	0x01	Clear RDS interrupt.
STATUS	→0x80	Reply Status. Clear-to-send (CTS) high. Seek/Tune Complete (STCINT) high.
RESP1	→0x01	Interrupt source: RDS received.
RESP2	→0x01	RDS Synchronized. No lost data.
RESP3	→0x14	RDS FIFO Used: 0x14 = 20. (FIFO receives another group while querying)
RESP4	→0x40	Block A: 0x40A7 → PI Code: 0x40A7 (KSLB).
RESP5	→0xA7	
RESP6	→0x00	Block B: 0x000C → Group Type: 0A (Program Service PS)
RESP7	→0x0A	→ PTY: 00000b (Undefined) → Address code: 10b = 2 (char 5,6)
RESP8	→0xE1	Block C (ignored)
RESP9	→0x02	
RESP10	→0x42	Block D: 0x4253 →BS
RESP11	→0x53	
RESP12	→0x00	BLE: 0 (No Error) Current PS: “SILABS” Complete Scrolling PS: “SILABS RDS DEMO”
CMD	0x24	FM_RDS_STATUS
ARG1	0x01	Clear RDS interrupt.
STATUS	→0x80	Reply Status. Clear-to-send (CTS) high. Seek/Tune Complete (STCINT) high.
RESP1	→0x01	Interrupt source: RDS received.
RESP2	→0x01	RDS Synchronized. No lost data.
RESP3	→0x13	RDS FIFO Used: 0x13 = 19.
RESP4	→0x40	Block A: 0x40A7 → PI Code: 0x40A7 (KSLB).
RESP5	→0xA7	
RESP6	→0x20	Block B: 0x2003 → Group Type: 2A (Radio Text RT)
RESP7	→0x03	→ PTY: 00000b (Undefined) → Address code: 0003b = 3 (char 13,14,15,16)
RESP8	→0x52	Block C: 0x5241 →RA
RESP9	→0x41	
RESP10	→0x54	Block D: 0x544F →TO
RESP11	→0x4F	
RESP12	→0x00	BLE: 0 (No Error) Current RT: “SILICON LABORATO”

Table 56. Programming Example for the FM/RDS Receiver (Continued)

Action	Data	Description
CMD	0x24	FM_RDS_STATUS
ARG1	0x01	Clear RDS interrupt.
STATUS	→0x80	Reply Status. Clear-to-send (CTS) high. Seek/Tune Complete (STCINT) high.
RESP1	→0x01	Interrupt source: RDS received.
RESP2	→0x01	RDS Synchronized. No lost data.
RESP3	→0x13	RDS FIFO Used: 0x13 = 19. (FIFO receives another group while querying)
RESP4	→0x40	Block A: 0x40A7 → PI Code: 0x40A7 (KSLB).
RESP5	→0xA7	
RESP6	→0x00	Block B: 0x000C → Group Type: 0A (Program Service PS)
RESP7	→0x0B	→ PTY: 00000b (Undefined) → Address code: 11b = 3 (char 7,8)
RESP8	→0xE1	Block C (ignored)
RESP9	→0x02	
RESP10	→0x20	Block D: 0x2020 →" "
RESP11	→0x20	
RESP12	→0x00	BLE: 0 (No Error) Current PS: "SILABS" Complete Scrolling PS: "SILABS RDS DEMO"
CMD	0x24	FM_RDS_STATUS
ARG1	0x01	Clear RDS interrupt.
STATUS	→0x80	Reply Status. Clear-to-send (CTS) high. Seek/Tune Complete (STCINT) high.
RESP1	→0x01	Interrupt source: RDS received.
RESP2	→0x01	RDS Synchronized. No lost data.
RESP3	→0x12	RDS FIFO Used: 0x12 = 18.
RESP4	→0x40	Block A: 0x40A7 → PI Code: 0x40A7 (KSLB).
RESP5	→0xA7	
RESP6	→0x20	Block B: 0x2004 → Group Type: 2A (Radio Text RT)
RESP7	→0x04	→ PTY: 00000b (Undefined) → Address code: 0004b = 4 (char 17,18,19,20)
RESP8	→0x52	Block C: 0x5249 →RI
RESP9	→0x49	
RESP10	→0x45	Block D: 0x4553 →ES
RESP11	→0x53	
RESP12	→0x00	BLE: 0 (No Error) Current RT: "Skyworks Solutions"

Table 56. Programming Example for the FM/RDS Receiver (Continued)

Action	Data	Description
CMD	0x24	FM_RDS_STATUS
ARG1	0x01	Clear RDS interrupt.
STATUS	→0x80	Reply Status. Clear-to-send (CTS) high. Seek/Tune Complete (STCINT) high.
RESP1	→0x01	Interrupt source: RDS received.
RESP2	→0x01	RDS Synchronized. No lost data.
RESP3	→0x12	RDS FIFO Used: 0x12 = 18. (FIFO receives another group while querying)
RESP4	→0x40	Block A: 0x40A7 → PI Code: 0x40A7 (KSLB).
RESP5	→0xA7	
RESP6	→0x00	Block B: 0x000C → Group Type: 0A (Program Service PS)
RESP7	→0x0C	→ PTY: 00000b (Undefined) → Address code: 00b = 0 (char 1,2)
RESP8	→0xE1	Block C (ignored)
RESP9	→0x02	
RESP10	→0x52	Block D: 0x5244 →RD
RESP11	→0x44	
RESP12	→0x00	BLE: 0 (No Error) Current PS: “RDLABS Scrolling PS: “SILABS RDS DEMO”
CMD	0x24	FM_RDS_STATUS
ARG1	0x01	Clear RDS interrupt.
STATUS	→0x80	Reply Status. Clear-to-send (CTS) high. Seek/Tune Complete (STCINT) high.
RESP1	→0x01	Interrupt source: RDS received.
RESP2	→0x01	RDS Synchronized. No lost data.
RESP3	→0x11	RDS FIFO Used: 0x11 = 17.
RESP4	→0x40	Block A: 0x40A7 → PI Code: 0x40A7 (KSLB).
RESP5	→0xA7	
RESP6	→0x20	Block B: 0x2005 → Group Type: 2A (Radio Text RT)
RESP7	→0x05	→ PTY: 00000b (Undefined) → Address code: 0005b = 5 (char 21,22,23,24)
RESP8	→0x20	Block C: 0x2053 → S
RESP9	→0x53	
RESP10	→0x49	Block D: 0x4934 →I4
RESP11	→0x34	
RESP12	→0x00	BLE: 0 (No Error) Current RT: “Skyworks Solutions SI4”

Table 56. Programming Example for the FM/RDS Receiver (Continued)

Action	Data	Description
CMD	0x24	FM_RDS_STATUS
ARG1	0x01	Clear RDS interrupt.
STATUS	→0x80	Reply Status. Clear-to-send (CTS) high. Seek/Tune Complete (STCINT) high.
RESP1	→0x01	Interrupt source: RDS received.
RESP2	→0x01	RDS Synchronized. No lost data.
RESP3	→0x10	RDS FIFO Used: 0x10 = 16.
RESP4	→0x40	Block A: 0x40A7 → PI Code: 0x40A7 (KSLB).
RESP5	→0xA7	
RESP6	→0x00	Block B: 0x000C → Group Type: 0A (Program Service PS)
RESP7	→0x09	→ PTY: 00000b (Undefined) → Address code: 01b = 1 (char 3,4)
RESP8	→0xE1	Block C (ignored)
RESP9	→0x02	
RESP10	→0x53	Block D: 0x5320 →S
RESP11	→0x20	
RESP12	→0x00	BLE: 0 (No Error) Current PS: “RDS BS” Complete Scrolling PS: “SILABS RDS DEMO”
CMD	0x24	FM_RDS_STATUS
ARG1	0x01	Clear RDS interrupt.
STATUS	→0x80	Reply Status. Clear-to-send (CTS) high. Seek/Tune Complete (STCINT) high.
RESP1	→0x01	Interrupt source: RDS received.
RESP2	→0x01	RDS Synchronized. No lost data.
RESP3	→0x0F	RDS FIFO Used: 0x0F = 15.
RESP4	→0x40	Block A: 0x40A7 → PI Code: 0x40A7 (KSLB).
RESP5	→0xA7	
RESP6	→0x20	Block B: 0x2006 → Group Type: 2A (Radio Text RT)
RESP7	→0x06	→ PTY: 00000b (Undefined) → Address code: 0006b = 6 (char 25, 26, 27, 28)
RESP8	→0x37	Block C: 0x3731 →71
RESP9	→0x31	
RESP10	→0x58	Block D: 0x5820 →x
RESP11	→0x20	
RESP12	→0x00	BLE: 0 (No Error) Current RT: “Skyworks Solutions SI471x ”

Table 56. Programming Example for the FM/RDS Receiver (Continued)

Action	Data	Description
CMD	0x24	FM_RDS_STATUS
ARG1	0x01	Clear RDS interrupt.
STATUS	→0x80	Reply Status. Clear-to-send (CTS) high. Seek/Tune Complete (STCINT) high.
RESP1	→0x01	Interrupt source: RDS received.
RESP2	→0x01	RDS Synchronized. No lost data.
RESP3	→0x0E	RDS FIFO Used: 0x0E = 14.
RESP4	→0x40	Block A: 0x40A7 → PI Code: 0x40A7 (KSLB).
RESP5	→0xA7	
RESP6	→0x00	Block B: 0x000A → Group Type: 0A (Program Service PS)
RESP7	→0x0A	→ PTY: 00000b (Undefined) → Address code: 10b = 2 (char 5, 6)
RESP8	→0xE1	Block C (ignored)
RESP9	→0x02	
RESP10	→0x44	Block D: 0x4445 →DE
RESP11	→0x45	
RESP12	→0x00	BLE: 0 (No Error) Current PS: “RDS DE” Complete Scrolling PS: “SILABS RDS DEMO”
CMD	0x24	FM_RDS_STATUS
ARG1	0x01	Clear RDS interrupt.
STATUS	→0x80	Reply Status. Clear-to-send (CTS) high. Seek/Tune Complete (STCINT) high.
RESP1	→0x01	Interrupt source: RDS received.
RESP2	→0x01	RDS Synchronized. No lost data.
RESP3	→0x0E	RDS FIFO Used: 0x0E = 14. (FIFO receives another group while querying)
RESP4	→0x40	Block A: 0x40A7 → PI Code: 0x40A7 (KSLB).
RESP5	→0xA7	
RESP6	→0x20	Block B: 0x2007 → Group Type: 2A (Radio Text RT)
RESP7	→0x07	→ PTY: 00000b (Undefined) → Address code: 0007b = 7 (char 29,30,31,32)
RESP8	→0x52	Block C: 0x5244 →RD
RESP9	→0x44	
RESP10	→0x53	Block D: 0x5320 →S
RESP11	→0x20	
RESP12	→0x00	BLE: 0 (No Error) Current RT: “Skyworks Solutions SI471x RDS”

Table 56. Programming Example for the FM/RDS Receiver (Continued)

Action	Data	Description
CMD	0x24	FM_RDS_STATUS
ARG1	0x01	Clear RDS interrupt.
STATUS	→0x80	Reply Status. Clear-to-send (CTS) high. Seek/Tune Complete (STCINT) high.
RESP1	→0x01	Interrupt source: RDS received.
RESP2	→0x01	RDS Synchronized. No lost data.
RESP3	→0x0D	RDS FIFO Used: 0x0D = 13.
RESP4	→0x40	Block A: 0x40A7 → PI Code: 0x40A7 (KSLB).
RESP5	→0xA7	
RESP6	→0x00	Block B: 0x000C → Group Type: 0A (Program Service PS)
RESP7	→0x0B	→ PTY: 00000b (Undefined) → Address code: 11b = 3 (char 7,8)
RESP8	→0xE1	Block C (ignored)
RESP9	→0x02	
RESP10	→0x4D	Block D: 0x4D4F →MO
RESP11	→0x4F	
RESP12	→0x00	BLE: 0 (No Error) Current PS: “RDS DEMO” Complete Scrolling PS: “SILABS RDS DEMO”
CMD	0x24	FM_RDS_STATUS
ARG1	0x01	Clear RDS interrupt.
+STATUS	→0x80	Reply Status. Clear-to-send (CTS) high. Seek/Tune Complete (STCINT) high.
RESP1	→0x01	Interrupt source: RDS received.
RESP2	→0x01	RDS Synchronized. No lost data.
RESP3	→0x0D	RDS FIFO Used: 0x0D = 13. (FIFO receives another group while querying)
RESP4	→0x40	Block A: 0x40A7 → PI Code: 0x40A7 (KSLB).
RESP5	→0xA7	
RESP6	→0x20	Block B: 0x2008 → Group Type: 2A (Radio Text RT)
RESP7	→0x08	→ PTY: 00000b (Undefined) → Address code: 0008b = 8 (char 33,34,35,36)
RESP8	→0x44	Block C: 0x4445 →DE
RESP9	→0x45	
RESP10	→0x4D	Block D: 0x4D4F →MO
RESP11	→0x4F	
RESP12	→0x00	BLE: 0 (No Error) Current RT: “Skyworks Solutions SI471x RDS DEMO”

Table 56. Programming Example for the FM/RDS Receiver (Continued)

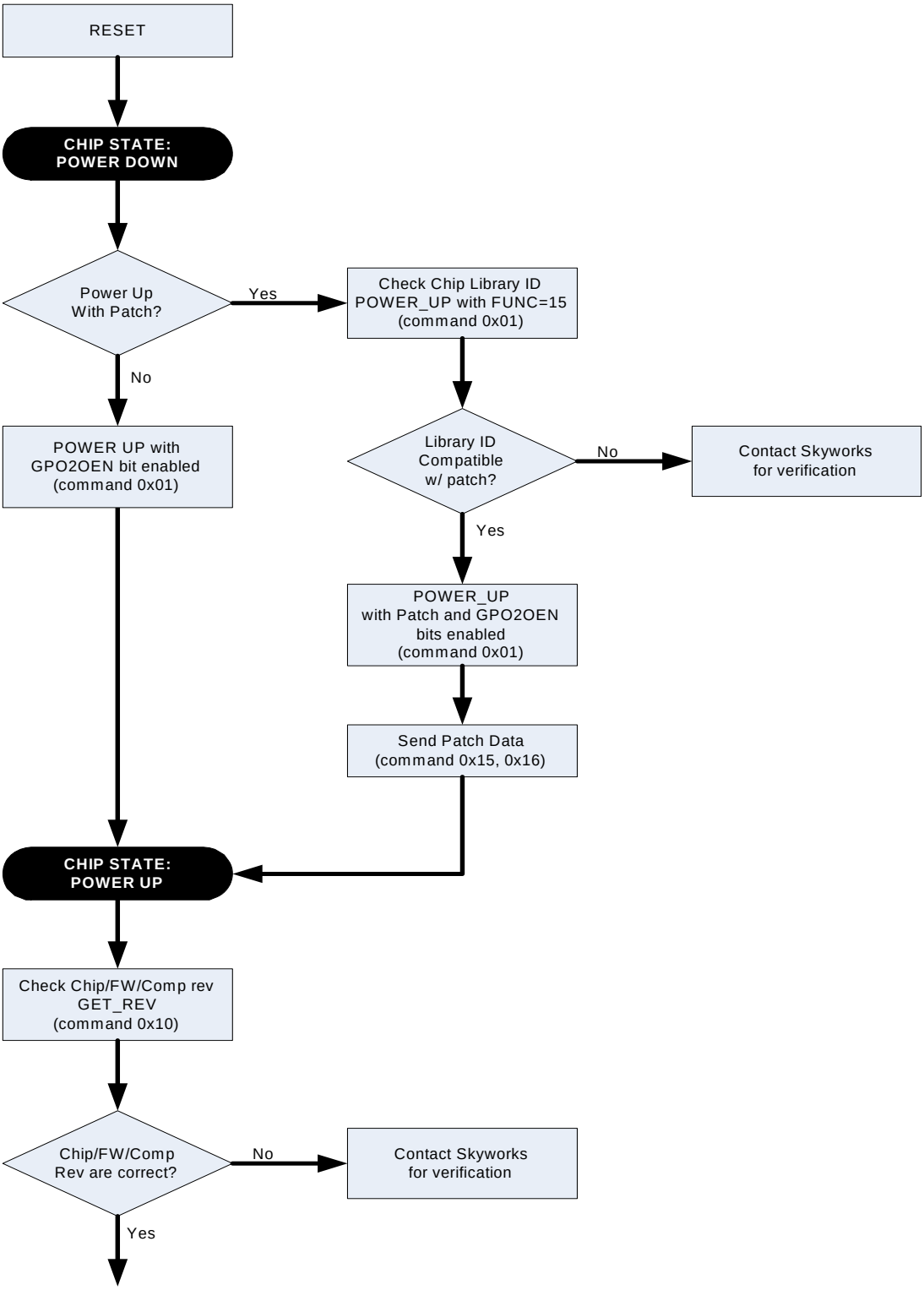
Action	Data	Description
CMD	0x24	FM_RDS_STATUS
ARG1	0x01	Clear RDS interrupt.
STATUS	→0x80	Reply Status. Clear-to-send (CTS) high. Seek/Tune Complete (STCINT) high.
RESP1	→0x01	Interrupt source: RDS received.
RESP2	→0x01	RDS Synchronized. No lost data.
RESP3	→0x0C	RDS FIFO Used: 0x0C = 12.
RESP4	→0x40	Block A: 0x40A7 → PI Code: 0x40A7 (KSLB).
RESP5	→0xA7	
RESP6	→0x00	Block B: 0x000C → Group Type: 0A (Program Service PS)
RESP7	→0x0C	→ PTY: 00000b (Undefined) → Address code: 00b = 0 (char 1,2)
RESP8	→0xE1	Block C (ignored)
RESP9	→0x02	
RESP10	→0x53	Block D: 0x5349 →SI
RESP11	→0x49	
RESP12	→0x00	BLE: 0 (No Error) Current PS: “SIS_DEMO” Complete Scrolling PS: “SILABS RDS DEMO”
CMD	0x24	FM_RDS_STATUS
ARG1	0x01	Clear RDS interrupt.
STATUS	→0x80	Reply Status. Clear-to-send (CTS) high. Seek/Tune Complete (STCINT) high.
RESP1	→0x01	Interrupt source: RDS received.
RESP2	→0x01	RDS Synchronized. No lost data.
RESP3	→0x0D	RDS FIFO Used: 0x0C = 12. (FIFO receives another group while querying)
RESP4	→0x40	Block A: 0x40A7 → PI Code: 0x40A7 (KSLB).
RESP5	→0xA7	
RESP6	→0x20	Block B: 0x2009 → Group Type: 2A (Radio Text RT)
RESP7	→0x09	→ PTY: 00000b (Undefined) → Address code: 0009b = 9 (char 37,38,39,40)
RESP8	→0x0D	Block C: 0x0D00 → ‘RET’ ‘NUL’ (end of RT)
RESP9	→0x00	
RESP10	→0x00	Block D: 0x0000 → ‘NUL’ ‘NUL’
RESP11	→0x00	
RESP12	→0x00	BLE: 0 (No Error) Current RT: “Skyworks Solutions SI471x RDS DEMO”
		- continue sending FM_RDS_STATUS until FIFO empty -
CMD	0x11	POWER_DOWN
STATUS	→0x80	Reply Status. Clear-to-send high.

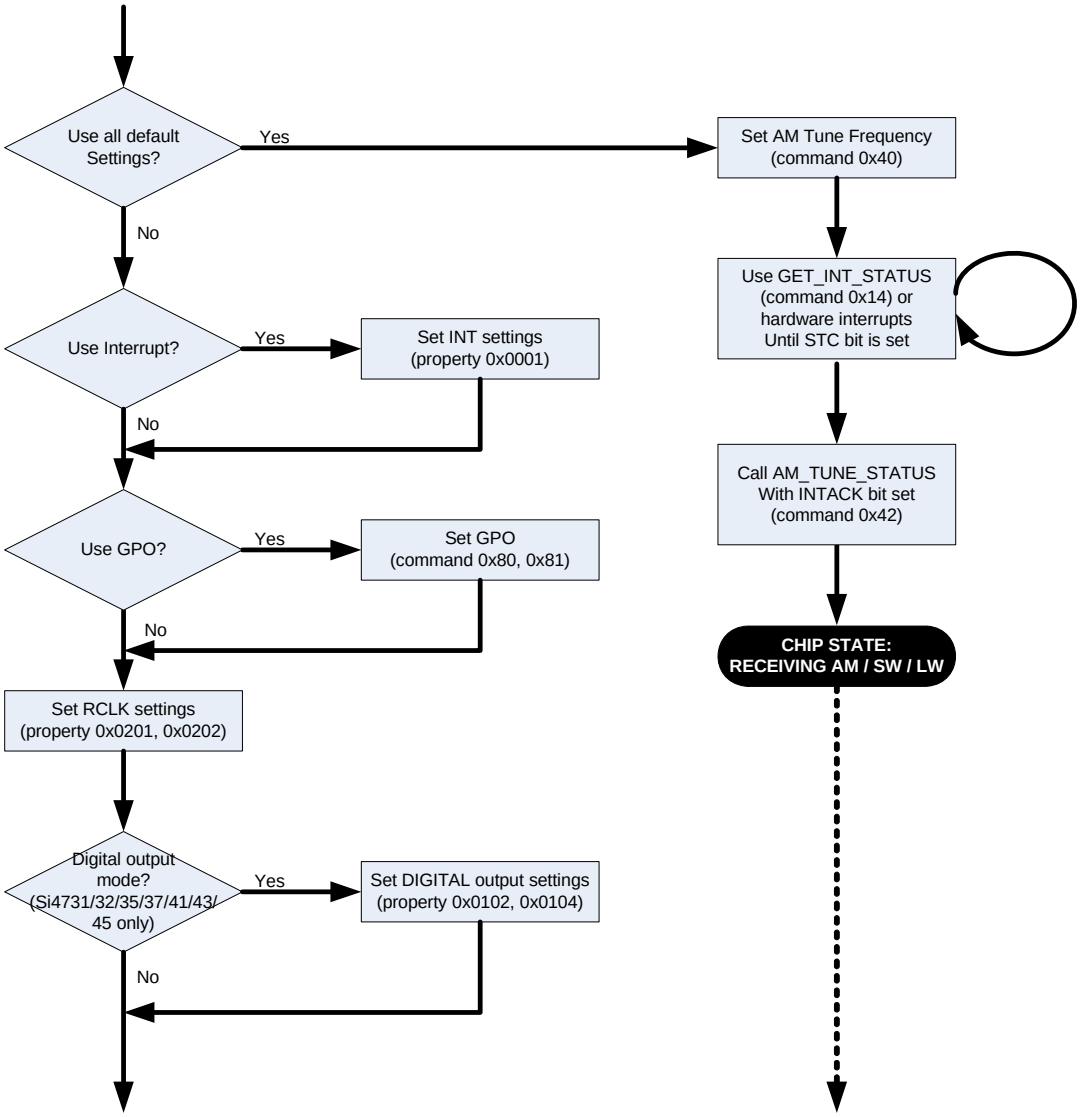
The device sets the CTS bit (and optional interrupt) to indicate that it is ready to accept the next command. The CTS bit also indicates that the POWER_UP, GET_REV, POWER_DOWN, GET_PROPERTY, GET_INT_STATUS, FM_TUNE_STATUS, and FM_RSQ_STATUS commands have completed execution.

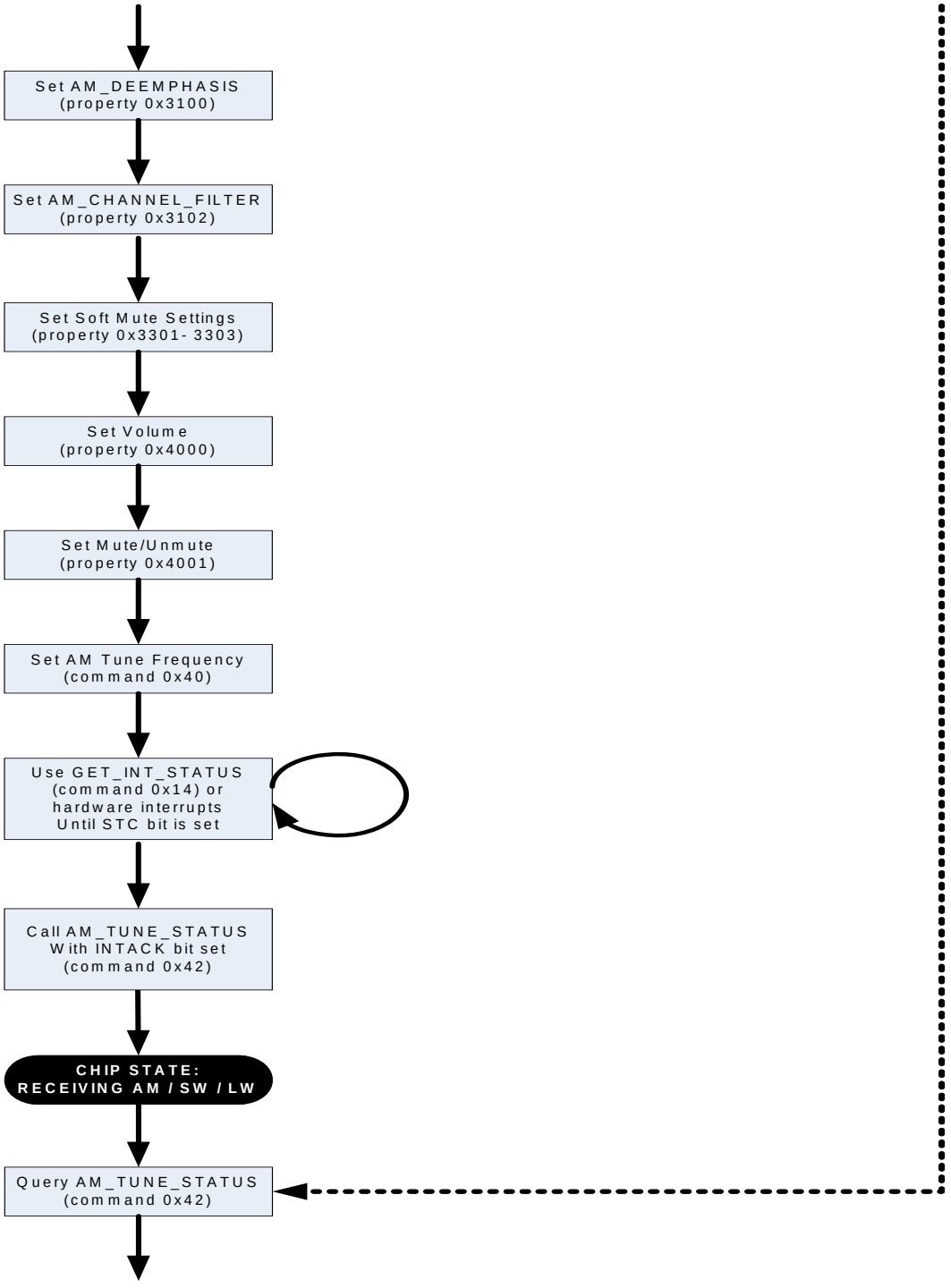
When performing a FM_TUNE_FREQ or FM_SEEK_START CTS will indicate that the device is ready to accept the next command even though the operation is not complete. GET_INT_STATUS or hardware interrupts should be used to query for the STC bit to be set prior to performing other commands. Use FM_TUNE_STATUS to clear the STC bit after it has been set.

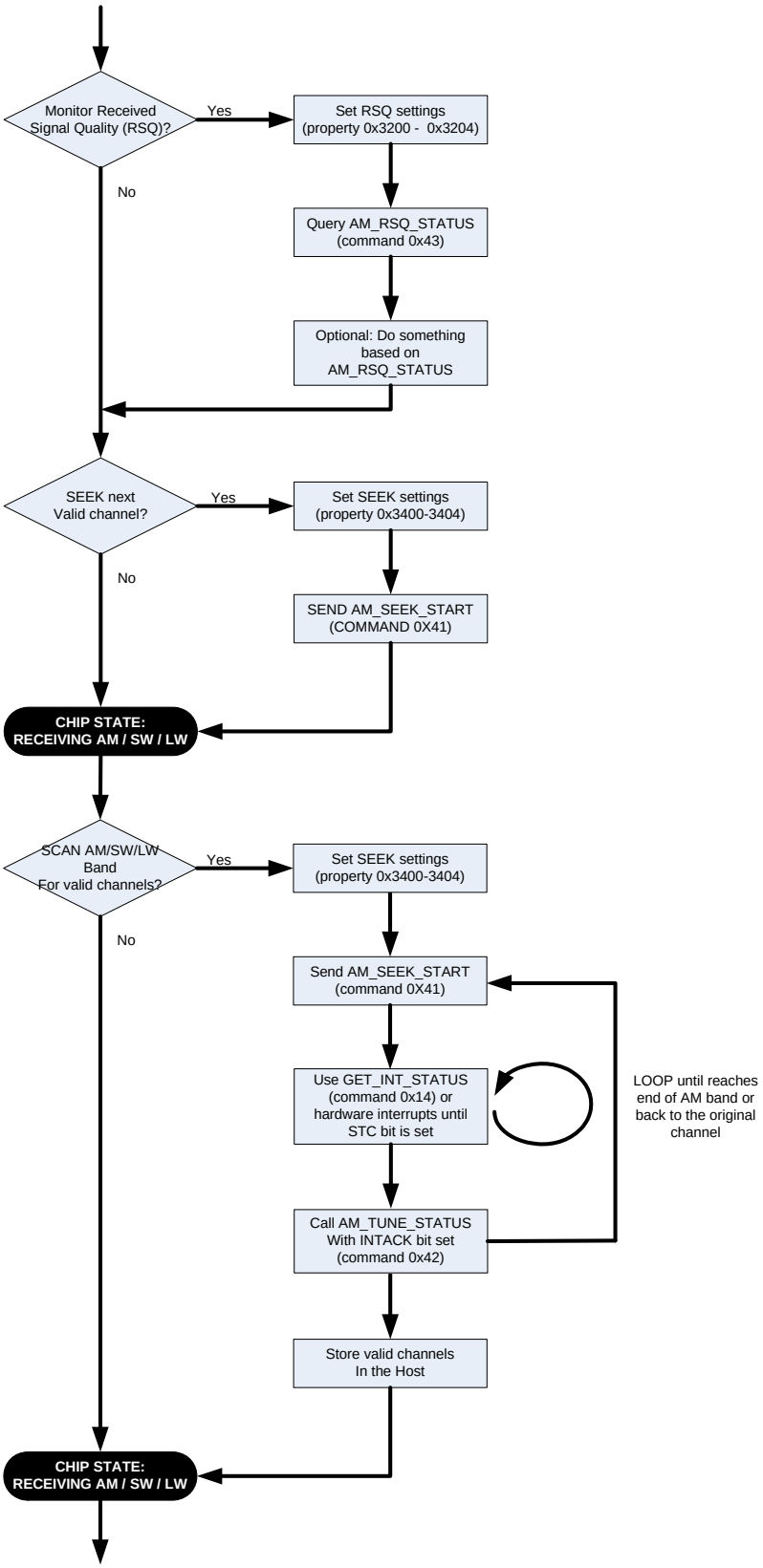
12.3. Programming Example for the AM/LW/SW Receiver

The following flowchart shows an overview of how to program the AM/LW/SW receiver.




Use all default Settings?
Yes
Set AM Tune Frequency (command 0x40)
No
Use GET_INT_STATUS (command 0x14) or hardware interrupts Until STC bit is set
Use Interrupt?
Yes
Set INT settings (property 0x0001)
No
Call AM_TUNE_STATUS With INTACK bit set (command 0x42)
Use GPO?
Yes
Set GPO (command 0x80, 0x81)
No
CHIP STATE: RECEIVING AM / SW / LW
Set RCLK settings (property 0x0201, 0x0202)
Digital output mode? (Si4731/32/35/37/41/43/45 only)
Yes
Set DIGITAL output settings (property 0x0102, 0x0104)
No


Set AM_DEEMPHASIS
(property 0x3100)
Set AM_CHANNEL_FILTER
(property 0x3102)
Set Soft Mute Settings
(property 0x3301- 3303)
Set Volume
(property 0x4000)
Set Mute/Unmute
(property 0x4001)
Set AM Tune Frequency
(command 0x40)
Use GET_INT_STATUS
(command 0x14) or
hardware interrupts
Until STC bit is set
Call AM_TUNE_STATUS
With INTACK bit set
(command 0x42)
CHIP STATE:
RECEIVING AM / SW / LW
Query AM_TUNE_STATUS
(command 0x42)


Monitor Received Signal Quality (RSQ)?
Yes
Set RSQ settings (property 0x3200 - 0x3204)
No
Query AM_RSQ_STATUS (command 0x43)
Optional: Do something based on AM_RSQ_STATUS
SEEK next Valid channel?
Yes
Set SEEK settings (property 0x3400-3404)
No
SEND AM_SEEK_START (COMMAND 0X41)
CHIP STATE: RECEIVING AM / SW / LW
SCAN AM/SW/LW Band For valid channels?
Yes
Set SEEK settings (property 0x3400-3404)
No
Send AM_SEEK_START (command 0X41)
Use GET_INT_STATUS (command 0x14) or hardware interrupts until STC bit is set
LOOP until reaches end of AM band or back to the original channel
Call AM_TUNE_STATUS With INTACK bit set (command 0x42)
Store valid channels In the Host
CHIP STATE: RECEIVING AM / SW / LW

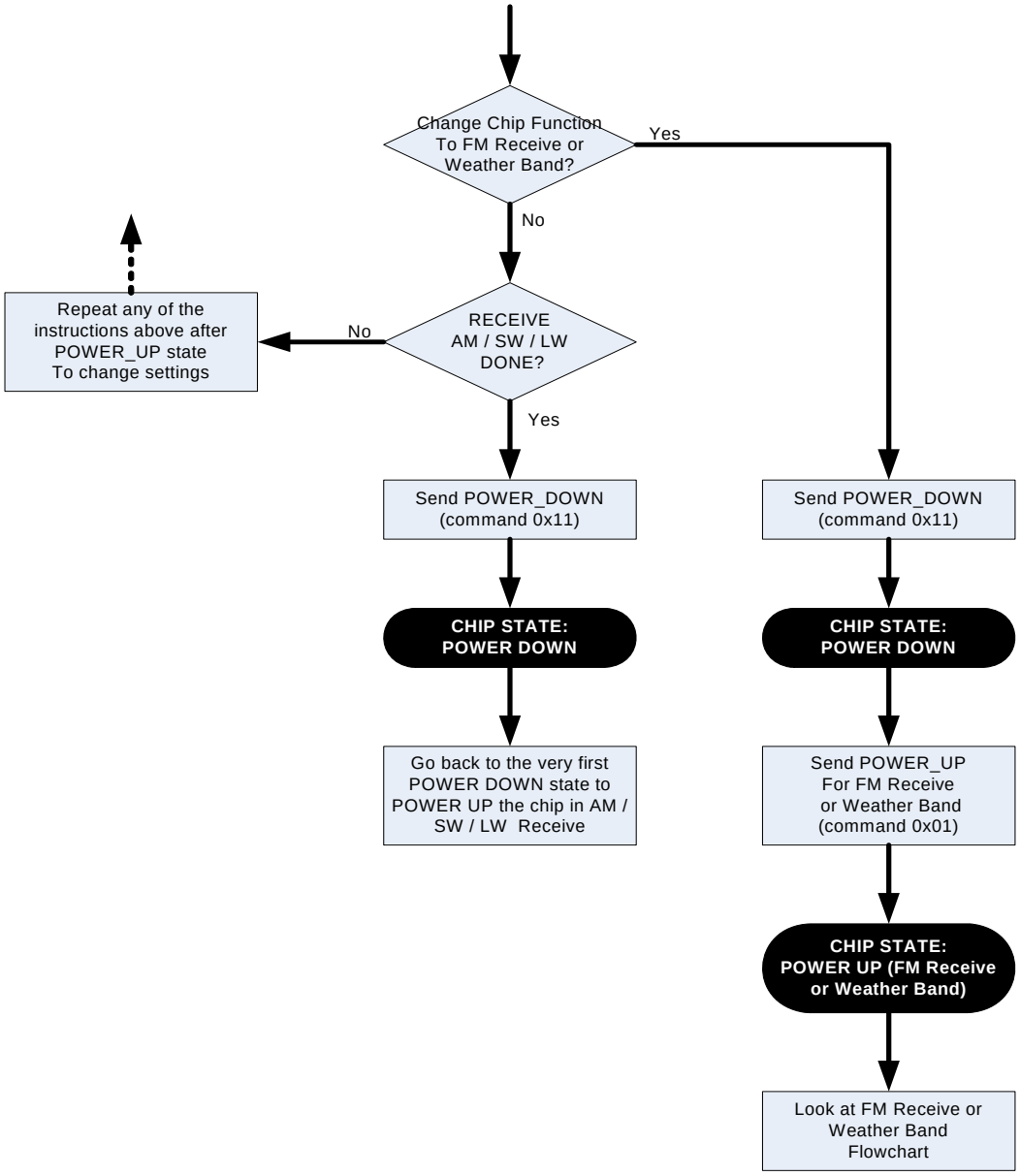

Change Chip Function To FM Receive or Weather Band?
Yes
No
RECEIVE AM / SW / LW DONE?
No
Repeat any of the instructions above after POWER_UP state To change settings
Yes
Send POWER_DOWN (command 0x11)
CHIP STATE: POWER DOWN
Go back to the very first POWER DOWN state to POWER UP the chip in AM / SW / LW Receive
Send POWER_DOWN (command 0x11)
CHIP STATE: POWER DOWN
Send POWER_UP For FM Receive or Weather Band (command 0x01)
CHIP STATE: POWER UP (FM Receive or Weather Band)
Look at FM Receive or Weather Band Flowchart

Table 57 provides an example of programming the AM/LW/SW receiver. The table is broken into three columns. The first column lists the action taking place: command (CMD), argument (ARG), status (STATUS) or response (RESP). For SET_PROPERTY commands, the property (PROP) and property data (PROPD) are indicated. The second column lists the data byte or bytes in hexadecimal that are being sent or received. An arrow preceding the data indicates data being sent from the device to the system controller. The third column describes the action.

Note that in some cases the default properties may be acceptable and no modification is necessary. Refer to Section “5. Commands and Properties” for a full description of each command and property.

Table 57. Programming Example for the AM/LW/SW Receiver

Action	Data	Description
Powerup in Digital Mode		
CMD	0x01	POWER_UP
ARG1	0xC1	Set to AM/LW/SW Receive. Enable interrupts.
ARG2	0xB0	Set to Digital Audio Output
STATUS	→0x80	Reply Status. Clear-to-send high.
		Action: Ensure that DCLK and DFS are already supplied
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x01	DIGITAL_OUTPUT_SAMPLE_RATE
ARG3 (PROP)	0x04	
ARG4 (PROPD)	0xBB	Sample rate = 48000 Hz = 0xBB80
ARG5 (PROPD)	0x80	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x01	DIGITAL_OUTPUT_FORMAT
ARG3 (PROP)	0x02	
ARG4 (PROPD)	0x00	Mode: I^2S, stereo, 16bit, sample on rising edge of DCLK.
ARG5 (PROPD)	0x00	
STATUS	→0x80	Reply Status. Clear-to-send high.
		Action: Go to Configuration (bypass “Powerup in analog mode” section). The rest of the programming is the same as analog.
Powerup in Analog Mode		
CMD	0x01	POWER_UP
ARG1	0xC1	Set to AM/LW/SW Receive. Enable interrupts.
ARG2	0x05	Set to Analog Audio Output
STATUS	→0x80	Reply Status. Clear-to-send high.
Configuration		
CMD	0x10	GET_REV
STATUS	→0x80	Reply Status. Clear-to-send high.
RESP1	→0x1F	Part Number, HEX (0x1F = 31 dec. = Si4731)
RESP2	→0x32	Firmware Major Rev, ASCII (0x32 = 2)
RESP3	→0x30	Firmware Minor Rev, ASCII (0x30 = 0)
RESP4	→0x85	Patch ID MSB, example only
RESP5	→0xC5	Patch ID LSB, example only
RESP6	→0x32	Component Firmware Major Rev, ASCII (0x32 = 2)
RESP7	→0x30	Component Firmware Minor Rev, ASCII (0x30 = 0)
RESP8	→0x42	Chip Rev, ASCII (0x42 = revB)

Table 57. Programming Example for the AM/LW/SW Receiver (Continued)

Action	Data	Description
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x00	GPO_IEN
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0x00	Set STCIEN, ERRIEN, CTSIEN
ARG5 (PROPD)	0xC1	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x02	REFCLK_FREQ
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0x7E	REFCLK = 32500 Hz
ARG5 (PROPD)	0xF4	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x02	REFCLK_PRESCALE
ARG3 (PROP)	0x02	
ARG4 (PROPD)	0x01	Divide by 400
ARG5 (PROPD)	0x90	(example RCLK = 13 MHz, REFCLK = 32500 Hz)
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x40	RX_VOLUME
ARG3 (PROP)	0x00	
ARG4 (PROPD)	0x00	Output Volume = 63
ARG5 (PROPD)	0x3F	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x31	AM_CHANNEL_FILTER
ARG3 (PROP)	0x02	
ARG4 (PROPD)	0x00	
ARG5 (PROPD)	0x01	4 kHz Bandwidth = 0x01
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x31	AM_DEEMPHASIS
ARG3 (PROP)	0x00	
ARG4 (PROPD)	0x00	50 µs
ARG5 (PROPD)	0x01	
STATUS	→0x80	Reply Status. Clear-to-send high.

Table 57. Programming Example for the AM/LW/SW Receiver (Continued)

Action	Data	Description
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x32	AM_RSQ_INTERRUPTS
ARG3 (PROP)	0x00	
ARG4 (PROPD)	0x00	Interrupt when SNR higher than RSQ SNR threshold
ARG5 (PROPD)	0x08	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x32	AM_RSQ_SNR_HIGH_THRESHOLD
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0x00	
ARG5 (PROPD)	0x0A	10 dB = 0x0A
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x32	AM_RSQ_SNR_LOW_THRESHOLD
ARG3 (PROP)	0x02	
ARG4 (PROPD)	0x00	
ARG5 (PROPD)	0x0A	10 dB = 0x0A
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x32	AM_RSQ_RSSI_HIGH_THRESHOLD
ARG3 (PROP)	0x03	
ARG4 (PROPD)	0x00	
ARG5 (PROPD)	0x1E	30 dBµV = 0x1E
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x32	AM_RSQ_RSSI_LOW_THRESHOLD
ARG3 (PROP)	0x04	
ARG4 (PROPD)	0x00	
ARG5 (PROPD)	0x0A	10 dBµV = 0x0A
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x33	AM_SOFT_MUTE_MAX_ATTENUATION
ARG3 (PROP)	0x02	
ARG4 (PROPD)	0x00	
ARG5 (PROPD)	0x0A	10 dB attenuation = 0x0A
STATUS	→0x80	Reply Status. Clear-to-send high.

Table 57. Programming Example for the AM/LW/SW Receiver (Continued)

Action	Data	Description
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x33	AM_SOFT_MUTE_SNR_THRESHOLD
ARG3 (PROP)	0x03	
ARG4 (PROPD)	0x00	
ARG5 (PROPD)	0x09	9 dB = 0x09
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x34	AM_SEEK_BAND_BOTTOM
ARG3 (PROP)	0x00	
ARG4 (PROPD)	0x02	520 kHz = 0x0208
ARG5 (PROPD)	0x08	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x34	AM_SEEK_BAND_TOP
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0x06	1710 kHz = 0x06AE
ARG5 (PROPD)	0xAE	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x34	AM_SEEK_FREQ_SPACING
ARG3 (PROP)	0x02	
ARG4 (PROPD)	0x00	10 kHz = 0x000A
ARG5 (PROPD)	0x0A	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x34	AM_SEEK_SNR_THRESHOLD
ARG3 (PROP)	0x03	
ARG4 (PROPD)	0x00	0x000B = 11 dB
ARG5 (PROPD)	0x0B	
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x34	AM_SEEK_RSSI_THRESHOLD
ARG3 (PROP)	0x04	
ARG4 (PROPD)	0x00	0x002A = 42 dBµV
ARG5 (PROPD)	0x2A	
STATUS	→0x80	Reply Status. Clear-to-send high.

Table 57. Programming Example for the AM/LW/SW Receiver (Continued)

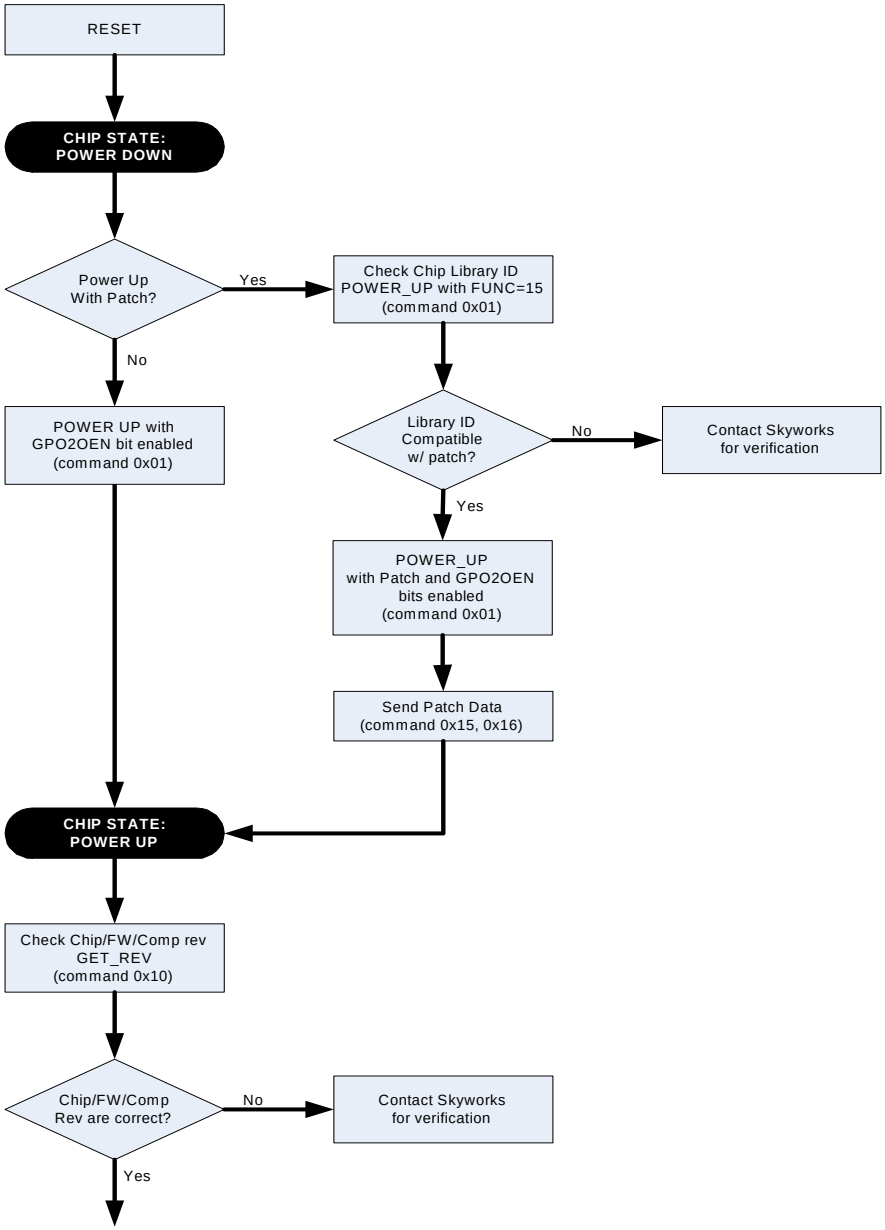
Action	Data	Description
CMD	0x40	AM_TUNE_FREQ
ARG1	0x00	
ARG2	0x03	Set frequency to 1000 kHz = 0x03E8
ARG3	0xE8	
ARG4	0x00	Automatically select tuning capacitor
ARG5	0x00	Reply Status. Clear-to-send high.
STATUS	→0x80	
CMD	0x14	GET_INT_STATUS
STATUS	→0x81	Reply Status. Clear-to-send high. STCINT = 1.
CMD	0x41	AM_SEEK_START
ARG1	0x0C	Seek up and wrap at band boundary
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x14	GET_INT_STATUS
STATUS	→0x81	Reply Status. Clear-to-send high. STCINT = 1.
CMD	0x42	AM_TUNE_STATUS
ARG1	0x01	Clear STC interrupt.
STATUS	→0x80	Reply Status. Clear-to-send high.
RESP1	→0x01	Channel is valid, AFC is not railed, and seek did not wrap at AM band boundary
RESP2	→0x03	Frequency = 0x03E8 = 1000 kHz
RESP3	→0xE8	
RESP4	→0x2A	RSSI = 0x2A = 42d = 42 dBµV
RESP5	→0x1A	SNR = 0x1A = 26d = 26 dB
RESP6	→0x0D	Value the antenna tuning capacitor is set to.
RESP7	→0x95	0x0D95 = 3477 dec.
CMD	0x43	AM_RSQ_STATUS
ARG1	0x01	Clear STC interrupt.
STATUS	→0x80	Reply Status. Clear-to-send high.
RESP1	→0x00	No SNR high, low, RSSI high, or low interrupts.
RESP2	→0x01	Channel is valid, soft mute is not activated, and AFC is not railed
RESP3	→0x00	
RESP4	→0x2A	RSSI = 0x2A = 42d = 42 dBµV
RESP5	→0x1A	SNR = 0x1A = 26d = 26 dB
CMD	0x11	POWER_DOWN
STATUS	→0x80	Reply Status. Clear-to-send high.

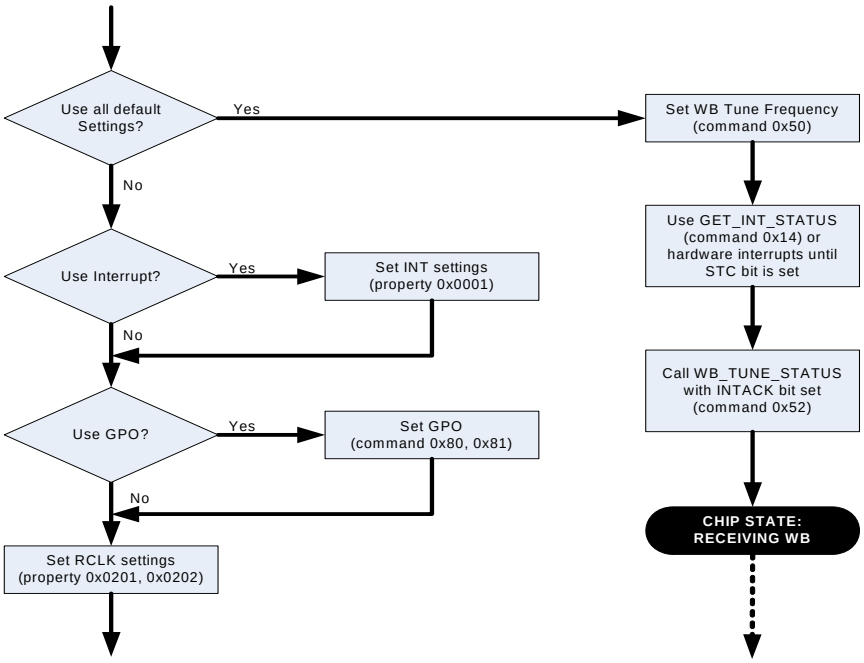
The device sets the CTS bit (and optional interrupt) to indicate that it is ready to accept the next command. The CTS bit also indicates that the POWER_UP, GET_REV, POWER_DOWN, GET_PROPERTY, GET_INT_STATUS, AM_TUNE_STATUS, and AM_RSQ_STATUS commands have completed execution.

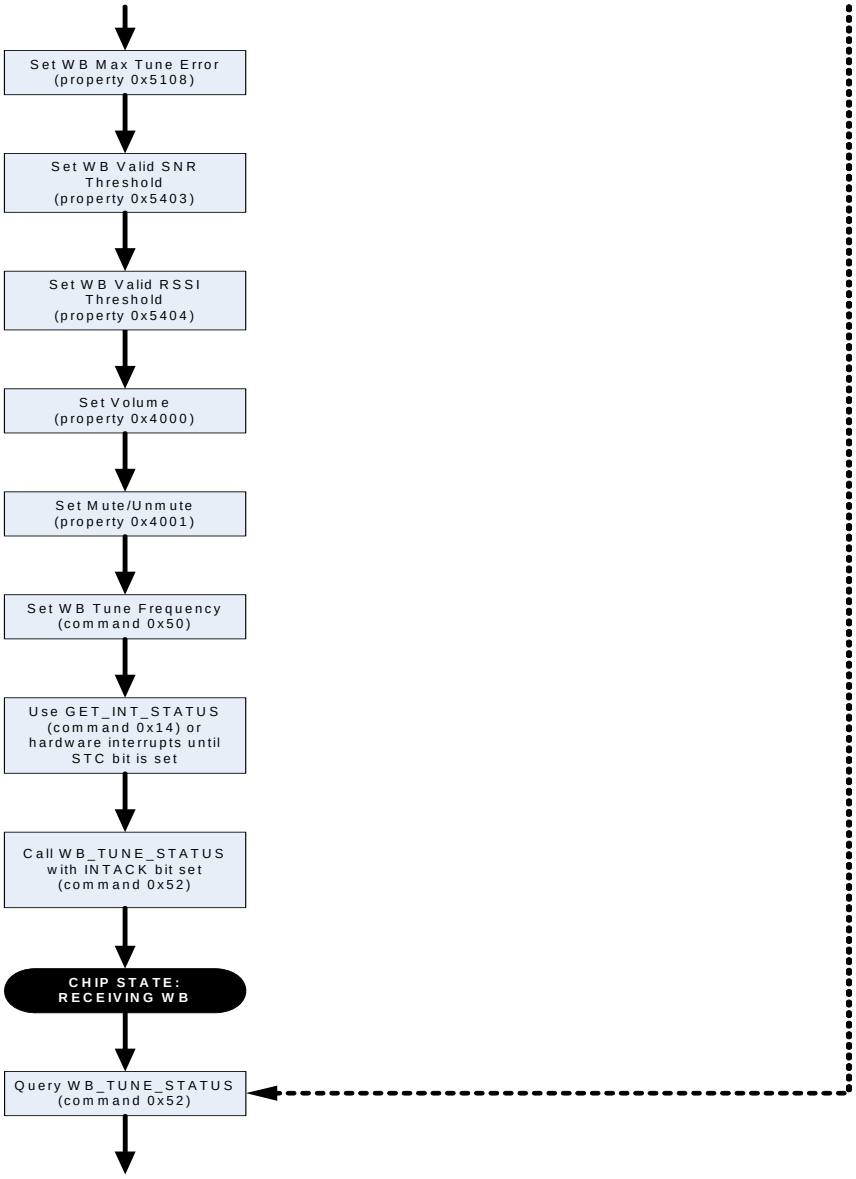
When performing a AM_TUNE_FREQ or AM_SEEK_START CTS will indicate that the device is ready to accept the next command even though the operation is not complete. GET_INT_STATUS or hardware interrupts should be used to query for the STC bit to be set prior to performing other commands. Use AM_TUNE_STATUS to clear the STC bit after it has been set.

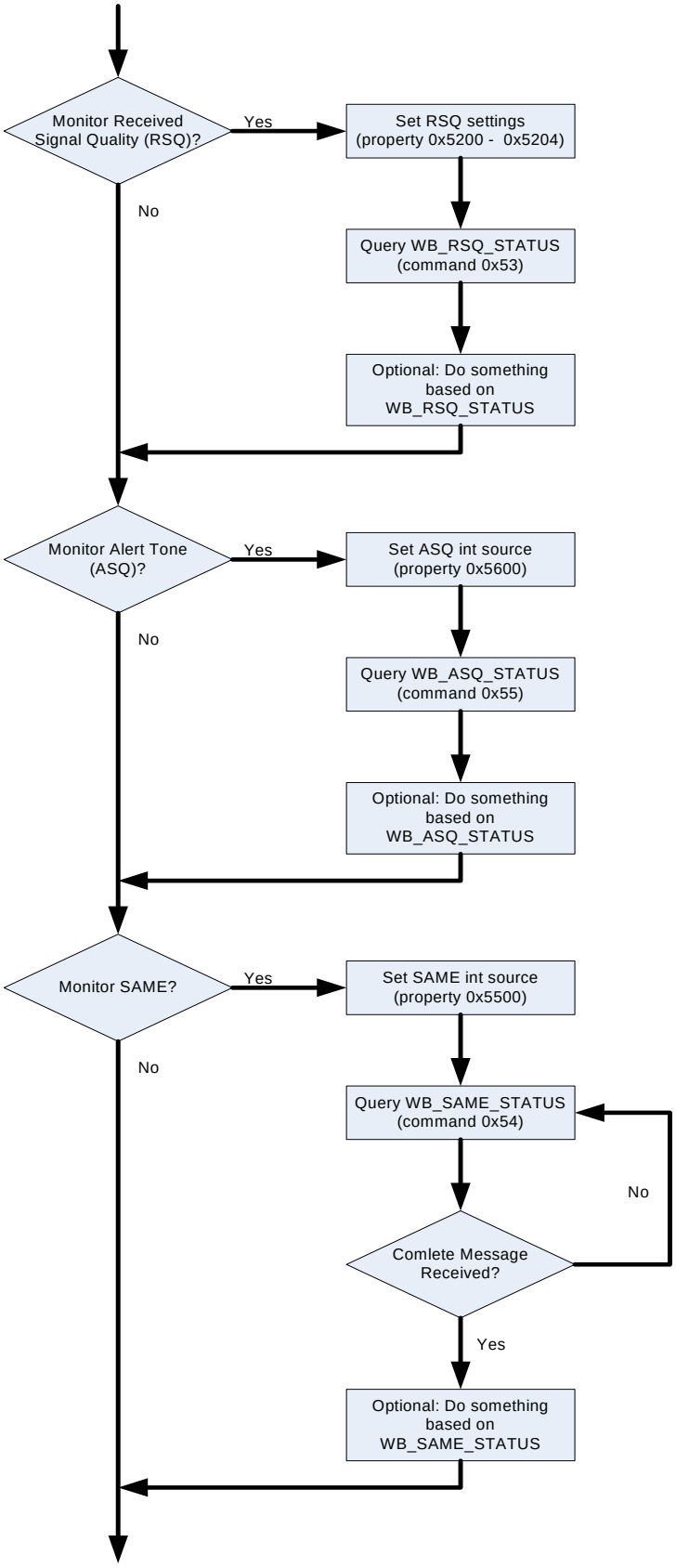
12.4. Programming Example for the WB/SAME Receiver

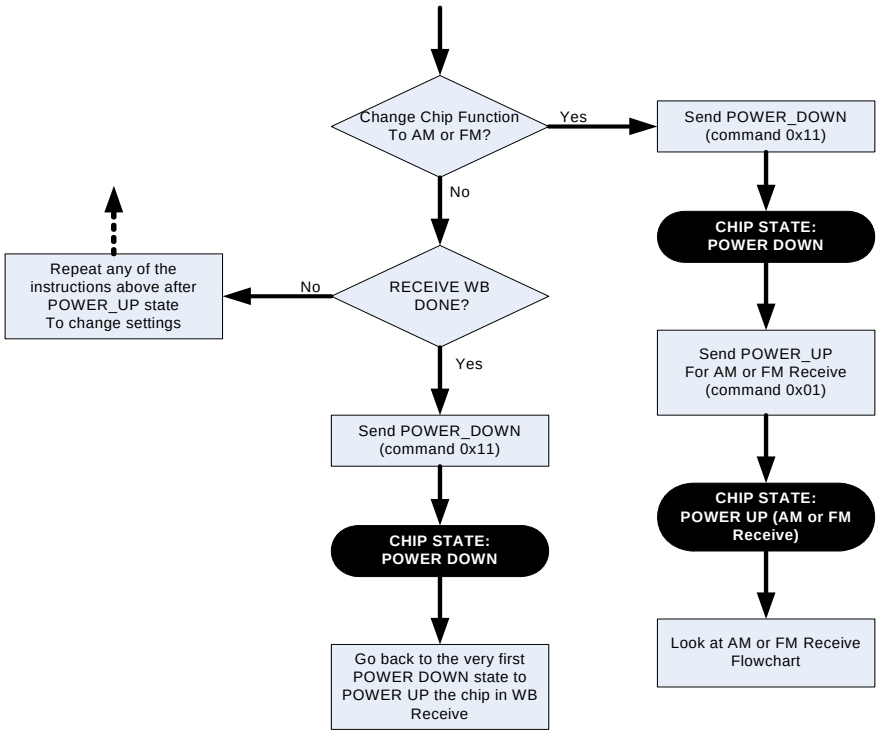
The following flowchart is an overview of how to program the WB (Weather Band) Receiver.




Use all default Settings?
Yes
No
Use Interrupt?
Yes
Set INT settings (property 0x0001)
No
Use GPO?
Yes
Set GPO (command 0x80, 0x81)
No
Set RCLK settings (property 0x0201, 0x0202)
Set WB Tune Frequency (command 0x50)
Use GET_INT_STATUS (command 0x14) or hardware interrupts until STC bit is set
Call WB_TUNE_STATUS with INTACK bit set (command 0x52)
CHIP STATE: RECEIVING WB


Set WB Max Tune Error (property 0x5108)
Set WB Valid SNR Threshold (property 0x5403)
Set WB Valid RSSI Threshold (property 0x5404)
Set Volume (property 0x4000)
Set Mute/Unmute (property 0x4001)
Set WB Tune Frequency (command 0x50)
Use GET_INT_STATUS (command 0x14) or hardware interrupts until STC bit is set
Call WB_TUNE_STATUS with INTACK bit set (command 0x52)
CHIP STATE: RECEIVING WB
Query WB_TUNE_STATUS (command 0x52)


Monitor Received Signal Quality (RSQ)?
Yes
Set RSQ settings (property 0x5200 - 0x5204)
No
Query WB_RSQ_STATUS (command 0x53)
Optional: Do something based on WB_RSQ_STATUS
Monitor Alert Tone (ASQ)?
Yes
Set ASQ int source (property 0x5600)
No
Query WB_ASQ_STATUS (command 0x55)
Optional: Do something based on WB_ASQ_STATUS
Monitor SAME?
Yes
Set SAME int source (property 0x5500)
No
Query WB_SAME_STATUS (command 0x54)
No
Comlete Message Received?
Yes
Optional: Do something based on WB_SAME_STATUS


Change Chip Function
To AM or FM?
Yes
Send POWER_DOWN
(command 0x11)
No
CHIP STATE:
POWER DOWN
Send POWER_UP
For AM or FM Receive
(command 0x01)
CHIP STATE:
POWER UP (AM or FM
Receive)
Look at AM or FM Receive
Flowchart
Repeat any of the
instructions above after
POWER_UP state
To change settings
No
RECEIVE WB
DONE?
Yes
Send POWER_DOWN
(command 0x11)
CHIP STATE:
POWER DOWN
Go back to the very first
POWER DOWN state to
POWER UP the chip in WB
Receive

For detailed information on SAME processing, please refer to the following flow chart:

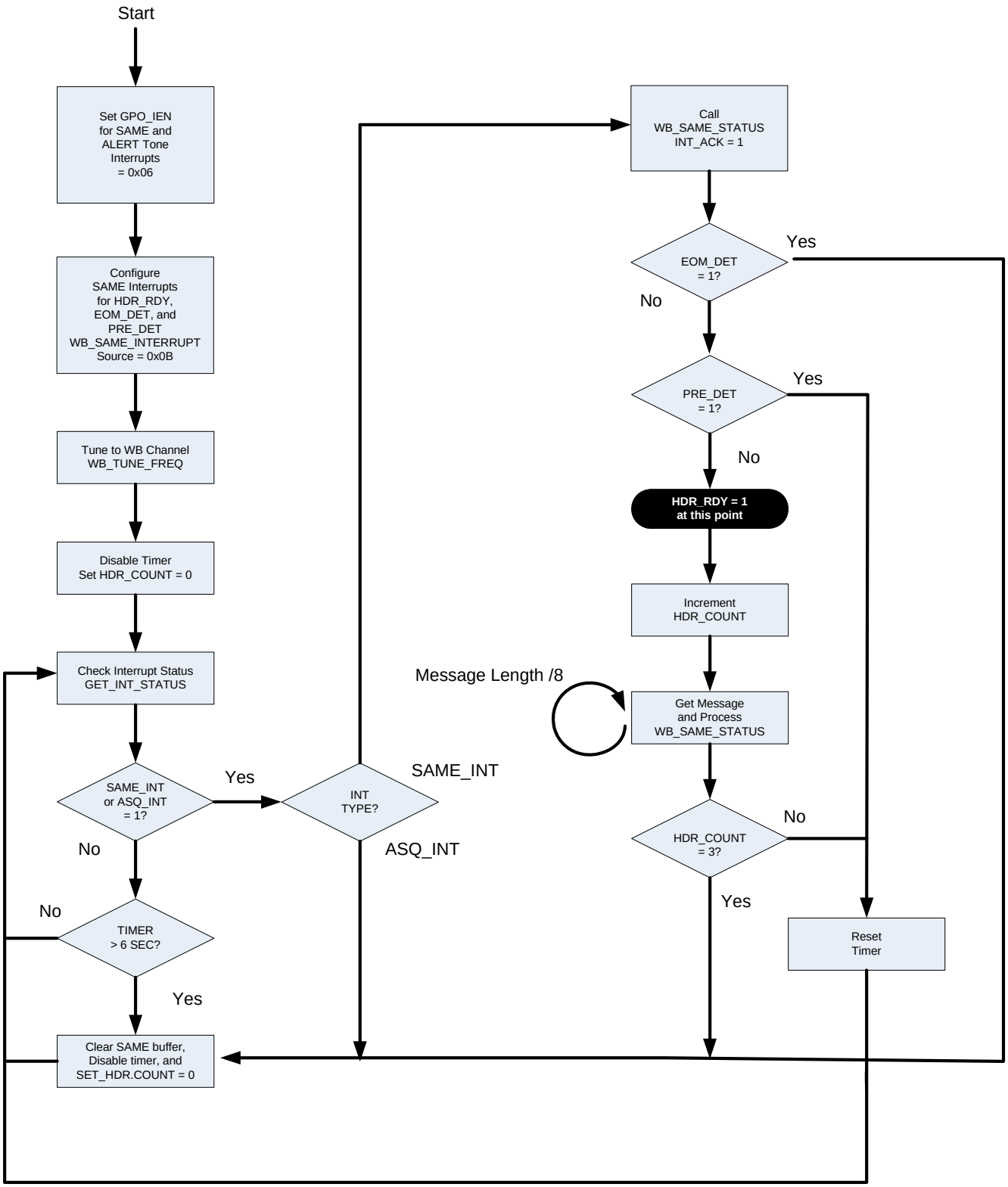


Table 58 provides an example for the WB Receiver. The table is broken into three columns. The first column lists the action taking place: command (CMD), argument (ARG), status (STATUS) or response (RESP). For SET_PROPERTY commands, the property (PROP) and property data (PROPD) are indicated. The second column lists the data byte or bytes in hexadecimal that are being sent or received. An arrow preceding the data indicates data being sent from the device to the system controller. The third column describes the action.

Note that in some cases the default properties may be acceptable and no modification is necessary. Refer to Section “5. Commands and Properties” for a full description of each command and property.

Table 58. Programming Example for the WB/SAME Receiver

Action	Data	Description
CMD	0x01	POWER_UP
ARG1	0xC3	Set to weatherband receive. Enable interrupts.
ARG2	0x05	Set to Analog Out.
STATUS	→0x80	Reply Status. Clear-to-send high.
CMD	0x10	GET_REV
STATUS	→ 0x80	Reply Status. Clear-to-send high.
RESP1	→ 0x25	Part Number, HEX (0x25 = 37 dec. = Si4737)
RESP2	→ 0x30	Firmware Major Rev, ASCII (0x30 = 0)
RESP3	→ 0x41	Firmware Minor Rev, ASCII (0x41 = A)
RESP4	→ 0x13	Patch ID MSB, example only
RESP5	→ 0x36	Patch ID LSB, example only
RESP6	→ 0x30	Component Firmware Major Rev, ASCII (0x30 = 0)
RESP7	→ 0x41	Component Firmware Minor Rev, ASCII (0x41 = A)
RESP8	→ 0x42	Chip Rev, ASCII (0x42 = revB)
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x00	GPO_IEN
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0x00	Set STCIEN, ERRIEN, CTSIEN, ASQIEN, SAMEIEN
ARG5 (PROPD)	0xC7	
STATUS	→ 0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x02	REFCLK_FREQ
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0x80	REFCLK = 32768 Hz
ARG5 (PROPD)	0x00	
STATUS	→ 0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x02	REFCLK_PRESCALE
ARG3 (PROP)	0x02	
ARG4 (PROPD)	0x00	Divide by 1
ARG5 (PROPD)	0x01	
STATUS	→ 0x80	Reply Status. Clear-to-send high.

Table 58. Programming Example for the WB/SAME Receiver (Continued)

CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x40	RX_VOLUME
ARG3 (PROP)	0x00	
ARG4 (PROPD)	0x00	Output Volume = 63
ARG5 (PROPD)	0x3F	
STATUS	→ 0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x40	RX_HARD_MUTE
ARG3 (PROP)	0x01	
ARG4 (PROPD)	0x00	Enable L and R audio outputs
ARG5 (PROPD)	0x00	
STATUS	→ 0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x54	WB_VALID_SNR_THRESHOLD
ARG3 (PROP)	0x03	
ARG4 (PROPD)	0x00	Threshold = 06 dB = 0x0006
ARG5 (PROPD)	0x06	
STATUS	→ 0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x54	WB_VALID_RSSI_THRESHOLD
ARG3 (PROP)	0x04	
ARG4 (PROPD)	0x00	Threshold = 20 dBµV = 0x0014
ARG5 (PROPD)	0x14	
STATUS	→ 0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET_PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x56	WB_ASQ_INTERRUPT_SOURCE
ARG3 (PROP)	0x00	
ARG4 (PROPD)	0x00	Interrupt when alert tone is present.
ARG5 (PROPD)	0x01	
STATUS	→ 0x80	Reply Status. Clear-to-send high.
CMD	0x12	SET PROPERTY
ARG1	0x00	
ARG2 (PROP)	0x55	WB_SAME_INTERRUPT_SOURCE
ARG3 (PROP)	0x00	(Si4707 only)
ARG4 (PROPD)	0x00	Interrupt when header is ready.
ARG5 (PROPD)	0x01	
STATUS	→ 0x80	Reply Status. Clear-to-send high.

Table 58. Programming Example for the WB/SAME Receiver (Continued)

CMD	0x50	WB_TUNE_FREQ
ARG1	0x00	
ARG2	0xFD	Set frequency to 162.4 MHz = 0xFDC0
ARG3	0xC0	Frequency is set in units of 2500 Hz.
STATUS	→ 0x80	Reply Status. Clear-to-send high.
CMD	0x14	GET_INT_STATUS
STATUS	→ 0x81	Reply Status. Clear-to-send high. STCINT = 1.
CMD	0x52	WB_TUNE_STATUS
ARG1	0x01	Clear STC interrupt.
STATUS	→ 0x80	Reply Status. Clear-to-send high.
RESP1	→ 0x01	Valid Frequency.
RESP2	→ 0xFD	Frequency = 0xFDC0 = 162.4 MHz
RESP3	→ 0xC0	
RESP4	→ 0x22	RSSI = 34 dBµV
RESP5	→ 0x17	SNR = 23 dB
CMD	0x55	WB_ASQ_STATUS
ARG1	0x01	
STATUS	→ 0x80	Reply Status. Clear-to-send high.
RESP1	→ 0x02	Alert tone is not present.
SAME (Si4707 Only)		
CMD	0x14	GET_INT_STATUS
STATUS	→ 0x84	Reply Status. Clear-to-send high. SAMEINT = 1.
CMD	0x54	WB_SAME_STATUS
ARG1	0x01	Clear SAME interrupt.
ARG2	0x00	Begin reading message from byte 0.
STATUS	→ 0x80	Reply Status. Clear-to-send high.
RESP1	→ 0x0F	Message flags set.
RESP2	→ 0x00	State = End of message.
RESP3	→ 0xFE	Message length 254 bytes.
RESP4	→ 0xFF	Data confidence level = high.
RESP5	→ 0x2D	Data0
RESP6	→ 0x57	Data1
RESP7	→ 0x58	Data2
RESP8	→ 0x52	Data3
RESP9	→ 0x2D	Data4
RESP10	→ 0x56	Data5
RESP11	→ 0x4F	Data6
RESP12	→ 0x57	Data7
		Note: This command should be called repeatedly with the readaddr[7:0] incremented by 8 each time until all 254 bytes (in this example) are returned. The buffer should then be cleared as described in the WB_SAME_STATUS:CLRBUF bit description.
CMD	0x11	POWER_DOWN
STATUS	→ 0x80	Reply Status. Clear-to-send high.

The device sets the CTS bit (and optional interrupt) to indicate that it is ready to accept the next command. The CTS bit also indicates that the POWER_UP, GET_REV, POWER_DOWN, GET_PROPERTY, GET_INT_STATUS, WB_TUNE_STATUS, WB_ASQ_STATUS, and WB_RSQ_STATUS commands have completed execution.

When performing a WB_TUNE_FREQ CTS will indicate that the device is ready to accept the next command even though the operation is not complete. GET_INT_STATUS or hardware interrupts should be used to query for the STC bit to be set prior to performing other commands. Use WB_TUNE_STATUS to clear the STC bit after it has been set.

Appendix A—Comparison of the Si4704/05/3x-B20, Si4704/05/3x-C40, and Si4704/05/3x-D60

This appendix describes the configuration, command, and property differences between silicon and firmware revisions of the Si4704/05/3x-B20, Si4704/05-3x-C40, and Si4704/05/3x-D60 devices. Each revision is referred to by its die revision and firmware revision suffix according to Table 1. For a more detailed configuration reference, consult “AN332: Si47xx Programming Guide”.

Table 59. Die Revision and Firmware Revision Table

Part Number	Function	Die Revision	Firmware Revision	Die Revision + Firmware Revision Suffix
Si4704-B20-GM/GU	FM Receiver	B	20	-B20
Si4705-B20-GM/GU	FM RDS Receiver	B	20	-B20
Si4730-B20-GM/GU	AM/FM Receiver	B	20	-B20
Si4731-B20-GM/GU	AM/FM RDS Receiver	B	20	-B20
Si4734-B20-GM/GU	AM/SW/FM Receiver	B	20	-B20
Si4735-B20-GM/GU	AM/SW/FM RDS Receiver	B	20	-B20
Si4704-C40-GM/GU	FM Receiver	C	40	-C40
Si4705-C40-GM/GU	FM RDS Receiver	C	40	-C40
Si4730-C40-GM/GU	AM/FM Receiver	C	40	-C40
Si4731-C40-GM/GU	AM/FM RDS Receiver	C	40	-C40
Si4734-C40-GM/GU	AM/SW/FM Receiver	C	40	-C40
Si4735-C40-GM/GU	AM/SW/FM RDS Receiver	C	40	-C40
Si4704-D60-GM/GU	FM Receiver	D	60	-D60
Si4705-D60-GM/GU	FM RDS Receiver	D	60	-D60
Si4730-D60-GM/GU	AM/FM Receiver	D	60	-D60
Si4731-D60-GM/GU	AM/FM RDS Receiver	D	60	-D60
Si4734-D60-GM/GU	AM/SW/FM Receiver	D	60	-D60
Si4735-D60-GM/GU	AM/SW/FM RDS Receiver	D	60	-D60

Each of the following subsections describes the differences between revisions for groups of properties and/or commands. Each property is listed as PROPERTY_NAME (number) = default (supported revisions).

Hexadecimal values are immediately preceded by “0x”; all other numeric values are decimal.

AM, FM, and WB errata on -B20 have been addressed in -C40 and/or -D60 devices.

The -D60 is the most recent revision and offers advanced features not available in the -C40 and -B20 revisions.

FM Properties and Commands

The properties and commands in this section are related to FM mode.

FM Mode Max Tune Error (0x110x Properties)

FM_MODE_MAX_TUNE_ERROR (0x1108) = 30 (-B20), 20 (-C40, -D60)

Maximum tune error in kHz is stored in property 0x1108. It has a default setting of 30 kHz in -B20, and a default setting of 20 kHz in -C40 and -D60. It should be noted that 20 kHz has been recommended for best performance even on -B20 devices through AN332.

FM RSQ Interrupt Configuration (0x120x Properties)

FM_RSQ_MULTIPATH_HIGH_THRESHOLD (0x1205) = 127 (-D60)

FM_RSQ_MULTIPATH_LOW_THRESHOLD (0x1206) = 0 (-D60)

Properties 0x1205 and 0x1206 are only available on -D60 parts.

FM Soft Mute Configuration (0x130x Properties)

FM_SOFT_MUTE_SLOPE (0x1301) = 2 (-C40, -D60)

The target soft mute target attenuation - up to a set maximum attenuation level - is calculated as the difference between the soft mute threshold and the received SNR multiplied by a property value called the FM_SOFT_MUTE_SLOPE. In -C40 and -D60, the default slope is 2 dB/dB. In in -B20, the slope is not configurable through a property, but is also 2 dB/dB.

Stereo Blend Thresholds (0x110x, 0x180x Properties)

FM_BLEND_STEREO_THRESHOLD (0x1105) = 49 (-B20, -C40)

FM_BLEND_MONO_THRESHOLD (0x1106) = 30 (-B20, -C40)

FM_BLEND_RSSI_STEREO_THRESHOLD (0x1800) = 49 (-D60)

FM_BLEND_RSSI_MONO_THRESHOLD (0x1801) = 30 (-D60)

FM_BLEND_RSSI_ATTACK_RATE (0x1802) = 4000 (-D60)

FM_BLEND_RSSI_RELEASE_RATE (0x1803) = 400 (-D60)

FM_BLEND_SNR_STEREO_THRESHOLD (0x1804) = 27 (-D60)

FM_BLEND_SNR_MONO_THRESHOLD (0x1805) = 14 (-D60)

FM_BLEND_SNR_ATTACK_RATE (0x1806) = 4000 (-D60)

FM_BLEND_SNR_RELEASE_RATE (0x1807) = 400 (-D60)

FM_BLEND_MULTIPATH_STEREO_THRESHOLD (0x1808) = 20 (-D60)

FM_BLEND_MULTIPATH_MONO_THRESHOLD (0x1809) = 60 (-D60)

FM_BLEND_MULTIPATH_ATTACK_RATE (0x180A) = 4000 (-D60)

FM_BLEND_MULTIPATH_RELEASE_RATE (0x180B) = 40 (-D60)

In -B20 and -C40, FM stereo blend is only determined by RSSI based on blend thresholds set in 0x1105 and 0x1106. In -D60 devices, a series of advanced blend properties have been added to improve the user experience

under dynamic signal conditions. To accommodate for this change, RSSI based threshold properties were relocated respectively to properties 0x1800 and 0x1801. 0x1800 and 0x1801 have the same default values as 0x1105 and 0x1106.

Additional advanced blend features include stereo blending based on SNR and multipath thresholds. For each set of thresholds, separate blend attack (into mono) and release (into stereo) rates may be set. Each of the factors is independently evaluated, and any may trigger a blend into mono at its given threshold and rate. To remove any of the advanced blend factors from consideration; set the corresponding blend thresholds to min value of 0 for SNR based blend (0x1804/0x1805), and set the corresponding blend thresholds to max value of 100 for multipath based blend (0x1808/0x1809).

FM Commands

Some parameters and returned values are only applicable to -D60 parts. These are: multipath indicator returned by the FM_TUNE_STATUS command and the MULTIPATH_DETECT_HIGH and MULTIPATH_DETECT_LOW parameters of the FM_RSQ_STATUS command.

In -C40 and -D60 devices, the RDSSYNC bit of the response to an FM_RDS_STATUS command may be incorrectly set. A patch is available only for -D60 devices.

AM Properties

The properties and commands in this section are related to AM mode.

AM Mode Configuration (0x310x Properties)

AM_MODE_AVC_MAX_GAIN (0x3103) = 0x1543 (-C40, -D60)

AM_MODE_AFC_SW_PULL_IN_RANGE (0x3104) = 8695 (-C40, -D60)

AM_MODE_AFC_SW_LOCK_IN_RANGE (0x3105) = 11765 (-C40, -D60)

AM_MODE_AVC_MAX_GAIN is available in -C40 and -D60 devices with a default max gain of 16 dB. In -B20, the AVC gain is set at maximum and not available through a property. To make -C40 or -D60 behave as -B20, set AM_MODE_MAX_GAIN to 0x7800.

AM shortwave AFC range properties are available in -C40 and -D60 devices (supported by Si4734/35 devices only). The default values of these properties provide similar behavior to the behavior of -B20 devices. However, in -B20 devices, these properties are not available through the programming API.

AM Soft Mute Configuration (0x330x Properties)

AM_SOFT_MUTE_SLOPE (0x3301) = 2 (-B20), 1 (-C40, -D60)

AM_SOFT_MUTE_MAX_ATTENUATION (0x3302) = 16 (-B20), 8 (-C40, -D60)

AM_SOFT_MUTE_SNR_THRESHOLD (0x3303) = 10 (-B20), 8 (-C40, -D60)

Settings for Audio Soft Mute

Soft mute is active when SNR falls below the given AM_SOFT_MUTE_SNR_THRESHOLD. When active, the output audio will be decreased at a set rate until the target soft mute attenuation is achieved. In -B20 devices the threshold is 10 dB, whereas in -C40 and -D60 devices it is 8 dB.

The target soft mute target attenuation - up to a set maximum attenuation level - is calculated as the difference between the soft mute threshold and the received SNR multiplied by a scalar value called the soft mute slope. The default value of this property is 1 dB/dB in -C40 and -D60. In -B20, the value used is 2 dB/dB.

The maximum soft mute attenuation level is 10 dB in -B20. In -C40 and -D60 devices, the maximum level can be set by a property AM_SOFT_MUTE_MAXIMUM_ATTENUATION, which has a default value of 8 dB.

The soft mute default changes in -C40 and -D60 have been made to improve weak signal listening experience.

APPENDIX B—Si4704/05/3X-B20/-C40/-D60 COMPATIBILITY CHECKLIST

This appendix describes the configuration differences between hardware revisions of Si4704/05/3x devices. It describes how to achieve backwards compatibility between systems designed for Si4704/05/3x-B20, -C40, and -D60 device hardware revisions. It is not intended as a complete reference to Si4704/05/3x configuration. For an in-depth configuration reference, consult “AN332: Si47xx Programming Guide”.

In this appendix, each revision is referred to by its die revision and firmware revision suffix according to the following table.

Table 60. Die Revision and Firmware Revision Table

Part Number	Function	Die Revision	Firmware Revision	Die Revision + Firmware Revision Suffix
Si4704-B20-GM/GU	FM Receiver	B	20	-B20
Si4705-B20-GM/GU	FM RDS Receiver	B	20	-B20
Si4730-B20-GM/GU	AM/FM Receiver	B	20	-B20
Si4731-B20-GM/GU	AM/FM RDS Receiver	B	20	-B20
Si4734-B20-GM/GU	AM/SW/FM Receiver	B	20	-B20
Si4735-B20-GM/GU	AM/SW/FM RDS Receiver	B	20	-B20
Si4704-C40-GM/GU	FM Receiver	C	40	-C40
Si4705-C40-GM/GU	FM RDS Receiver	C	40	-C40
Si4730-C40-GM/GU	AM/FM Receiver	C	40	-C40
Si4731-C40-GM/GU	AM/FM RDS Receiver	C	40	-C40
Si4734-C40-GM/GU	AM/SW/FM Receiver	C	40	-C40
Si4735-C40-GM/GU	AM/SW/FM RDS Receiver	C	40	-C40
Si4704-D60-GM/GU	FM Receiver	D	60	-D60
Si4705-D60-GM/GU	FM RDS Receiver	D	60	-D60
Si4730-D60-GM/GU	AM/FM Receiver	D	60	-D60
Si4731-D60-GM/GU	AM/FM RDS Receiver	D	60	-D60
Si4734-D60-GM/GU	AM/SW/FM Receiver	D	60	-D60
Si4735-D60-GM/GU	AM/SW/FM RDS Receiver	D	60	-D60

Hexadecimal values are immediately preceded by “0x”; all other numeric values are decimal.

To Achieve Similar Performance in SI4704/05/3X-D60 to SI4704/05/3X-C40

The -D60 devices have a more advanced feature set than -C40 devices. This section describes a step-by-step procedure to achieve similar performance from -D60 devices to that of -C40 devices by modifying or disabling some of the advanced features.

FM Receiver Mode

- There is a debug feature that remains active in Si4704/05/3x-D60 firmware which can create periodic noise in audio. Skyworks Solutions recommends you disable this feature by sending the following bytes (shown here in hexadecimal form):

  0x12 0x00 0xFF 0x00 0x00 0x00
- In Si4704/05/3x-D60 devices, the FM_BLEND_RSSI_STEREO_THRESHOLD property is no longer at address 0x1105. Use address 0x1800 instead.
- In Si4704/05/3x-D60 devices, the FM_BLEND_RSSI_MONO_THRESHOLD property is no longer at address 0x1106. Use address 0x1801 instead.
- To disable the SNR-based stereo blend, set both the FM_BLEND_SNR_STEREO_THRESHOLD property (0x1804) and the FM_BLEND_SNR_MONO_THRESHOLD property (0x1805) to 0.
- To disable the multipath-based stereo blend, set both the FM_BLEND_MULTIPATH_STEREO_THRESHOLD property (0x1808) and the FM_BLEND_MULTIPATH_MONO_THRESHOLD property (0x1809) to 100 (0x64).

AM Receive Mode

Si473x-D60 devices are compatible with Si473x-C40 devices in AMRX mode.

WB Receive Mode

There are no Si473x-D60 devices which support WBRX mode.

To Achieve Similar Performance in SI4704/05/3X-D60 to SI4704/05/3X-B20

The -D60 devices have a more advanced feature set than -B20 devices. This section describes a step-by-step procedure to achieve similar performance from -D60 devices to that of -B20 devices by modifying or disabling some of the advanced features.

FM Receiver Mode

- There is a debug feature that remains active in Si4704/05/3x-D60 firmware which can create periodic noise in audio. Skyworks Solutions recommends you disable this feature by sending the following bytes (shown here in hexadecimal form):

  0x12 0x00 0xFF 0x00 0x00 0x00
- In Si4704/05/3X-D60 devices, the FM_BLEND_RSSI_STEREO_THRESHOLD property is no longer at address 0x1105. Use address 0x1800 instead.
- In Si4704/05/3X-D60 devices, the FM_BLEND_RSSI_MONO_THRESHOLD property is no longer at address 0x1106. Use address 0x1801 instead.
- To disable the SNR-based stereo blend, set both the FM_BLEND_SNR_STEREO_THRESHOLD property (0x1804) and the FM_BLEND_SNR_MONO_THRESHOLD property (0x1805) to 0.
- To disable the multipath-based stereo blend, set both the FM_BLEND_MULTIPATH_STEREO_THRESHOLD property (0x1808) and the FM_BLEND_MULTIPATH_MONO_THRESHOLD property (0x1809) to 100 (0x64).

AM Receive Mode

- Set the AM_MODE_AVC_MAX_GAIN property (0x3103) to 0x7800.
- Set the AM_SOFT_MUTE_THRESHOLD property (03303) to 10.
- Set the AM_SOFT_MUTE_SLOPE property (0x3301) to 2
- Set the AM_SOFT_MUTE_MAX_ATTENUATION property (0x3302) to 16.

WB Receive Mode

There are no Si473x-D60 devices which support WBRX mode.

To Achieve Similar Performance in Si4704/05/3X-C40 to Si4704/05/3X-B20

This section describes a step-by-step procedure to achieve performance from -C40 devices that is similar to that of -B20 devices.

FM Receiver Mode

Si473x-C40 devices are compatible with Si473x-B20 devices in FMRX mode.

AM Receive Mode

- Set the AM_MODE_AVC_MAX_GAIN property (0x3103) to 0x7800 (maximum).
- Set the AM_SOFT_MUTE_THRESHOLD property (0x3303) to 10 (db).
- Set the AM_SOFT_MUTE_SLOPE property (0x3301) to 2 (dB/dB).
- Set the AM_SOFT_MUTE_MAX_ATTENUATION property (0x3302) to 16 (dB).

WB Receive Mode

Si473x-C40 devices are compatible with Si473x-B20 devices in WBRX mode.

Document Change List

Revision 0.1 to Revision 0.2

- Updated Product Matrix in Table 1.
- Added Si4706 FM and High-Performance RDS Receiver support.
- Added Si4707 WB/SAME Receiver support.
- Added Si4740/41 multipath, blend, and AGC properties.
- Added Si4749 High-Performance RDS Receiver support.
- Updated Firmware, Library, and Component Compatibility tables.
- Added Command Timing Parameters for the WB Receiver.
- Updated FM Transmitter maximum audio volume recommendations.

Revision 0.2 to Revision 0.3

- Added notes to AM/SW/LW Receiver Reference Clock section.
- Removed Si4706/07/4x–related material.
- Updated product matrix in Table 1.

Revision 0.3 to Revision 0.4

- Added Si4704/05/30/31/34/35/36/37/38/39-C40 receiver support and additional AM properties.
- Added Si4784/85-B20 receiver support.
- Updated product matrix in Table 1.
- Updated with corrections to couple commands and properties.

Revision 0.4 to Revision 0.41

- Minor edits.

Revision 0.41 to Revision 0.5

- Combined information in AN332 Rev. 0.41 and AN344 Rev. 0.4 into AN332 Rev. 0.5.
- Added information for Si47xx-D50 and Si47xx-D60 parts.

Revision 0.5 to Revision 0.6

- Added Appendix A and Appendix B.

Revision 0.6 to Revision 0.7

- Added FM_BLEND_MAX_STEREO_SEPARATION property

Revision 0.7 to Revision 0.8

- Corrected pin numbers of LIN and RIN for Si4704/05/3x-D60 parts.
- Added more explanations to property 0x1900 and 0x3103.
- Added AUXIN Components in Tables 33, 38, and 41.

Revision 0.8 to Revision 0.9

- Added Si4732 AM/SW/LW/FM RDS Receiver support.

Revision 0.9 to Revision 1.0

- Removed information about AUXIN components.
- Added notes to powerup command section.

Revision 1.0 to Revision 1.1

- Added Si4704/05/30/31-D62 part information.
- Removed AUXIN components from Si4704/05/30/31/34/35-D60 parts.

Revision 1.1 to Revision 1.2

- Added information that Digital Output is available in Si4704-D60 and later.
- Added errata for the digital audio input for three devices: Si4710-B30, Si4712-B30, Si4720-B20.

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