

## FEATURES

- 1 pF off capacitance
- 2.6 pF on capacitance
- <1 pC charge injection
- 33 V supply range
- 120  $\Omega$  on resistance
- Fully specified at  $\pm 15\text{ V}$ , +12 V
- No  $V_L$  supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- 16-lead TSSOP
- Typical power consumption: <0.03  $\mu\text{W}$

## ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Product change notification
- Qualification data available on request

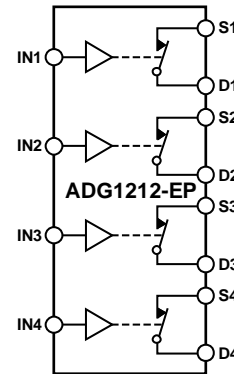
## APPLICATIONS

- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Audio signal routing
- Video signal routing
- Communication systems

## GENERAL DESCRIPTION

The **ADG1212-EP** is a monolithic complementary metal-oxide semiconductor (CMOS) device containing four independently selectable switches designed on an *i*CMOS® (industrial CMOS) process. *i*CMOS is a modular manufacturing process combining high voltage CMOS and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

## FUNCTIONAL BLOCK DIAGRAM



NOTES  
1. SWITCHES SHOWN ARE FOR LOGIC 1 INPUT.

Figure 1.

10012-201

The ultralow capacitance and charge injection of this switch makes it an ideal solution for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Fast switching speed coupled with high signal bandwidth makes the part suitable for video signal switching.

*i*CMOS construction ensures ultralow power dissipation, making the part ideally suited for portable and battery-powered instruments.

The **ADG1212-EP** contains four independent single-pole/single-throw (SPST) switches. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

Additional application and technical information can be found in the **ADG1212** data sheet.

## PRODUCT HIGHLIGHTS

1. Ultralow capacitance.
2. <1 pC charge injection.
3. 3 V logic compatible digital inputs:  $V_{IH} = 2.0\text{ V}$ ,  $V_{IL} = 0.8\text{ V}$ .
4. No  $V_L$  logic power supply required.
5. Ultralow power dissipation: <0.03  $\mu\text{W}$ .
6. 16-lead TSSOP package.

Rev. B

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**REVISION HISTORY**

**5/2018—Rev. A to Rev. B**

Change to Enhanced Product Features Section .....	1
Changes to Ordering Guide .....	11

**7/2012—Rev. 0 to Rev. A**

Changed Operating Temperature Range from $-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ to $-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ ; Table 3.....	5
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**11/2011—Revision 0: Initial Version**

## SPECIFICATIONS

### DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ , GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range				V	
On Resistance ( $R_{ON}$ )	120			$\Omega$ typ	$V_S = \pm 10\text{ V}$ , $I_S = -1\text{ mA}$ ; see Figure 15
	190	230	260	$\Omega$ max	$V_{DD} = +13.5\text{ V}$ , $V_{SS} = -13.5\text{ V}$
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	2.5			$\Omega$ typ	$V_S = \pm 10\text{ V}$ , $I_S = -1\text{ mA}$
	6	10	11	$\Omega$ max	
On Resistance Flatness ( $R_{FLAT(ON)}$ )	20			$\Omega$ typ	$V_S = -5\text{ V}/0\text{ V}/+5\text{ V}$ ; $I_S = -1\text{ mA}$
	57	72	79	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.02$			nA typ	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$
	$\pm 0.1$	$\pm 0.6$	$\pm 1$	nA max	$V_S = \pm 10\text{ V}$ , $V_D = \pm 10\text{ V}$ ; see Figure 11
Drain Off Leakage, $I_D$ (Off)	$\pm 0.02$			nA typ	$V_S = \pm 10\text{ V}$ , $V_D = \pm 10\text{ V}$ ; see Figure 11
	$\pm 0.1$	$\pm 0.6$	$\pm 1$	nA max	
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.02$			nA typ	$V_S = V_D = \pm 10\text{ V}$ ; see Figure 12
	$\pm 0.1$	$\pm 0.6$	$\pm 1$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	2.5			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	65			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	80	95	110	ns max	$V_S = 10\text{ V}$ ; see Figure 18
$t_{OFF}$	80			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	100	115	135	ns max	$V_S = 10\text{ V}$ ; see Figure 18
Charge Injection	-0.3			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 19
Off Isolation	80			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 13
Channel-to-Channel Crosstalk	90			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 14
Total Harmonic Distortion + Noise	0.15			% typ	$R_L = 10\text{ k}\Omega$ , 5 V rms, $f = 20\text{ Hz}$ to 20 kHz; see Figure 17
-3 dB Bandwidth	1000			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 16
$C_S$ (Off)	0.9			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
	1.1			pF max	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)	1			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
	1.2			pF max	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ , $C_S$ (On)	2.6			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
	3			pF max	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$
			1.0	$\mu\text{A}$ max	Digital inputs = 0 V or $V_{DD}$
$I_{DD}$	220			$\mu\text{A}$ typ	Digital inputs = 5 V
			420	$\mu\text{A}$ max	
$I_{SS}$	0.001			$\mu\text{A}$ typ	Digital inputs = 0 V or $V_{DD}$
			1.0	$\mu\text{A}$ max	
$I_{SS}$	0.001			$\mu\text{A}$ typ	Digital inputs = 5 V
			1.0	$\mu\text{A}$ max	

<sup>1</sup> Guaranteed by design, not subject to production test.

## SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

Table 2.

Parameter	25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	300			$\Omega$ typ	$V_S = 0\text{ V}$ to $10\text{ V}$ , $I_S = -1\text{ mA}$ ; see Figure 15
	475	567	625	$\Omega$ max	$V_{DD} = 10.8\text{ V}$ , $V_{SS} = 0\text{ V}$
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	4.5			$\Omega$ typ	$V_S = 0\text{ V}$ to $10\text{ V}$ , $I_S = -1\text{ mA}$
	12	26	27	$\Omega$ max	
On Resistance Flatness ( $R_{FLAT(ON)}$ )	60			$\Omega$ typ	$V_S = 3\text{ V}/6\text{ V}/9\text{ V}$ , $I_S = -1\text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.02$			nA typ	$V_{DD} = 13.2\text{ V}$ , $V_{SS} = 0\text{ V}$
	$\pm 0.1$	$\pm 0.6$	$\pm 1$	nA max	$V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ ; see Figure 11
Drain Off Leakage, $I_D$ (Off)	$\pm 0.02$			nA typ	$V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ ; see Figure 11
	$\pm 0.1$	$\pm 0.6$	$\pm 1$	nA max	
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.02$			nA typ	$V_S = V_D = 1\text{ V}$ or $10\text{ V}$ ; see Figure 12
	$\pm 0.1$	$\pm 0.6$	$\pm 1$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.001			$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	3			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	80			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	105	125	140	ns max	$V_S = 8\text{ V}$ ; see Figure 18
$t_{OFF}$	90			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	115	140	165	ns max	$V_S = 8\text{ V}$ ; see Figure 18
Charge Injection	0			pC typ	$V_S = 6\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 19
Off Isolation	80			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 13
Channel-to-Channel Crosstalk	90			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 14
-3 dB Bandwidth	900			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 16
$C_S$ (Off)	1.2			pF typ	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
	1.4			pF max	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)	1.3			pF typ	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
	1.5			pF max	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ , $C_S$ (On)	3.2			pF typ	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
	3.9			pF max	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = 13.2\text{ V}$
			1.0	$\mu\text{A}$ max	Digital inputs = $0\text{ V}$ or $V_{DD}$
$I_{DD}$	220			$\mu\text{A}$ typ	Digital inputs = $5\text{ V}$
			420	$\mu\text{A}$ max	

<sup>1</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

Parameter	Rating
$V_{DD}$ to $V_{SS}$	35 V
$V_{DD}$ to GND	-0.3 V to +25 V
$V_{SS}$ to GND	+0.3 V to -25 V
Analog Inputs <sup>1</sup>	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs <sup>1</sup>	GND - 0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, S or D	100 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current per Channel, S or D	25 mA
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP, $\theta_{JA}$ Thermal Impedance (4-Layer Board)	112°C/W
Lead Temperature, Soldering	As per JEDEC J-STD-020

<sup>1</sup> Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating may be applied at any one time.

**Table 4. ADG1212-EP Truth Table**

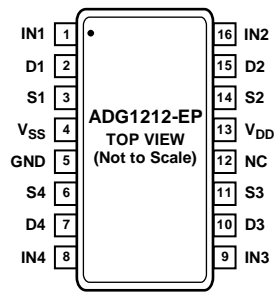
ADG1212-EP INx	Switch Condition
1	On
0	Off

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES  
 1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.

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Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN1	Logic Control Input.
2	D1	Drain Terminal. This pin can be an input or output.
3	S1	Source Terminal. This pin can be an input or output.
4	V <sub>SS</sub>	Most Negative Power Supply Potential.
5	GND	Ground (0 V) Reference.
6	S4	Source Terminal. This pin can be an input or output.
7	D4	Drain Terminal. This pin can be an input or output.
8	IN4	Logic Control Input.
9	IN3	Logic Control Input.
10	D3	Drain Terminal. This pin can be an input or output.
11	S3	Source Terminal. This pin can be an input or output.
12	NC	No Connection.
13	V <sub>DD</sub>	Most Positive Power Supply Potential.
14	S2	Source Terminal. This pin can be an input or output.
15	D2	Drain Terminal. This pin can be an input or output.
16	IN2	Logic Control Input.

### TYPICAL PERFORMANCE CHARACTERISTICS

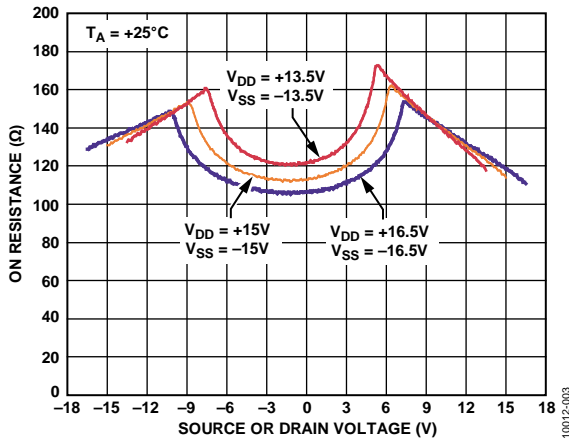


Figure 3. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Dual Supply

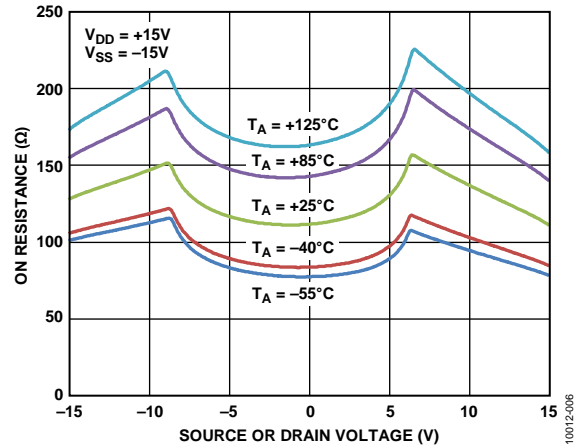


Figure 6. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, Dual Supply

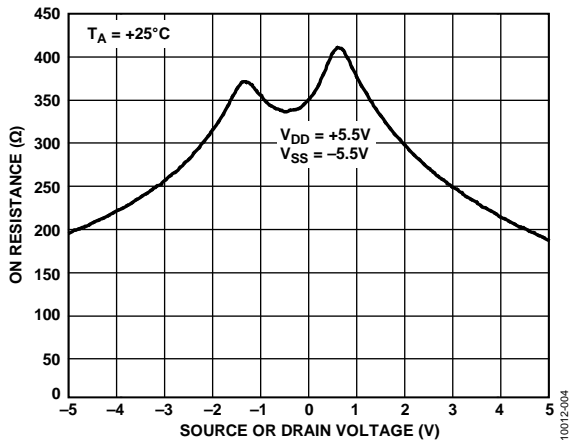


Figure 4. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Dual Supply

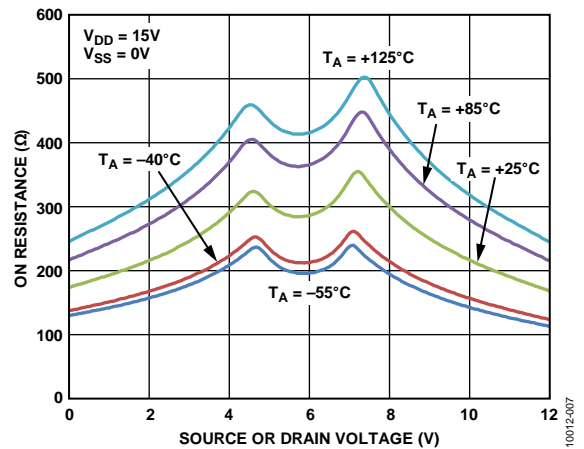


Figure 7. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, Single Supply

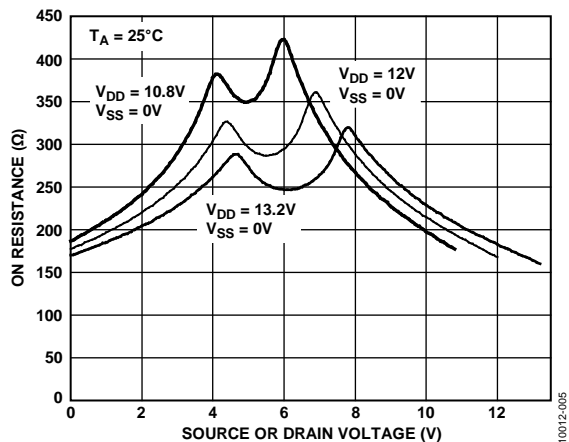


Figure 5. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Single Supply

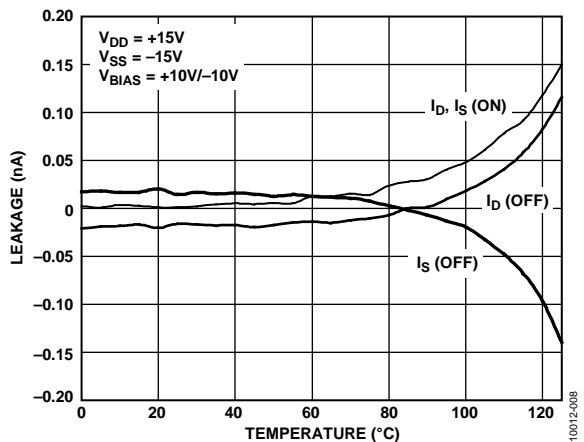


Figure 8. Leakage Currents as a Function of Temperature, Dual Supply

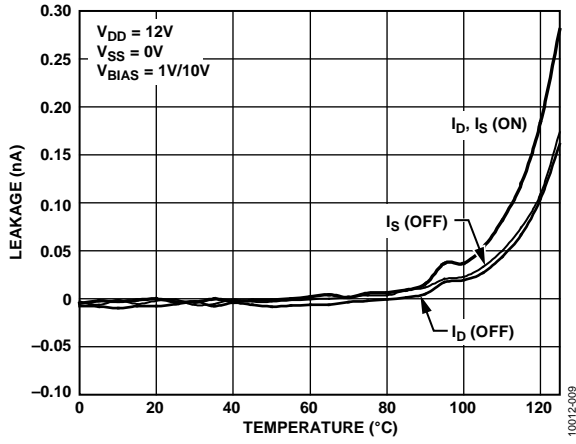


Figure 9. Leakage Currents as a Function of Temperature, Single Supply

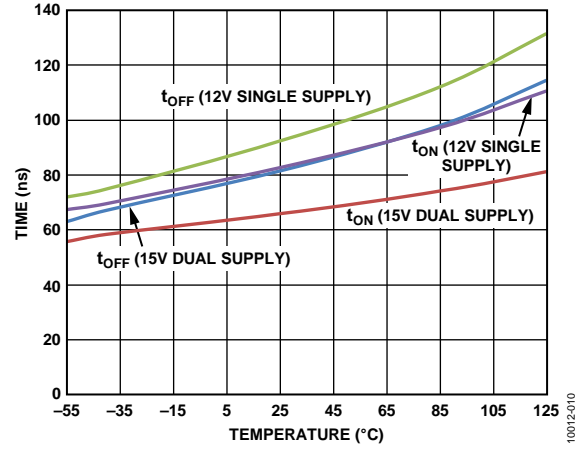


Figure 10.  $t_{ON}/t_{OFF}$  Times vs. Temperature



TEST CIRCUITS

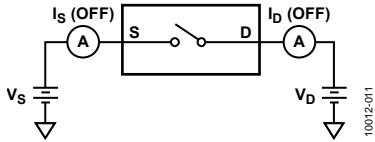


Figure 11. Off Leakage

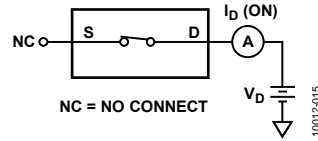


Figure 15. On Resistance

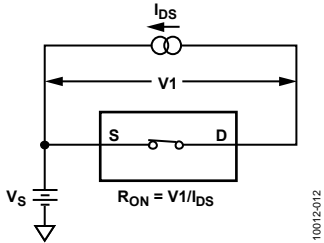
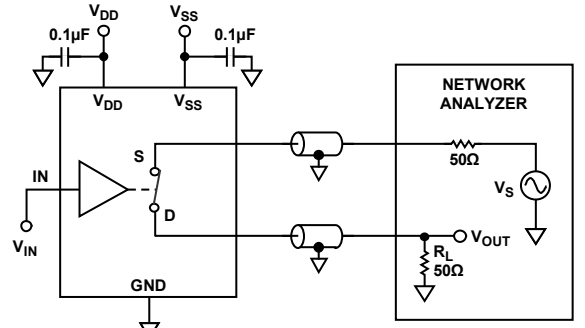
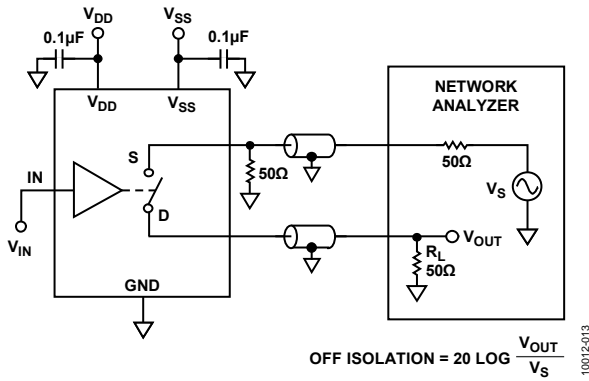


Figure 12. On Leakage



$$\text{INSERTION LOSS} = 20 \text{ LOG} \frac{V_{\text{OUT WITH SWITCH}}}{V_{\text{OUT WITHOUT SWITCH}}}$$

Figure 16. Bandwidth



$$\text{OFF ISOLATION} = 20 \text{ LOG} \frac{V_{\text{OUT}}}{V_s}$$

Figure 13. Off Isolation

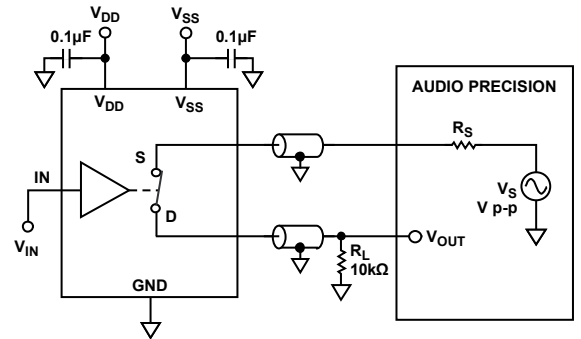
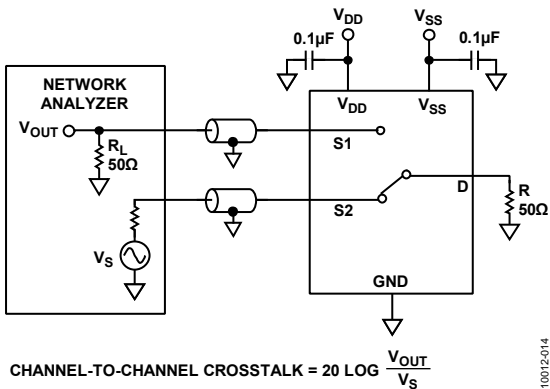


Figure 17. THD + Noise



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \text{ LOG} \frac{V_{\text{OUT}}}{V_s}$$

Figure 14. Channel-to-Channel Crosstalk

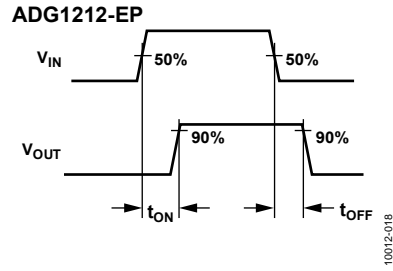
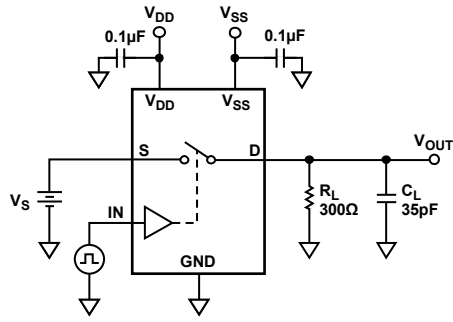


Figure 18. Switching Times

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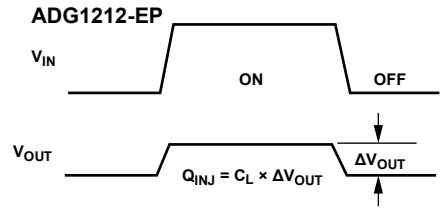
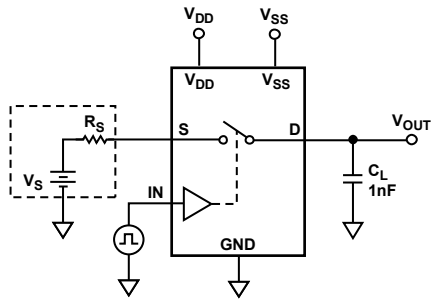
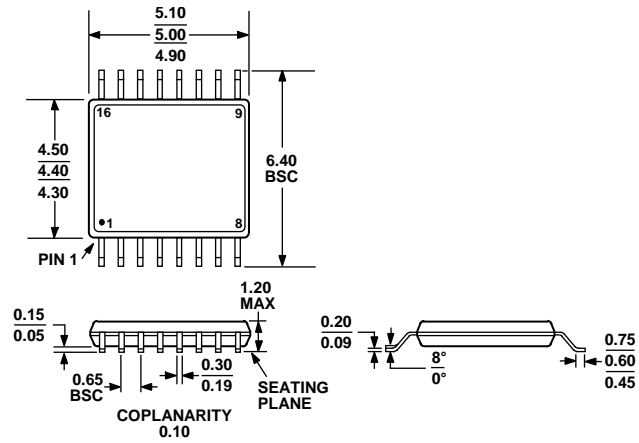


Figure 19. Charge Injection

10012-018

# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 20. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)  
 Dimensions shown in millimeters

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADG1212SRU-EP-RL7	-55°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1212SRUZ-EP-RL7	-55°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16

<sup>1</sup> Z = RoHS Compliant Part

**NOTES**