

# D45C12 (PNP), D44C12 (NPN)

## Complementary Silicon Power Transistor

The D45C12 and D44C12 are for general purpose driver or medium power output stages in CW or switching applications.

### Features

- Low Collector–Emitter Saturation Voltage – 0.5 V (Max)
- High  $f_t$  for Good Frequency Response
- Low Leakage Current
- Pb–Free Packages are Available\*

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	80	Vdc
Collector–Emitter Voltage	$V_{CES}$	90	Vdc
Emitter Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current – Continuous Peak (Note 1)	$I_C$	4.0 6.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ @ $T_A = 25^\circ\text{C}$	$P_D$	30 1.67	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–55 to 150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	4.2	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	75	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/8 in from Case for 5 Sec	$T_L$	275	$^\circ\text{C}$

1. Pulse Width  $\leq 6.0$  ms, Duty Cycle  $\leq 50\%$ .

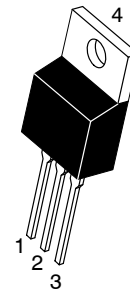
\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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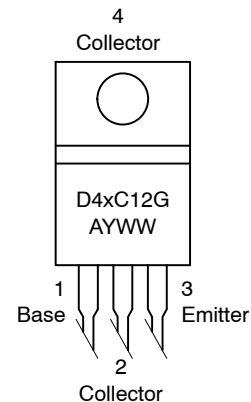
<http://onsemi.com>

## 4.0 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 80 VOLTS



TO-220AB  
CASE 221A  
STYLE 1

### MARKING DIAGRAM & PIN ASSIGNMENT



x = 4 or 5  
A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb–Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# D45C12 (PNP), D44C12 (NPN)

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
DC Current Gain (V <sub>CE</sub> = 1.0 Vdc, I <sub>C</sub> = 0.2 Adc) (V <sub>CE</sub> = 1.0 Vdc, I <sub>C</sub> = 1.0 Adc) (V <sub>CE</sub> = 1.0 Vdc, I <sub>C</sub> = 2.0 Adc)	h <sub>FE</sub>	40 20 20	120 – –	–

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CES</sub> , V <sub>BE</sub> = 0)	I <sub>CES</sub>	–	–	0.1	μA
Emitter Cutoff Current (V <sub>EB</sub> = 5.0 Vdc)	I <sub>EBO</sub>	–	–	10	μA

### ON CHARACTERISTICS

Collector–Emitter Saturation Voltage (I <sub>C</sub> = 1.0 Adc, I <sub>B</sub> = 50 mAdc)	V <sub>CE(sat)</sub>	–	0.135	0.5	Vdc
Base–Emitter Saturation Voltage (I <sub>C</sub> = 1.0 Adc, I <sub>B</sub> = 100 mAdc)	V <sub>BE(sat)</sub>	–	0.85	1.3	Vdc

### DYNAMIC CHARACTERISTICS

Collector Capacitance (V <sub>CB</sub> = 10 Vdc, f = 1.0 MHz)	C <sub>cb</sub>	–	125	–	pF
Gain Bandwidth Product (I <sub>C</sub> = 20 mA, V <sub>CE</sub> = 4.0 Vdc, f = 20 MHz)	f <sub>T</sub>	–	40	–	MHz

### SWITCHING TIMES

Delay and Rise Times (I <sub>C</sub> = 1.0 Adc, I <sub>B1</sub> = 0.1 Adc)	t <sub>d</sub> + t <sub>r</sub>	–	50	75	ns
Storage Time (I <sub>C</sub> = 1.0 Adc, I <sub>B1</sub> = I <sub>B2</sub> = 0.1 Adc)	t <sub>s</sub>	–	350	550	ns
Fall Time (I <sub>C</sub> = 1.0 Adc, I <sub>B1</sub> = I <sub>B2</sub> = 0.1 Adc)	t <sub>f</sub>	–	50	75	ns

### ORDERING INFORMATION

Device	Package	Shipping†
D45C12	TO–220AB	50 Units / Rail
D45C12G	TO–220AB (Pb–Free)	
D44C12	TO–220AB	
D44C12G	TO–220AB (Pb–Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

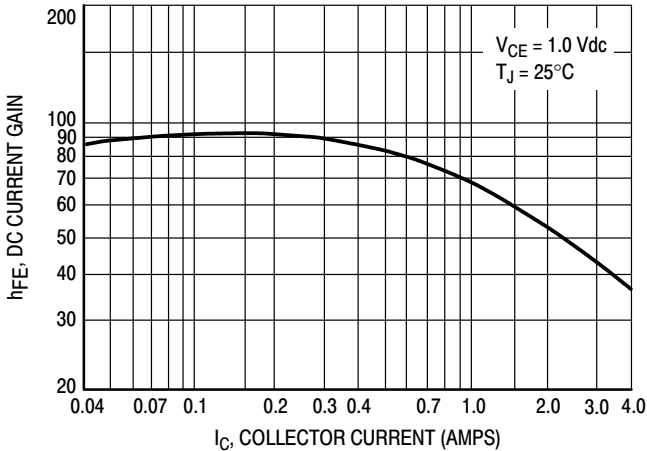


Figure 1. Typical DC Current Gain

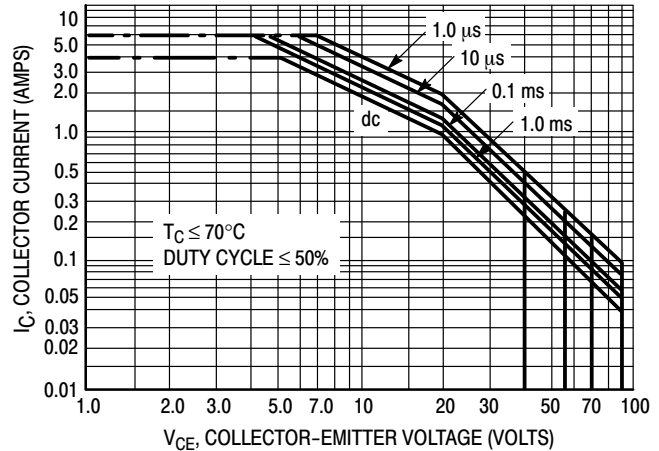
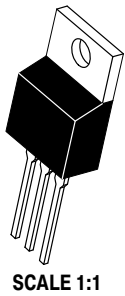


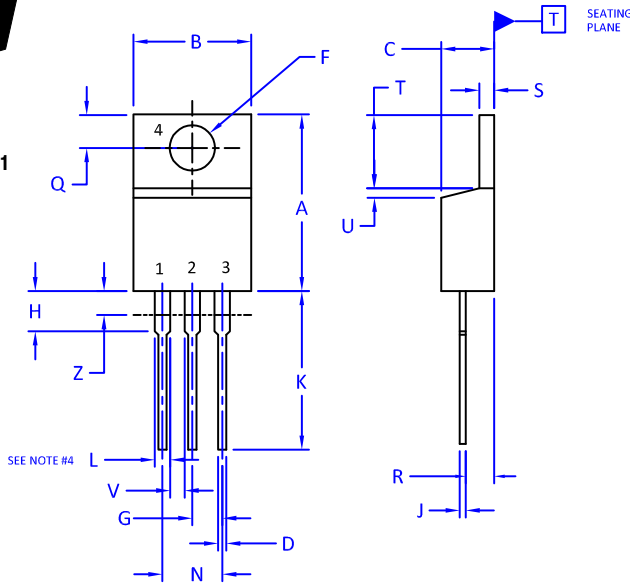
Figure 2. Maximum Rated Forward Bias Safe Operating Area

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



## TO-220 CASE 221A ISSUE AK

DATE 13 JAN 2022



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:

- PIN 1. BASE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 2:

- PIN 1. BASE
- 2. EMITTER
- 3. COLLECTOR
- 4. EMITTER

STYLE 3:

- PIN 1. CATHODE
- 2. ANODE
- 3. GATE
- 4. ANODE

STYLE 4:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. MAIN TERMINAL 2

STYLE 5:

- PIN 1. GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN

STYLE 6:

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. CATHODE

STYLE 7:

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. ANODE

STYLE 8:

- PIN 1. CATHODE
- 2. ANODE
- 3. EXTERNAL TRIP/DELAY
- 4. ANODE

STYLE 9:

- PIN 1. GATE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 10:

- PIN 1. GATE
- 2. SOURCE
- 3. DRAIN
- 4. SOURCE

STYLE 11:

- PIN 1. DRAIN
- 2. SOURCE
- 3. GATE
- 4. SOURCE

STYLE 12:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. NOT CONNECTED

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