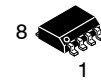


# Boost Regulators, 1.5 A, 280 kHz/560 kHz

## CS5171, CS5172, CS5173, CS5174



SOIC-8  
D SUFFIX  
CASE 751

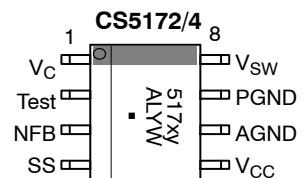
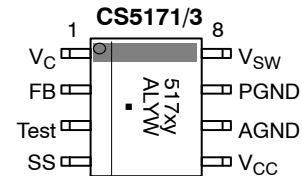
The CS5171/2/3/4 products are 280 kHz/560 kHz switching regulators with a high efficiency, 1.5 A integrated switch. These parts operate over a wide input voltage range, from 2.7 V to 30 V. The flexibility of the design allows the chips to operate in most power supply configurations, including boost, flyback, forward, inverting, and SEPIC. The ICs utilize current mode architecture, which allows excellent load and line regulation, as well as a practical means for limiting current. Combining high frequency operation with a highly integrated regulator circuit results in an extremely compact power supply solution. The circuit design includes provisions for features such as frequency synchronization, shutdown, and feedback controls for either positive or negative voltage regulation. These parts are pin-to-pin compatible with LT1372/1373.

Part Number	Frequency	Feedback Voltage Polarity
CS5171	280 kHz	positive
CS5172	280 kHz	negative
CS5173	560 kHz	positive
CS5174	560 kHz	negative

### Features

- Integrated Power Switch: 1.5 A Guaranteed
- Wide Input Range: 2.7 V to 30 V
- High Frequency Allows for Small Components
- Minimum External Components
- Easy External Synchronization
- Built in Overcurrent Protection
- Frequency Foldback Reduces Component Stress During an Overcurrent Condition
- Thermal Shutdown with Hysteresis
- Regulates Either Positive or Negative Output Voltages
- Shut Down Current: 50  $\mu$ A Maximum
- Pin-to-Pin Compatible with LT1372/1373
- Wide Temperature Range
  - ◆ Industrial Grade: -40°C to 125°C
  - ◆ Commercial Grade: 0°C to 125°C
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MARKING DIAGRAM AND PIN CONNECTIONS

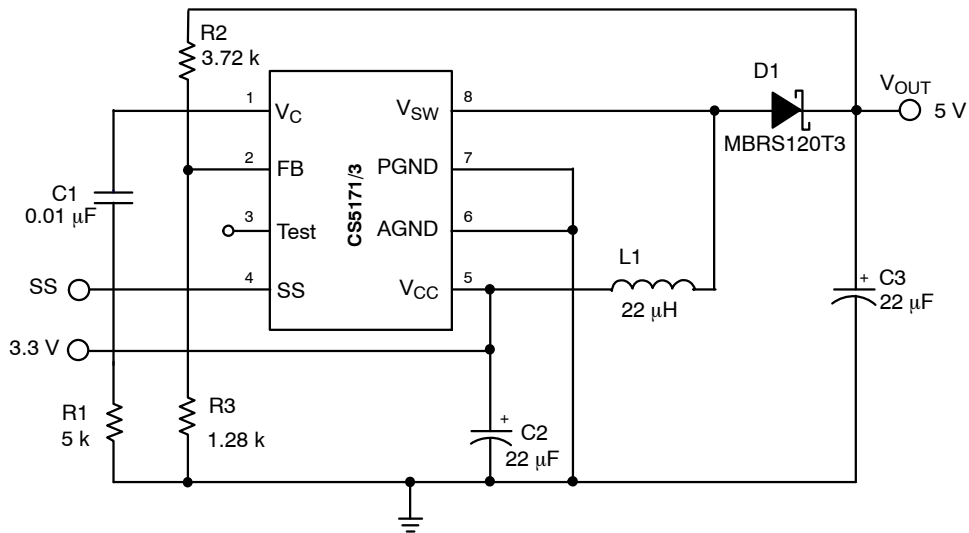


517xy = Device Code  
 x= 1, 2, 3, or 4  
 y= E, G  
 A = Assembly Location  
 L = Wafer Lot  
 Y = Year  
 W = Work Week  
 ■ = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 20 of this data sheet.

## CS5171, CS5172, CS5173, CS5174



**Figure 1. Applications Diagram**

### MAXIMUM RATINGS

Rating	Value	Unit
Junction Temperature Range, $T_J$	-40 to +150	°C
Storage Temperature Range, $T_{STORAGE}$	-65 to +150	°C
Package Thermal Resistance, Junction-to-Case, $R_{\theta JC}$ Junction-to-Ambient, $R_{\theta JA}$	45 165	°C/W °C/W
Lead Temperature Soldering: Reflow (Note 1)	260 Peak	°C
ESD, Human Body Model	1.2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. 60 second maximum above 183°C.

### MAXIMUM RATINGS

Pin Name	Pin Symbol	$V_{MAX}$	$V_{MIN}$	$I_{SOURCE}$	$I_{SINK}$
IC Power Input	$V_{CC}$	35 V	-0.3 V	N/A	200 mA
Shutdown/Sync	SS	30 V	-0.3 V	1.0 mA	1.0 mA
Loop Compensation	$V_C$	6.0 V	-0.3 V	10 mA	10 mA
Voltage Feedback Input	FB (CS5171/3 only)	10 V	-0.3 V	1.0 mA	1.0 mA
Negative Feedback Input (transient, 10 ms)	NFB (CS5172/4 only)	-10 V	10 V	1.0 mA	1.0 mA
Test Pin	Test	6.0 V	-0.3 V	1.0 mA	1.0 mA
Power Ground	PGND	0.3 V	-0.3 V	4 A	10 mA
Analog Ground	AGND	0 V	0 V	N/A	10 mA
Switch Input	$V_{SW}$	40 V	-0.3 V	10 mA	3.0 A

# CS5171, CS5172, CS5173, CS5174

**ELECTRICAL CHARACTERISTICS** (2.7 V < V<sub>CC</sub> < 30 V; Industrial Grade: -40°C < T<sub>J</sub> < 125°C; Commercial Grade: 0°C < T<sub>J</sub> < 125°C; For all CS5171/2/3/4 specifications unless otherwise stated.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
<b>Positive and Negative Error Amplifiers</b>					
FB Reference Voltage (CS5171/3 only)	V <sub>C</sub> tied to FB; measure at FB	1.246	1.276	1.300	V
NFB Reference Voltage (CS5172/4 only)	V <sub>C</sub> = 1.25 V	-2.55	-2.45	-2.35	V
FB Input Current (CS5171/3 only)	FB = V <sub>REF</sub>	-1.0	0.1	1.0	μA
NFB Input Current (CS5172/4 only)	NFB = NV <sub>REF</sub>	-16	-10	-5.0	μA
FB Reference Voltage Line Regulation (CS5171/3 only)	V <sub>C</sub> = FB	-	0.01	0.03	%/V
NFB Reference Voltage Line Regulation (CS5172/4 only)	V <sub>C</sub> = 1.25 V	-	0.01	0.05	%/V
Positive Error Amp Transconductance	I <sub>VC</sub> = ± 25 μA	300	550	800	μMho
Negative Error Amp Transconductance	I <sub>VC</sub> = ± 5 μA	115	160	225	μMho
Positive Error Amp Gain	(Note 2)	200	500	-	V/V
Negative Error Amp Gain	(Note 2)	100	180	320	V/V
V <sub>C</sub> Source Current	FB = 1.0 V or NFB = -1.9 V, V <sub>C</sub> = 1.25 V	25	50	90	μA
V <sub>C</sub> Sink Current	FB = 1.5 V or NFB = -3.1 V, V <sub>C</sub> = 1.25 V	200	625	1500	μA
V <sub>C</sub> High Clamp Voltage	FB = 1.0 V or NFB = -1.9 V; V <sub>C</sub> sources 25 μA	1.5	1.7	1.9	V
V <sub>C</sub> Low Clamp Voltage	FB = 1.5 V or NFB = -3.1 V, V <sub>C</sub> sinks 25 μA	0.25	0.50	0.65	V
V <sub>C</sub> Threshold	Reduce V <sub>C</sub> from 1.5 V until switching stops	0.75	1.05	1.30	V

## Oscillator

Base Operating Frequency	CS5171/2, FB = 1 V or NFB = -1.9 V	230	280	310	kHz
Reduced Operating Frequency	CS5171/2, FB = 0 V or NFB = 0 V	30	52	120	kHz
Maximum Duty Cycle	CS5171/2	90	94	-	%
Base Operating Frequency	CS5173/4, FB = 1 V or NFB = -1.9 V	460	560	620	kHz
Reduced Operating Frequency	CS5173/4, FB = 0 V or NFB = 0 V	60	104	160	kHz
Maximum Duty Cycle	CS5173/4	82	90	-	%
NFB Frequency Shift Threshold	Frequency drops to reduced operating frequency	-0.80	-0.65	-0.50	V
FB Frequency Shift Threshold	Frequency drops to reduced operating frequency	0.36	0.40	0.44	V

## Sync/ Shutdown

Sync Range	CS5171/2	320	-	500	kHz
Sync Range	CS5173/4	640	-	1000	kHz
Sync Pulse Transition Threshold	Rise time = 20 ns	2.5	-	-	V
SS Bias Current	SS = 0 V SS = 3.0 V	-15 -	-3.0 3.0	- 8.0	μA μA
Shutdown Threshold	-	0.50	0.85	1.20	V
Shutdown Delay	2.7 V ≤ V <sub>CC</sub> ≤ 12 V 12 V < V <sub>CC</sub> ≤ 30 V	12 12	80 36	350 200	μs μs

2. Guaranteed by design, not 100% tested in production.

# CS5171, CS5172, CS5173, CS5174

**ELECTRICAL CHARACTERISTICS** (2.7 V < V<sub>CC</sub> < 30 V; Industrial Grade: -40°C < T<sub>J</sub> < 125°C; Commercial Grade: 0°C < T<sub>J</sub> < 125°C; For all CS5171/2/3/4 specifications unless otherwise stated.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
<b>Power Switch</b>					
Switch Saturation Voltage	I <sub>SWITCH</sub> = 1.5 A, (Note 3)	-	0.8	1.4	V
	I <sub>SWITCH</sub> = 1.0 A, 0°C ≤ T <sub>J</sub> ≤ 85°C	-	0.55	-	V
	I <sub>SWITCH</sub> = 1.0 A, -40°C ≤ T <sub>J</sub> ≤ 0°C	-	0.75	-	V
	I <sub>SWITCH</sub> = 10 mA	-	0.09	0.45	V
Switch Current Limit	50% duty cycle, (Note 3)	1.6	1.9	2.4	A
	80% duty cycle, (Note 3)	1.5	1.7	2.2	A
Minimum Pulse Width	FB = 0 V or NFB = 0 V, I <sub>SW</sub> = 4.0 A, (Note 3)	200	250	300	ns
ΔI <sub>CC</sub> / ΔI <sub>SW</sub>	2.7 V ≤ V <sub>CC</sub> ≤ 12 V, 10 mA ≤ I <sub>SW</sub> ≤ 1.0 A	-	10	30	mA/A
	12 V < V <sub>CC</sub> ≤ 30 V, 10 mA ≤ I <sub>SW</sub> ≤ 1.0 A	-	-	100	mA/A
	2.7 V ≤ V <sub>CC</sub> ≤ 12 V, 10 mA ≤ I <sub>SW</sub> ≤ 1.5 A, (Note 3)	-	17	30	mA/A
	12 V < V <sub>CC</sub> ≤ 30 V, 10 mA ≤ I <sub>SW</sub> ≤ 1.5 A, (Note 3)	-	-	100	mA/A
Switch Leakage	V <sub>SW</sub> = 40 V, V <sub>CC</sub> = 0V	-	2.0	100	μA

## General

Operating Current	I <sub>SW</sub> = 0	-	5.5	8.0	mA
Shutdown Mode Current	V <sub>C</sub> < 0.8 V, SS = 0 V, 2.7 V ≤ V <sub>CC</sub> ≤ 12 V	-	12	60	μA
	V <sub>C</sub> < 0.8 V, SS = 0 V, 12 V ≤ V <sub>CC</sub> ≤ 30 V	-	-	100	μA
Minimum Operation Input Voltage	V <sub>SW</sub> switching, maximum I <sub>SW</sub> = 10 mA	-	2.45	2.70	V
Thermal Shutdown	(Note 3)	150	180	210	°C
Thermal Hysteresis	(Note 3)	-	25	-	°C

3. Guaranteed by design, not 100% tested in production.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## PACKAGE PIN DESCRIPTION

Package Pin #	Pin Symbol	Function
1	V <sub>C</sub>	Loop compensation pin. The V <sub>C</sub> pin is the output of the error amplifier and is used for loop compensation, current limit and soft start. Loop compensation can be implemented by a simple RC network as shown in the application diagram on page 2 as R1 and C1.
2 (CS5171/3 only)	FB	Positive regulator feedback pin. This pin senses a positive output voltage and is referenced to 1.276 V. When the voltage at this pin falls below 0.4 V, chip switching frequency reduces to 20% of the nominal frequency.
2 (CS5172/4) 3 CS5171/3)	Test	These pins are connected to internal test logic and should either be left floating or tied to ground. Connection to a voltage between 2 V and 6 V shuts down the internal oscillator and leaves the power switch running.
3 (CS5172/4)	NFB	Negative feedback pin. This pin senses a negative output voltage and is referenced to -2.5 V. When the voltage at this pin goes above -0.65 V, chip switching frequency reduces to 20% of the nominal frequency.
4	SS	Synchronization and shutdown pin. This pin may be used to synchronize the part to nearly twice the base frequency. A TTL low will shut the part down and put it into low current mode. If synchronization is not used, this pin should be either tied high or left floating for normal operation.
5	V <sub>CC</sub>	Input power supply pin. This pin supplies power to the part and should have a bypass capacitor connected to AGND.

# CS5171, CS5172, CS5173, CS5174

## PACKAGE PIN DESCRIPTION

Package Pin #	Pin Symbol	Function
6	AGND	Analog ground. This pin provides a clean ground for the controller circuitry and should not be in the path of large currents. The output voltage sensing resistors should be connected to this ground pin. This pin is connected to the IC substrate.
7	PGND	Power ground. This pin is the ground connection for the emitter of the power switching transistor. Connection to a good ground plane is essential.
8	V <sub>SW</sub>	High current switch pin. This pin connects internally to the collector of the power switch. The open voltage across the power switch can be as high as 40 V. To minimize radiation, use a trace as short as practical.

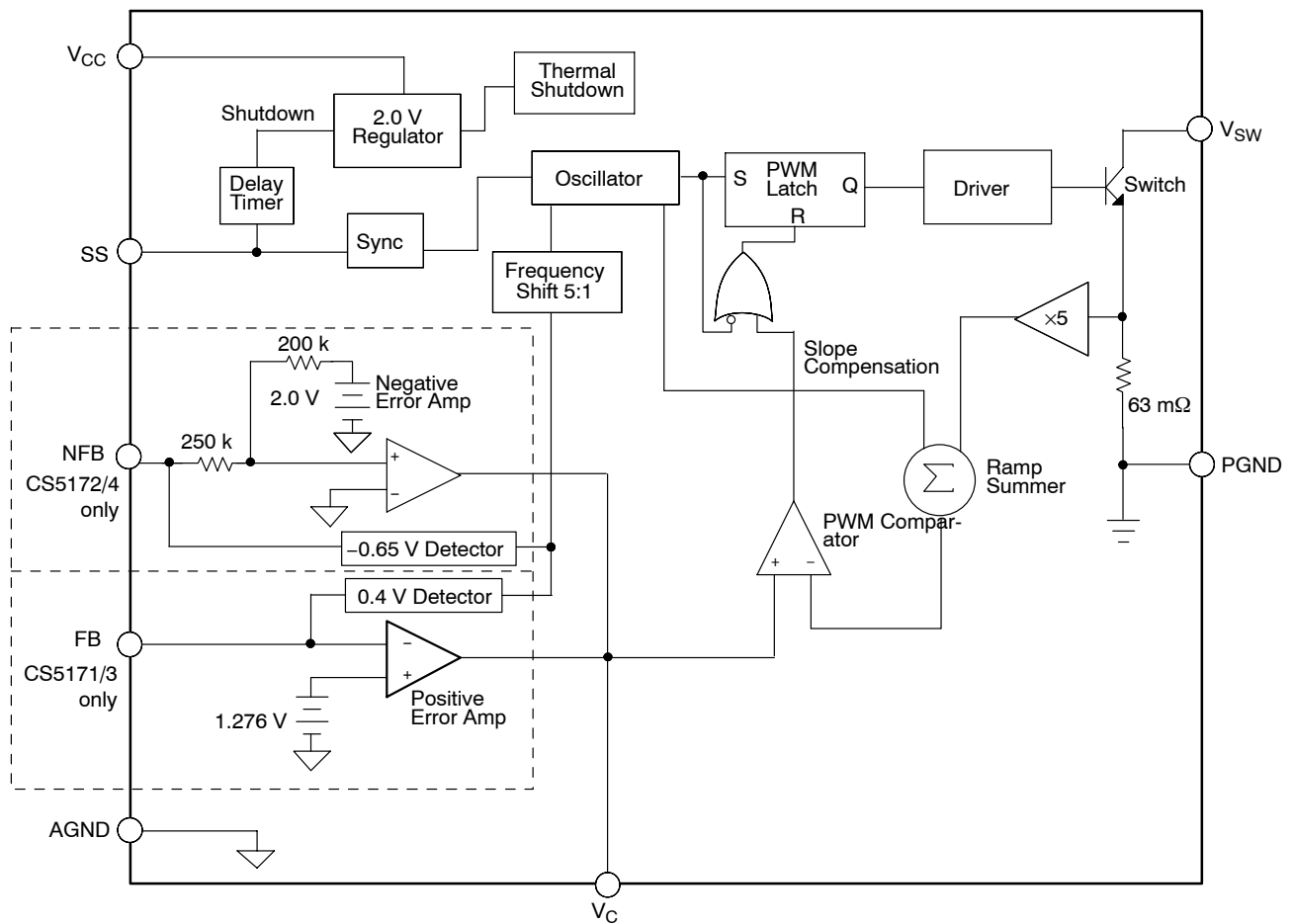


Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

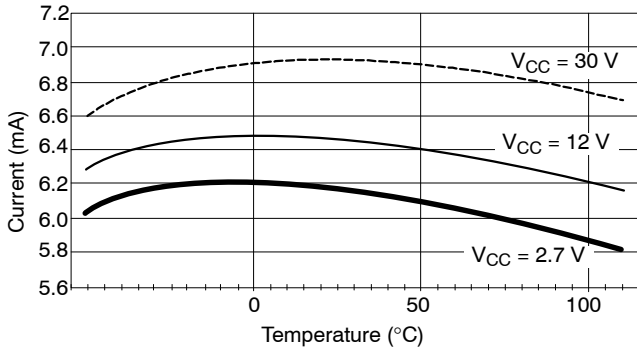


Figure 3.  $I_{CC}$  (No Switching) vs. Temperature

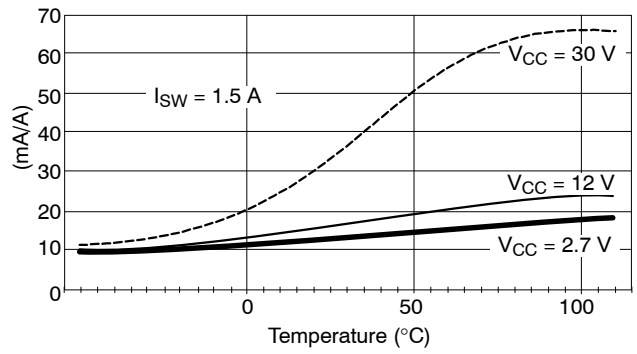


Figure 4.  $\Delta I_{CC} / \Delta I_{SW}$  vs. Temperature

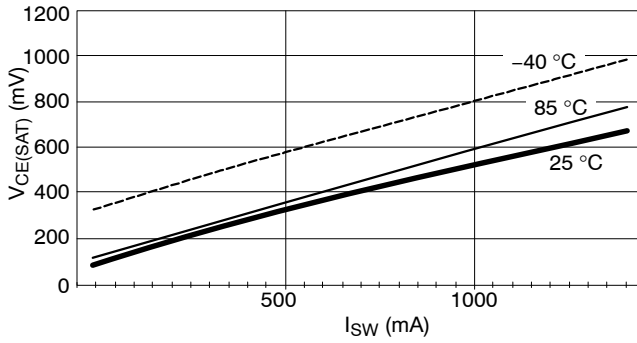


Figure 5.  $V_{CE(SAT)}$  vs.  $I_{SW}$

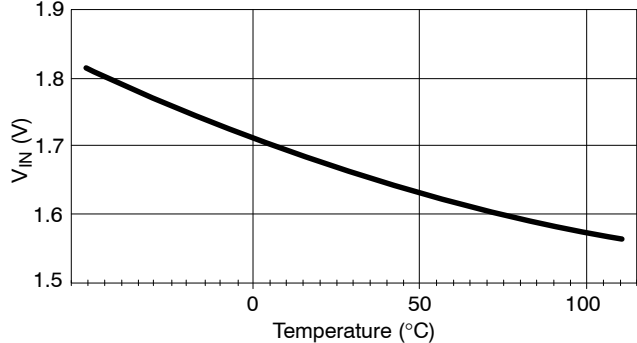


Figure 6. Minimum Input Voltage vs. Temperature

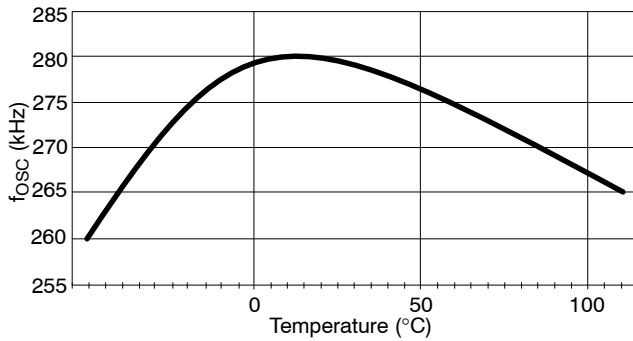


Figure 7. Switching Frequency vs. Temperature (CS5171/2 only)

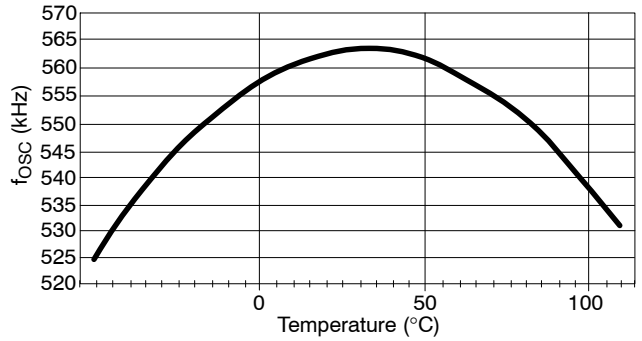


Figure 8. Switching Frequency vs. Temperature (CS5173/4 only)

TYPICAL PERFORMANCE CHARACTERISTICS

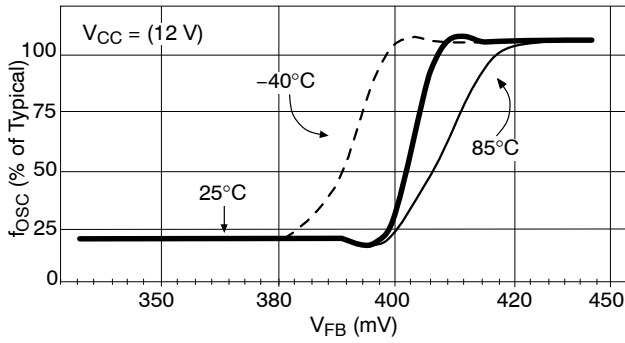


Figure 9. Switching Frequency vs.  $V_{FB}$  (CS5171/3 only)

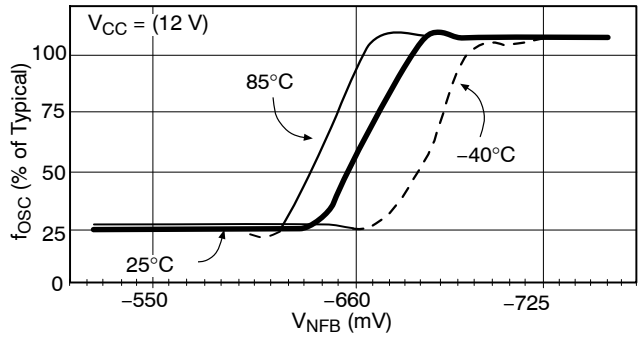


Figure 10. Switching Frequency vs.  $V_{NFB}$  (CS5172/4 only)

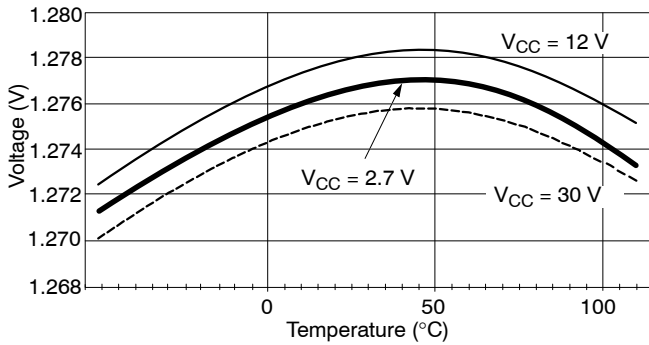


Figure 11. Reference Voltage vs. Temperature (CS5171/3 only)

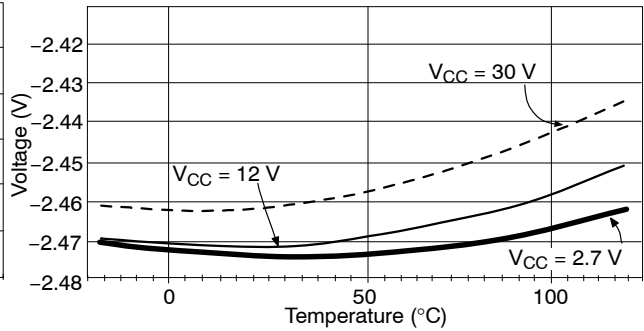


Figure 12. Reference Voltage vs. Temperature (CS5172/4 only)

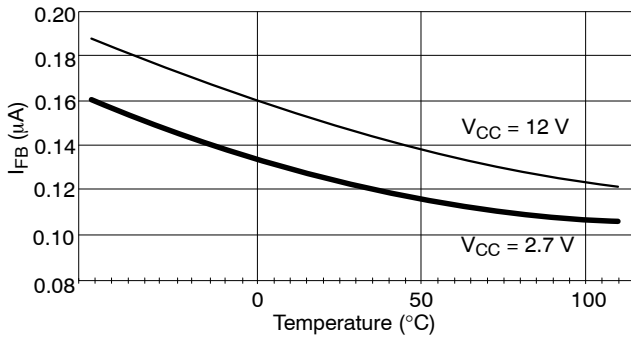


Figure 13.  $I_{FB}$  vs. Temperature (CS5171/3 only)

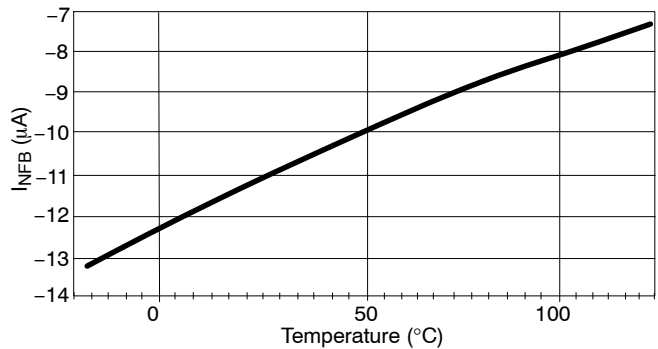


Figure 14.  $I_{NFB}$  vs. Temperature (CS5172/4 only)

TYPICAL PERFORMANCE CHARACTERISTICS

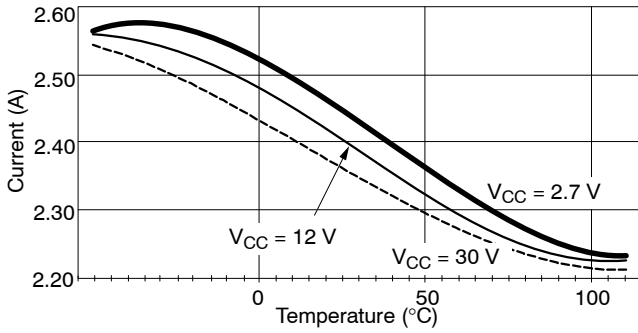


Figure 15. Current Limit vs. Temperature

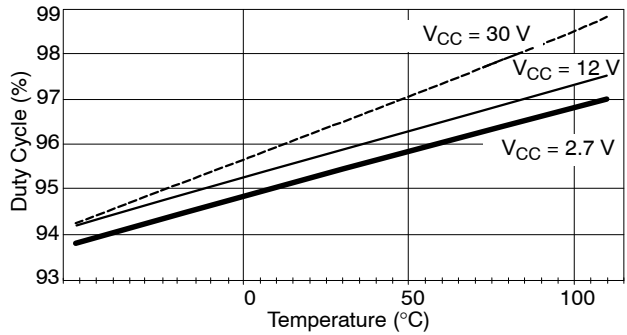


Figure 16. Maximum Duty Cycle vs. Temperature

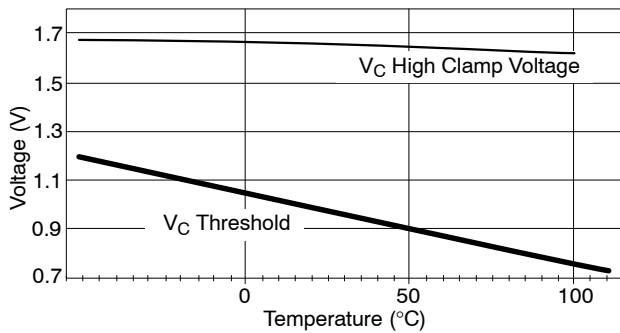


Figure 17.  $V_C$  Threshold and High Clamp Voltage vs. Temperature

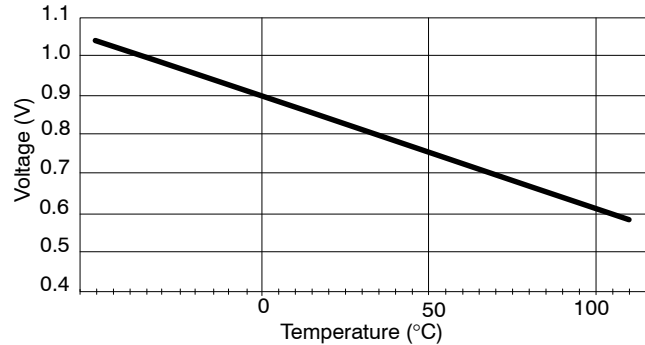


Figure 18. Shutdown Threshold vs. Temperature

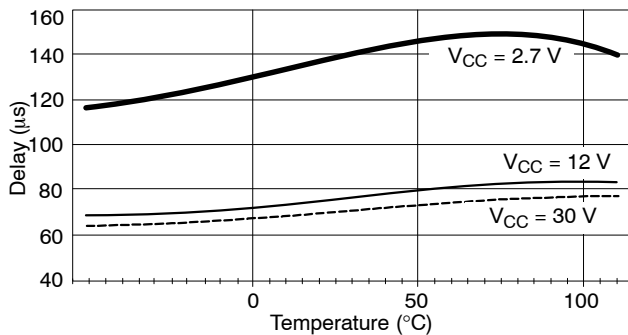


Figure 19. Shutdown Delay vs. Temperature

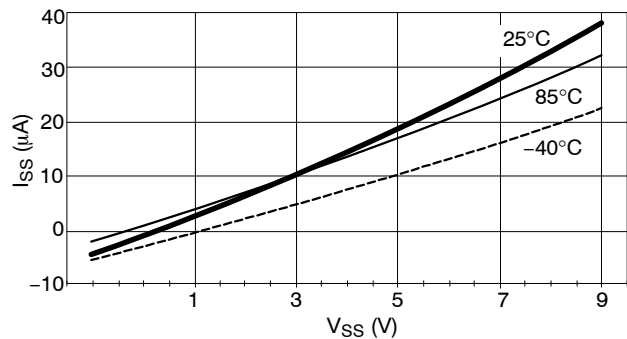


Figure 20.  $I_{SS}$  vs.  $V_{SS}$



TYPICAL PERFORMANCE CHARACTERISTICS

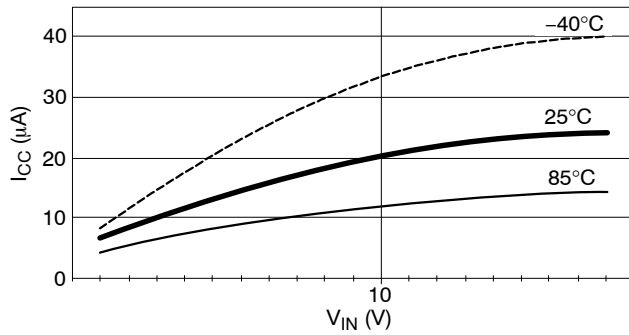


Figure 21.  $I_{CC}$  vs.  $V_{IN}$  During Shutdown

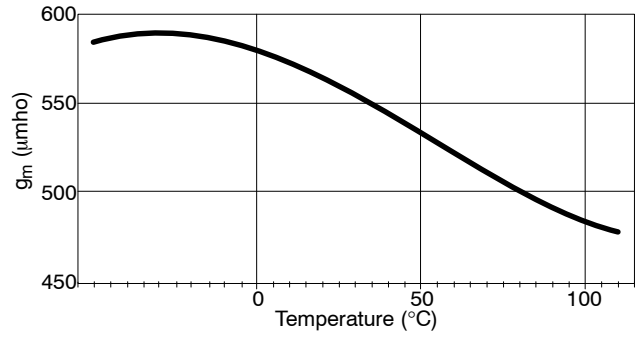


Figure 22. Error Amplifier Transconductance vs. Temperature (CS5171/3 only)

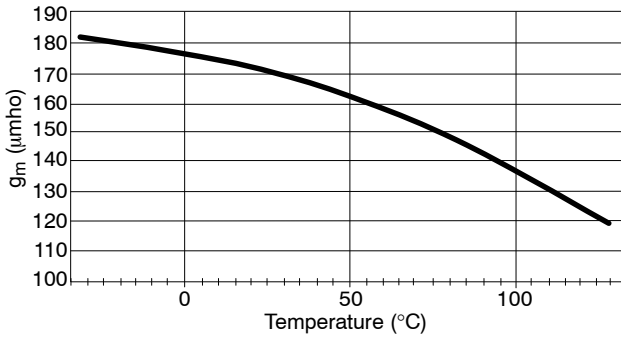


Figure 23. Negative Error Amplifier Transconductance vs. Temperature (CS5172/4 only)

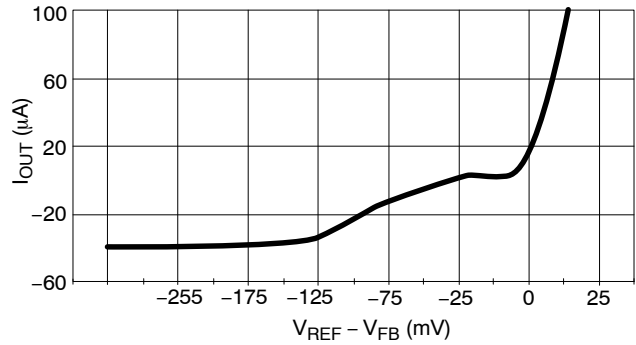


Figure 24. Error Amplifier  $I_{OUT}$  vs.  $V_{FB}$  (CS5171/3 only)

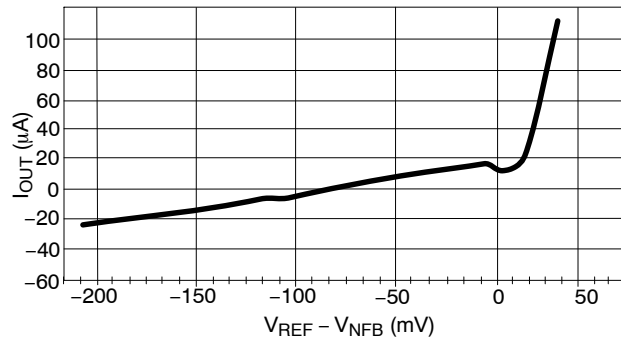


Figure 25. Error Amplifier  $I_{OUT}$  vs.  $V_{NFB}$  (CS5172/4 only)

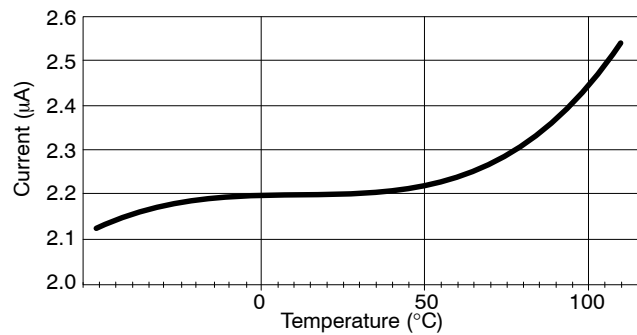


Figure 26. Switch Leakage vs. Temperature

APPLICATIONS INFORMATION

THEORY OF OPERATION

Current Mode Control

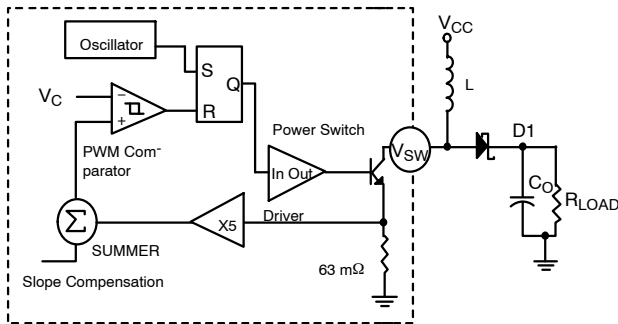


Figure 27. Current Mode Control Scheme

The CS517x family incorporates a current mode control scheme, in which the PWM ramp signal is derived from the power switch current. This ramp signal is compared to the output of the error amplifier to control the on-time of the power switch. The oscillator is used as a fixed-frequency clock to ensure a constant operational frequency. The resulting control scheme features several advantages over conventional voltage mode control. First, derived directly from the inductor, the ramp signal responds immediately to line voltage changes. This eliminates the delay caused by the output filter and error amplifier, which is commonly found in voltage mode controllers. The second benefit comes from inherent pulse-by-pulse current limiting by merely clamping the peak switching current. Finally, since current mode commands an output current rather than voltage, the filter offers only a single pole to the feedback loop. This allows both a simpler compensation and a higher gain-bandwidth over a comparable voltage mode circuit.

Without discrediting its apparent merits, current mode control comes with its own peculiar problems, mainly, subharmonic oscillation at duty cycles over 50%. The CS517x family solves this problem by adopting a slope compensation scheme in which a fixed ramp generated by the oscillator is added to the current ramp. A proper slope rate is provided to improve circuit stability without sacrificing the advantages of current mode control.

Oscillator and Shutdown

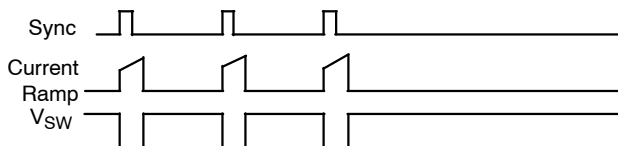


Figure 28. Timing Diagram of Sync and Shutdown

The oscillator is trimmed to guarantee an 18% frequency accuracy. The output of the oscillator turns on the power switch at a frequency of 280 kHz (CS5171/2) or 560 kHz (CS5173/4), as shown in Figure 27. The power switch is turned off by the output of the PWM Comparator.

A TTL-compatible sync input at the SS pin is capable of syncing up to 1.8 times the base oscillator frequency. As shown in Figure 28, in order to sync to a higher frequency, a positive transition turns on the power switch before the output of the oscillator goes high, thereby resetting the oscillator. The sync operation allows multiple power supplies to operate at the same frequency.

A sustained logic low at the SS pin will shut down the IC and reduce the supply current.

An additional feature includes frequency shift to 20% of the nominal frequency when either the NFB or FB pins trigger the threshold. During power up, overload, or short circuit conditions, the minimum switch on-time is limited by the PWM comparator minimum pulse width. Extra switch off-time reduces the minimum duty cycle to protect external components and the IC itself.

As previously mentioned, this block also produces a ramp for the slope compensation to improve regulator stability.

Error Amplifier

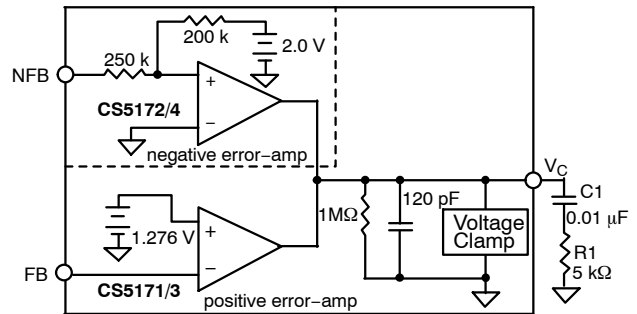


Figure 29. Error Amplifier Equivalent Circuit

For CS5172/4, the NFB pin is internally referenced to -2.5 V with approximately a 250 kΩ input impedance. For CS5171/3, the FB pin is directly connected to the inverting input of the positive error amplifier, whose non-inverting input is fed by the 1.276 V reference. Both amplifiers are transconductance amplifiers with a high output impedance of approximately 1 MΩ, as shown in Figure 29. The V<sub>C</sub> pin is connected to the output of the error amplifiers and is internally clamped between 0.5 V and 1.7 V. A typical connection at the V<sub>C</sub> pin includes a capacitor in series with a resistor to ground, forming a pole/zero for loop compensation.

An external shunt can be connected between the V<sub>C</sub> pin and ground to reduce its clamp voltage. Consequently, the current limit of the internal power transistor current is reduced from its nominal value.

**Switch Driver and Power Switch**

The switch driver receives a control signal from the logic section to drive the output power switch. The switch is grounded through emitter resistors (63 mΩ total) to the PGND pin. PGND is not connected to the IC substrate so that switching noise can be isolated from the analog ground. The peak switching current is clamped by an internal circuit. The clamp current is guaranteed to be greater than 1.5 A and varies with duty cycle due to slope compensation. The power switch can withstand a maximum voltage of 40 V on the collector (V<sub>SW</sub> pin). The saturation voltage of the switch is typically less than 1 V to minimize power dissipation.

**Short Circuit Condition**

When a short circuit condition happens in a boost circuit, the inductor current will increase during the whole switching cycle, causing excessive current to be drawn from the input power supply. Since control ICs don't have the means to limit load current, an external current limit circuit (such as a fuse or relay) has to be implemented to protect the load, power supply and ICs.

In other topologies, the frequency shift built into the IC prevents damage to the chip and external components. This feature reduces the minimum duty cycle and allows the transformer secondary to absorb excess energy before the switch turns back on.

approximately 1.5 V, the internal power switch briefly turns on. This is a part of the CS517x's normal operation. The turn-on of the power switch accounts for the initial current swing.

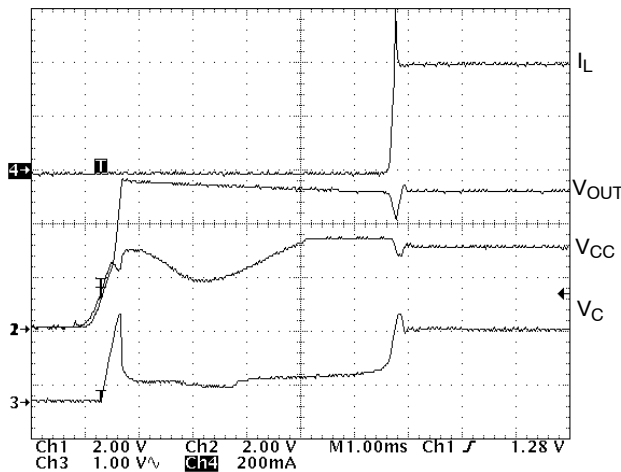
When the V<sub>C</sub> pin voltage rises above the threshold, the internal power switch starts to switch and a voltage pulse can be seen at the V<sub>SW</sub> pin. Detecting a low output voltage at the FB pin, the built-in frequency shift feature reduces the switching frequency to a fraction of its nominal value, reducing the minimum duty cycle, which is otherwise limited by the minimum on-time of the switch. The peak current during this phase is clamped by the internal current limit.

When the FB pin voltage rises above 0.4 V, the frequency increases to its nominal value, and the peak current begins to decrease as the output approaches the regulation voltage. The overshoot of the output voltage is prevented by the active pull-on, by which the sink current of the error amplifier is increased once an overvoltage condition is detected. The overvoltage condition is defined as when the FB pin voltage is 50 mV greater than the reference voltage.

**COMPONENT SELECTION**

**Frequency Compensation**

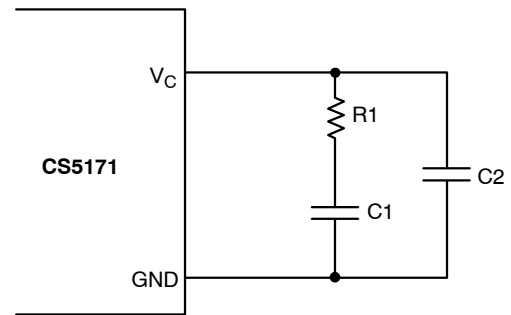
The goal of frequency compensation is to achieve desirable transient response and DC regulation while ensuring the stability of the system. A typical compensation network, as shown in Figure 31, provides a frequency response of two poles and one zero. This frequency response is further illustrated in the Bode plot shown in Figure 32.



**Figure 30. Startup Waveforms of Circuit Shown in the Application Diagram. Load = 400 mA.**

The CS517x can be activated by either connecting the V<sub>CC</sub> pin to a voltage source or by enabling the SS pin. Startup waveforms shown in Figure 30 are measured in the boost converter demonstrated in the Application Diagram on the page 2 of this document. Recorded after the input voltage is turned on, this waveform shows the various phases during the power up transition.

When the V<sub>CC</sub> voltage is below the minimum supply voltage, the V<sub>SW</sub> pin is in high impedance. Therefore, current conducts directly from the input power source to the output through the inductor and diode. Once V<sub>CC</sub> reaches



**Figure 31. A Typical Compensation Network**

The high DC gain in Figure 32 is desirable for achieving DC accuracy over line and load variations. The DC gain of a transconductance error amplifier can be calculated as follows:

$$\text{Gain}_{DC} = G_M \times R_O$$

where:

- G<sub>M</sub> = error amplifier transconductance;
- R<sub>O</sub> = error amplifier output resistance ≈ 1 MΩ.

The low frequency pole, f<sub>P1</sub>, is determined by the error amplifier output resistance and C1 as:

$$f_{P1} = \frac{1}{2\pi C1 R_O}$$

The first zero generated by C1 and R1 is:

$$f_{Z1} = \frac{1}{2\pi C1R1}$$

The phase lead provided by this zero ensures that the loop has at least a 45° phase margin at the crossover frequency. Therefore, this zero should be placed close to the pole generated in the power stage which can be identified at frequency:

$$f_P = \frac{1}{2\pi C_{O}R_{LOAD}}$$

where:

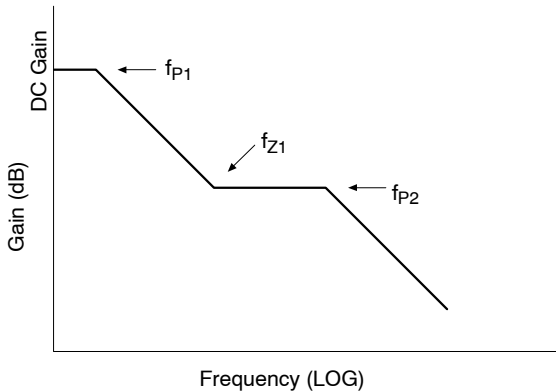
$C_O$  = output capacitor of the boost regulator.

$R_{LOAD}$  = load resistance.

The high frequency pole,  $f_{P2}$ , can be placed at the output filter's ESR zero or at half the switching frequency. Placing the pole at this frequency will cut down on switching noise. The frequency of this pole is determined by the value of C2 and R1:

$$f_{P2} = \frac{1}{2\pi C2R1}$$

One simple method to ensure adequate phase margin is to design the frequency response with a -20 dB per decade slope, until unity-gain crossover. The crossover frequency should be selected at the midpoint between  $f_{Z1}$  and  $f_{P2}$  where the phase margin is maximized.

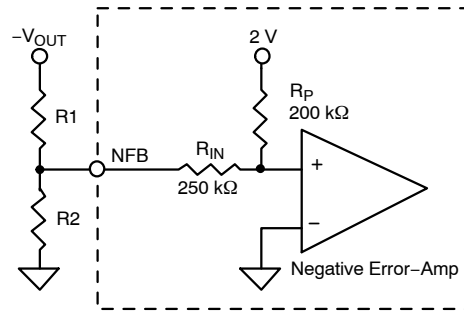


**Figure 32. Bode Plot of the Compensation Network Shown in Figure 31**

**Negative Voltage Feedback**

Since the negative error amplifier has finite input impedance as shown in Figure 33, its induced error has to be considered. If a voltage divider is used to scale down the negative output voltage for the NFB pin, the equation for calculating output voltage is:

$$-V_{OUT} = \left( \frac{-2.5 (R1 + R2)}{R2} \right) - 10 \mu A \times R1$$



**Figure 33. Negative Error Amplifier and NFB Pin**

It is shown that if R1 is less than 10 k, the deviation from the design target will be less than 0.1 V. If the tolerances of the negative voltage reference and NFB pin input current are considered, the possible offset of the output  $V_{OFFSET}$  varies in the range of:

$$\left( \frac{-0.05 (R1 + R2)}{R2} \right) - (15 \mu A \times R1) \leq V_{OFFSET} \leq \left( \frac{0.05 (R1 + R2)}{R2} \right) - (5 \mu A \times R1)$$

**V<sub>SW</sub> Voltage Limit**

In the boost topology,  $V_{SW}$  pin maximum voltage is set by the maximum output voltage plus the output diode forward voltage. The diode forward voltage is typically 0.5 V for Schottky diodes and 0.8 V for ultrafast recovery diodes

$$V_{SW(MAX)} = V_{OUT(MAX)} + V_F$$

where:

$V_F$  = output diode forward voltage.

In the flyback topology, peak  $V_{SW}$  voltage is governed by:

$$V_{SW(MAX)} = V_{CC(MAX)} + (V_{OUT} + V_F) \times N$$

where:

$N$  = transformer turns ratio, primary over secondary.

When the power switch turns off, there exists a voltage spike superimposed on top of the steady-state voltage. Usually this voltage spike is caused by transformer leakage inductance charging stray capacitance between the  $V_{SW}$  and PGND pins. To prevent the voltage at the  $V_{SW}$  pin from exceeding the maximum rating, a transient voltage suppressor in series with a diode is paralleled with the primary windings. Another method of clamping switch voltage is to connect a transient voltage suppressor between the  $V_{SW}$  pin and ground.

**Magnetic Component Selection**

When choosing a magnetic component, one must consider factors such as peak current, core and ferrite material, output voltage ripple, EMI, temperature range, physical size and cost. In boost circuits, the average inductor current is the product of output current and voltage gain ( $V_{OUT}/V_{CC}$ ), assuming 100% energy transfer efficiency. In continuous conduction mode, inductor ripple current is

$$I_{RIPPLE} = \frac{V_{CC}(V_{OUT} - V_{CC})}{(f)(L)(V_{OUT})}$$

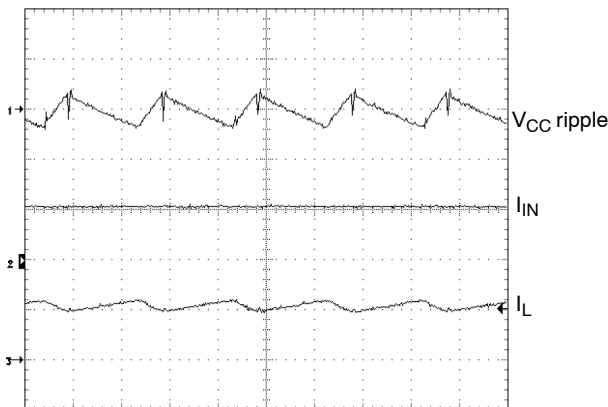
where:

$$f = 280 \text{ kHz for CS5171/2 and } 560 \text{ kHz for CS5173/4.}$$

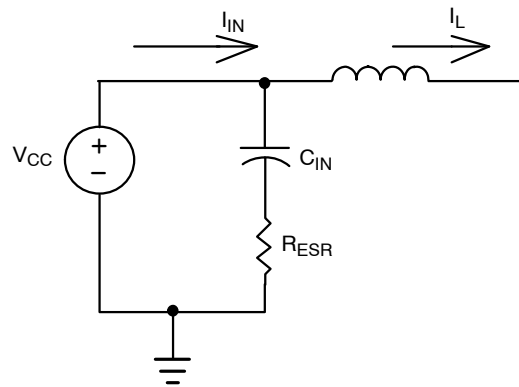
The peak inductor current is equal to average current plus half of the ripple current, which should not cause inductor saturation. The above equation can also be referenced when selecting the value of the inductor based on the tolerance of the ripple current in the circuits. Small ripple current provides the benefits of small input capacitors and greater output current capability. A core geometry like a rod or barrel is prone to generating high magnetic field radiation, but is relatively cheap and small. Other core geometries, such as toroids, provide a closed magnetic loop to prevent EMI.

**Input Capacitor Selection**

In boost circuits, the inductor becomes part of the input filter, as shown in Figure 35. In continuous mode, the input current waveform is triangular and does not contain a large pulsed current, as shown in Figure 34. This reduces the requirements imposed on the input capacitor selection. During continuous conduction mode, the peak to peak inductor ripple current is given in the previous section. As we can see from Figure 34, the product of the inductor current ripple and the input capacitor's effective series resistance (ESR) determine the  $V_{CC}$  ripple. In most applications, input capacitors in the range of 10  $\mu\text{F}$  to 100  $\mu\text{F}$  with an ESR less than 0.3  $\Omega$  work well up to a full 1.5 A switch current.



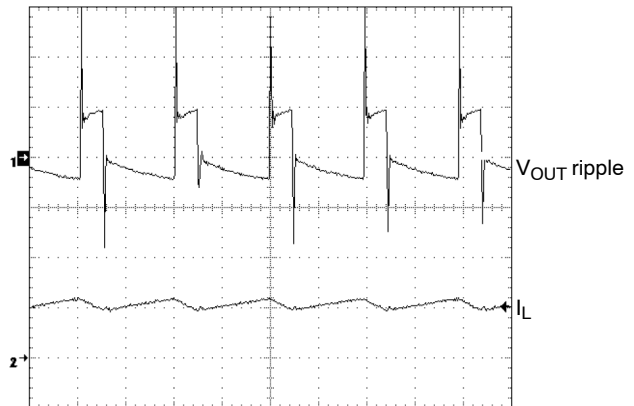
**Figure 34. Boost Input Voltage and Current Ripple Waveforms**



**Figure 35. Boost Circuit Effective Input Filter**

The situation is different in a flyback circuit. The input current is discontinuous and a significant pulsed current is seen by the input capacitors. Therefore, there are two requirements for capacitors in a flyback regulator: energy storage and filtering. To maintain a stable voltage supply to the chip, a storage capacitor larger than 20  $\mu\text{F}$  with low ESR is required. To reduce the noise generated by the inductor, insert a 1.0  $\mu\text{F}$  ceramic capacitor between  $V_{CC}$  and ground as close as possible to the chip.

**Output Capacitor Selection**



**Figure 36. Typical Output Voltage Ripple**

By examining the waveforms shown in Figure 36, we can see that the output voltage ripple comes from two major sources, namely capacitor ESR and the charging/discharging of the output capacitor. In boost circuits, when the power switch turns off,  $I_L$  flows into the output capacitor causing an instant  $\Delta V = I_L \times \text{ESR}$ . At the same time, current  $I_L - I_{OUT}$  charges the capacitor and increases the output voltage gradually. When the power output switch is turned on,  $I_L$  is shunted to ground and  $I_{OUT}$  discharges the output capacitor. When the  $I_L$  ripple is small enough,  $I_L$  can be treated as a constant and is equal to input current  $I_{IN}$ .

Summing up, the output voltage peak–peak ripple can be calculated by:

$$V_{OUT(RIPPLE)} = \frac{(I_{IN} - I_{OUT})(1 - D)}{(C_{OUT})(f)} + \frac{I_{OUT}D}{(C_{OUT})(f)} + I_{IN} \times ESR$$

The equation can be expressed more conveniently in terms of  $V_{CC}$ ,  $V_{OUT}$  and  $I_{OUT}$  for design purposes as follows:

$$V_{OUT(RIPPLE)} = \frac{I_{OUT}(V_{OUT} - V_{CC})}{(C_{OUT})(f)} \times \frac{1}{(C_{OUT})(f)} + \frac{(I_{OUT})(V_{OUT})(ESR)}{V_{CC}}$$

The capacitor RMS ripple current is:

$$I_{RIPPLE} = \sqrt{(I_{IN} - I_{OUT})^2(1 - D) + (I_{OUT})^2(D)}$$

$$= I_{OUT} \sqrt{\frac{V_{OUT} - V_{CC}}{V_{CC}}}$$

Although the above equations apply only for boost circuits, similar equations can be derived for flyback circuits.

**Reducing the Current Limit**

In some applications, the designer may prefer a lower limit on the switch current than 1.5 A. An external shunt can be connected between the  $V_C$  pin and ground to reduce its clamp voltage. Consequently, the current limit of the internal power transistor current is reduced from its nominal value.

The voltage on the  $V_C$  pin can be evaluated with the equation

$$V_C = I_{SW}R_{EA}V$$

where:

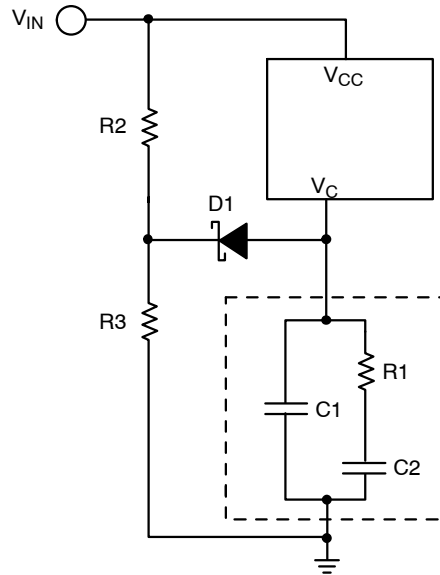
$R_E = .063\Omega$ , the value of the internal emitter resistor;

$A_V = 5 \text{ V/V}$ , the gain of the current sense amplifier.

Since  $R_E$  and  $A_V$  cannot be changed by the end user, the only available method for limiting switch current below 1.5 A is to clamp the  $V_C$  pin at a lower voltage. If the maximum switch or inductor current is substituted into the equation above, the desired clamp voltage will result.

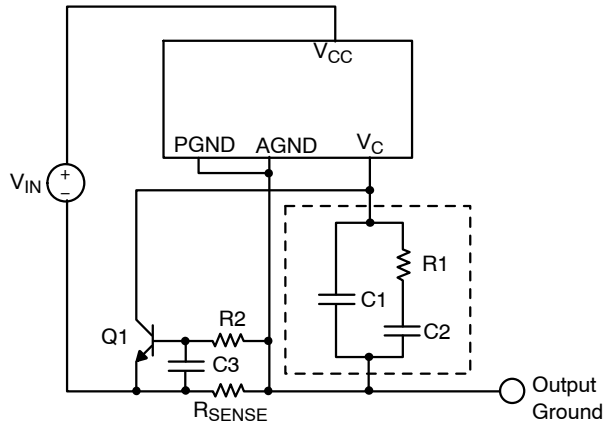
A simple diode clamp, as shown in Figure 37, clamps the  $V_C$  voltage to a diode drop above the voltage on resistor R3.

Unfortunately, such a simple circuit is not generally acceptable if  $V_{IN}$  is loosely regulated.



**Figure 37. Current Limiting using a Diode Clamp**

Another solution to the current limiting problem is to externally measure the current through the switch using a sense resistor. Such a circuit is illustrated in Figure 38.



**Figure 38. Current Limiting using a Current Sense Resistor**

The switch current is limited to

$$I_{SWITCH(PEAK)} = \frac{V_{BE}(Q1)}{R_{SENSE}}$$

where:

$V_{BE}(Q1)$  = the base–emitter voltage drop of Q1, typically 0.65 V.



The improved circuit does not require a regulated voltage to operate properly. Unfortunately, a price must be paid for this convenience in the overall efficiency of the circuit. The designer should note that the input and output grounds are no longer common. Also, the addition of the current sense resistor,  $R_{SENSE}$ , results in a considerable power loss which increases with the duty cycle. Resistor R2 and capacitor C3 form a low-pass filter to remove noise.

**Subharmonic Oscillation**

Subharmonic oscillation (SHM) is a problem found in current-mode control systems, where instability results when duty cycle exceeds 50%. SHM only occurs in switching regulators with a continuous inductor current. This instability is not harmful to the converter and usually does not affect the output voltage regulation. SHM will increase the radiated EM noise from the converter and can cause, under certain circumstances, the inductor to emit high-frequency audible noise.

SHM is an easily remedied problem. The rising slope of the inductor current is supplemented with internal “slope compensation” to prevent any duty cycle instability from carrying through to the next switching cycle. In the CS517x family, slope compensation is added during the entire switch on-time, typically in the amount of 180 mA/μs.

In some cases, SHM can rear its ugly head despite the presence of the onboard slope compensation. The simple cure to this problem is more slope compensation to avoid the unwanted oscillation. In that case, an external circuit, shown in Figure 39, can be added to increase the amount of slope compensation used. This circuit requires only a few components and is “tacked on” to the compensation network.

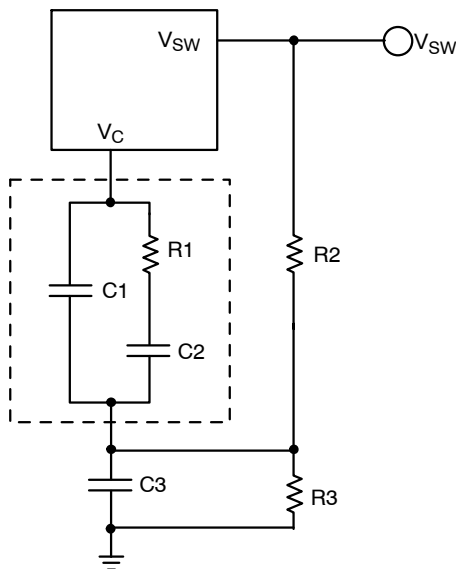


Figure 39. Technique for Increasing Slope Compensation

The dashed box contains the normal compensation circuitry to limit the bandwidth of the error amplifier. Resistors R2 and R3 form a voltage divider off of the  $V_{SW}$  pin. In normal operation,  $V_{SW}$  looks similar to a square wave, and is dependent on the converter topology. Formulas for calculating  $V_{SW}$  in the boost and flyback topologies are given in the section “ $V_{SW}$  Voltage Limit.” The voltage on  $V_{SW}$  charges capacitor C3 when the switch is off, causing the voltage at the  $V_C$  pin to shift upwards. When the switch turns on, C3 discharges through R3, producing a negative slope at the  $V_C$  pin. This negative slope provides the slope compensation.

The amount of slope compensation added by this circuit is

$$\frac{\Delta I}{\Delta T} = V_{SW} \left( \frac{R_3}{R_2 + R_3} \right) \left( 1 - e^{-\frac{(1-D)}{R_3 C_3 f_{SW}}} \right) \left( \frac{f_{SW}}{(1-D)R_E A_V} \right)$$

where:

- $\Delta I/\Delta T$  = the amount of slope compensation added (A/s);
- $V_{SW}$  = the voltage at the switch node when the transistor is turned off (V);
- $f_{SW}$  = the switching frequency, typically 280 kHz (CS5171/3) or 560 kHz (CS5172/4) (Hz);
- D = the duty cycle;
- $R_E = 0.063 \Omega$ , the value of the internal emitter resistor;
- $A_V = 5 \text{ V/V}$ , the gain of the current sense amplifier.

In selecting appropriate values for the slope compensation network, the designer is advised to choose a convenient capacitor, then select values for R2 and R3 such that the amount of slope compensation added is 100 mA/μs. Then R2 may be increased or decreased as necessary. Of course, the series combination of R2 and R3 should be large enough to avoid drawing excessive current from  $V_{SW}$ . Additionally, to ensure that the control loop stability is improved, the time constant formed by the additional components should be chosen such that

$$R_3 C_3 < \frac{1-D}{f_{SW}}$$

Finally, it is worth mentioning that the added slope compensation is a tradeoff between duty cycle stability and transient response. The more slope compensation a designer adds, the slower the transient response will be, due to the external circuitry interfering with the proper operation of the error amplifier.

**Soft-Start**

Through the addition of an external circuit, a Soft-Start function can be added to the CS5171/2/3/4 family of components. Soft-Start circuitry prevents the  $V_C$  pin from slamming high during startup, thereby inhibiting the inductor current from rising at a high slope.

This circuit, shown in Figure 40, requires a minimum number of components and allows the Soft-Start circuitry to activate any time the SS pin is used to restart the converter.

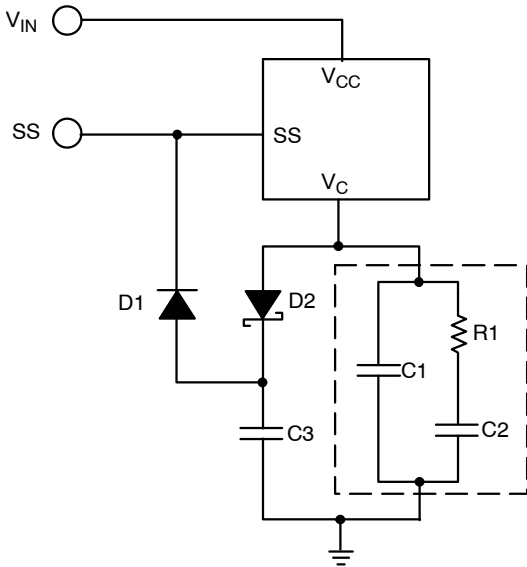


Figure 40. Soft Start

Resistor R1 and capacitors C1 and C2 form the compensation network. At turn on, the voltage at the V<sub>C</sub> pin starts to come up, charging capacitor C3 through Schottky diode D2, clamping the voltage at the V<sub>C</sub> pin such that switching begins when V<sub>C</sub> reaches the V<sub>C</sub> threshold, typically 1.05 V (refer to graphs for detail over temperature).  
 $V_C = V_F(D2) + V_{C3}$

Therefore, C3 slows the startup of the circuit by limiting the voltage on the V<sub>C</sub> pin. The Soft-Start time increases with the size of C3.

Diode D1 discharges C3 when SS is low. If the shutdown function is not used with this part, the cathode of D1 should be connected to V<sub>IN</sub>.

**Calculating Junction Temperature**

To ensure safe operation of the CS5171/2/3/4, the designer must calculate the on-chip power dissipation and determine its expected junction temperature. Internal thermal protection circuitry will turn the part off once the junction temperature exceeds 180°C ± 30°. However, repeated operation at such high temperatures will ensure a reduced operating life.

Calculation of the junction temperature is an imprecise but simple task. First, the power losses must be quantified. There are three major sources of power loss on the CS517x:

- biasing of internal control circuitry, P<sub>BIAS</sub>
- switch driver, P<sub>DRIVER</sub>
- switch saturation, P<sub>SAT</sub>

The internal control circuitry, including the oscillator and linear regulator, requires a small amount of power even

when the switch is turned off. The specifications section of this datasheet reveals that the typical operating current, I<sub>O</sub>, due to this circuitry is 5.5 mA. Additional guidance can be found in the graph of operating current vs. temperature. This graph shows that I<sub>O</sub> is strongly dependent on input voltage, V<sub>IN</sub>, and temperature. Then

$$P_{BIAS} = V_{IN}I_O$$

Since the onboard switch is an NPN transistor, the base drive current must be factored in as well. This current is drawn from the V<sub>IN</sub> pin, in addition to the control circuitry current. The base drive current is listed in the specifications as ΔI<sub>CC</sub>/ΔI<sub>SW</sub>, or switch transconductance. As before, the designer will find additional guidance in the graphs. With that information, the designer can calculate

$$P_{DRIVER} = V_{IN}I_{SW} \times \frac{I_{CC}}{\Delta I_{SW}} \times D$$

where:

I<sub>SW</sub> = the current through the switch;

D = the duty cycle or percentage of switch on-time.

I<sub>SW</sub> and D are dependent on the type of converter. In a boost converter,

$$I_{SW(AVG)} \approx I_L(AVG) \times D \times \frac{1}{\text{Efficiency}}$$

$$D \approx \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

In a flyback converter,

$$I_{SW(AVG)} \approx \frac{V_{OUT}I_{LOAD}}{V_{IN}} \times \frac{1}{\text{Efficiency}} \times \frac{1}{D}$$

$$D \approx \frac{V_{OUT}}{V_{OUT} + \frac{N_S}{N_P}V_{IN}}$$

The switch saturation voltage, V<sub>(CE)SAT</sub>, is the last major source of on-chip power loss. V<sub>(CE)SAT</sub> is the collector-emitter voltage of the internal NPN transistor when it is driven into saturation by its base drive current. The value for V<sub>(CE)SAT</sub> can be obtained from the specifications or from the graphs, as “Switch Saturation Voltage.” Thus,

$$P_{SAT} \approx V_{(CE)SAT}I_{SW} \times D$$

Finally, the total on-chip power losses are

$$P_D = P_{BIAS} + P_{DRIVER} + P_{SAT}$$

Power dissipation in a semiconductor device results in the generation of heat in the junctions at the surface of the chip. This heat is transferred to the surface of the IC package, but a thermal gradient exists due to the resistive properties of the package molding compound. The magnitude of the thermal gradient is expressed in manufacturers’ data sheets as θ<sub>JA</sub>, or junction-to-ambient thermal resistance. The on-chip junction temperature can be calculated if θ<sub>JA</sub>, the air temperature near the surface of the IC, and the on-chip power dissipation are known.



## CS5171, CS5172, CS5173, CS5174

$$T_J = T_A + (P_D \theta_{JA})$$

where:

$T_J$  = IC or FET junction temperature ( $^{\circ}\text{C}$ );

$T_A$  = ambient temperature ( $^{\circ}\text{C}$ );

$P_D$  = power dissipated by part in question (W);

$\theta_{JA}$  = junction-to-ambient thermal resistance ( $^{\circ}\text{C}/\text{W}$ ).

For the CS517x,  $\theta_{JA}=165^{\circ}\text{C}/\text{W}$ .

Once the designer has calculated  $T_J$ , the question of whether the CS517x can be used in an application is settled. If  $T_J$  exceeds  $150^{\circ}\text{C}$ , the absolute maximum allowable junction temperature, the CS517x is not suitable for that application.

If  $T_J$  approaches  $150^{\circ}\text{C}$ , the designer should consider possible means of reducing the junction temperature. Perhaps another converter topology could be selected to reduce the switch current. Increasing the airflow across the surface of the chip might be considered to reduce  $T_A$ .

### Circuit Layout Guidelines

In any switching power supply, circuit layout is very important for proper operation. Rapidly switching currents combined with trace inductance generates voltage

transitions that can cause problems. Therefore the following guidelines should be followed in the layout.

1. In boost circuits, high AC current circulates within the loop composed of the diode, output capacitor, and on-chip power transistor. The length of associated traces and leads should be kept as short as possible. In the flyback circuit, high AC current loops exist on both sides of the transformer. On the primary side, the loop consists of the input capacitor, transformer, and on-chip power transistor, while the transformer, rectifier diodes, and output capacitors form another loop on the secondary side. Just as in the boost circuit, all traces and leads containing large AC currents should be kept short.
2. Separate the low current signal grounds from the power grounds. Use single point grounding or ground plane construction for the best results.
3. Locate the voltage feedback resistors as near the IC as possible to keep the sensitive feedback wiring short. Connect feedback resistors to the low current analog ground.

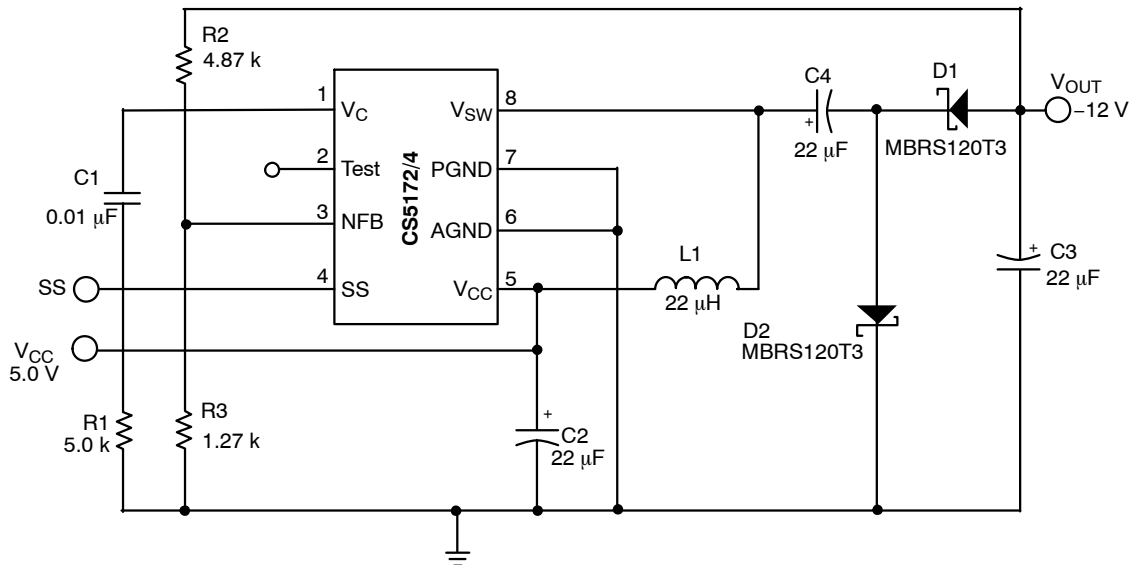
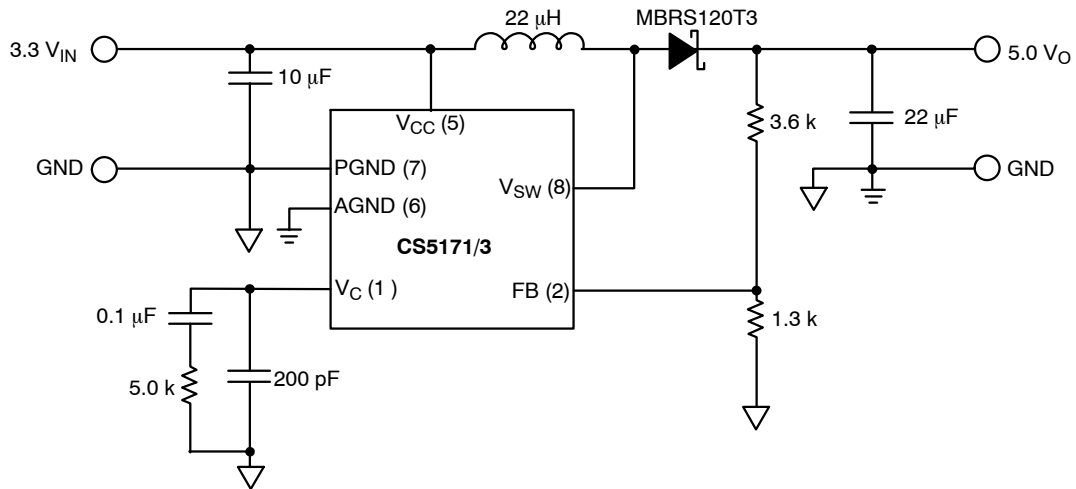
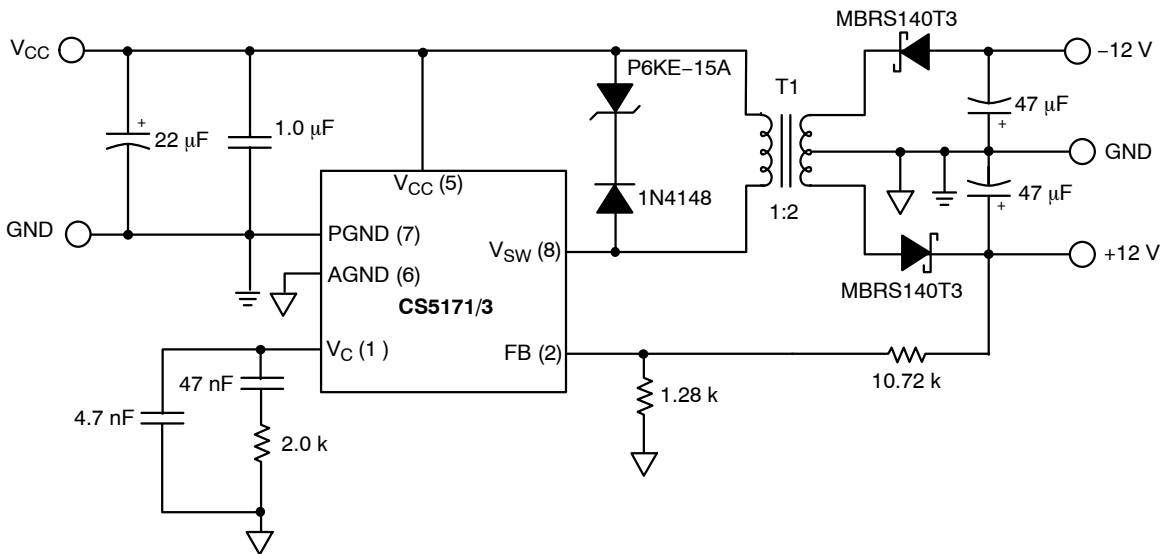


Figure 41. Additional Application Diagram, 5.0 V to -12 V/ 75 mA Inverting Converter

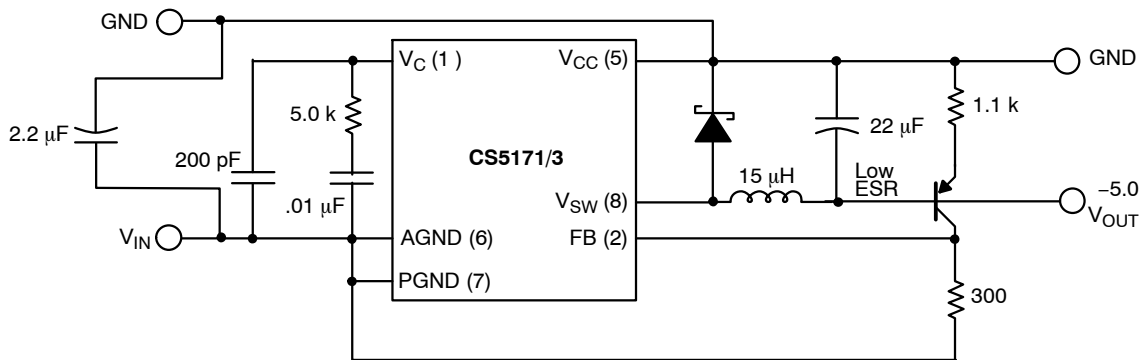
## CS5171, CS5172, CS5173, CS5174



**Figure 42. Additional Application Diagram, 3.3 V Input, 5.0 V/ 400 mA Output Boost Converter**

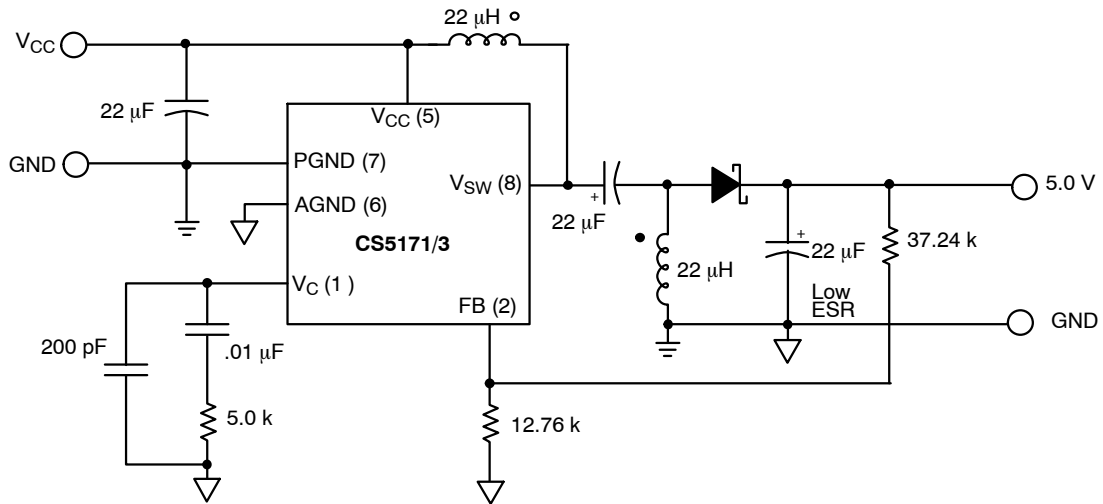


**Figure 43. Additional Application Diagram, 2.7 to 13 V Input, ±12 V/ 200 mA Output Flyback Converter**

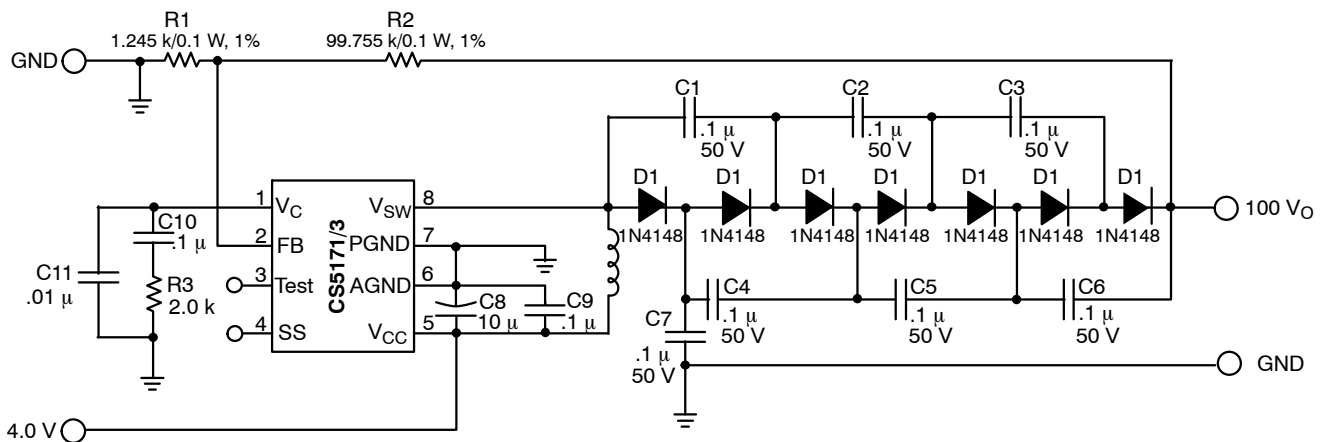


**Figure 44. Additional Application Diagram, -9.0 V to -28 V Input, -5.0 V/700 mA Output Inverted Buck Converter**

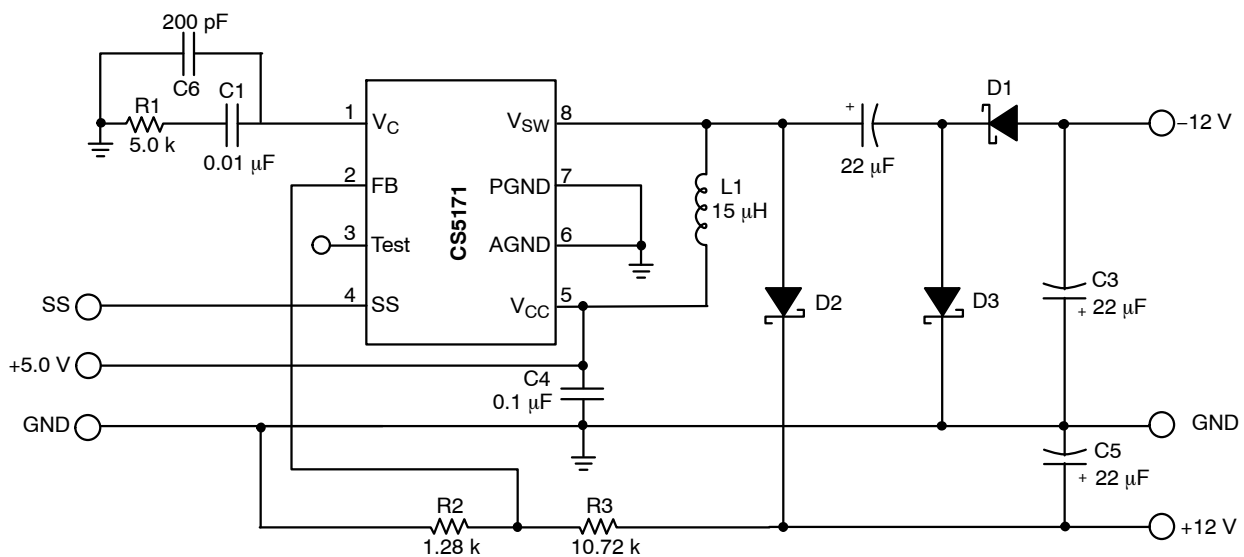
## CS5171, CS5172, CS5173, CS5174



**Figure 45. Additional Application Diagram, 2.7 V to 28 V Input, 5.0 V Output SEPIC Converter**



**Figure 46. Additional Application Diagram, 4.0 V Input, 100 V/ 10 mA Output Boost Converter with Output Voltage Multiplier**



**Figure 47. Additional Application Diagram, 5.0 V Input, ± 12 V Output Dual Boost Converter**

## CS5171, CS5172, CS5173, CS5174

### ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping <sup>†</sup>
CS5171ED8G	-40°C < T <sub>J</sub> < 125°C	SOIC-8 (Pb-Free)	98 Units/Rail
CS5171EDR8G		SOIC-8 (Pb-Free)	2500 Tape & Reel
CS5172ED8G		SOIC-8 (Pb-Free)	98 Units/Rail
CS5172EDR8G		SOIC-8 (Pb-Free)	2500 Tape & Reel
CS5173ED8G		SOIC-8 (Pb-Free)	98 Units/Rail
CS5173EDR8G		SOIC-8 (Pb-Free)	2500 Tape & Reel
CS5174ED8G		SOIC-8 (Pb-Free)	98 Units/Rail
CS5174EDR8G		SOIC-8 (Pb-Free)	2500 Tape & Reel
CS5171GD8G	0°C < T <sub>J</sub> < 125°C	SOIC-8 (Pb-Free)	98 Units/Rail
CS5171GDR8G		SOIC-8 (Pb-Free)	2500 Tape & Reel
CS5172GD8G		SOIC-8 (Pb-Free)	98 Units/Rail
CS5172GDR8G		SOIC-8 (Pb-Free)	2500 Tape & Reel
CS5173GD8G		SOIC-8 (Pb-Free)	98 Units/Rail
CS5173GDR8G		SOIC-8 (Pb-Free)	2500 Tape & Reel
CS5174GD8G		SOIC-8 (Pb-Free)	98 Units/Rail
CS5174GDR8G		SOIC-8 (Pb-Free)	2500 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |   |  |  |  |
|---|--|--|--|
| <p>STYLE 1:<br/>         PIN 1. EMITTER<br/>         2. COLLECTOR<br/>         3. COLLECTOR<br/>         4. EMITTER<br/>         5. EMITTER<br/>         6. BASE<br/>         7. BASE<br/>         8. EMITTER</p>   | <p>STYLE 2:<br/>         PIN 1. COLLECTOR, DIE, #1<br/>         2. COLLECTOR, #1<br/>         3. COLLECTOR, #2<br/>         4. COLLECTOR, #2<br/>         5. BASE, #2<br/>         6. EMITTER, #2<br/>         7. BASE, #1<br/>         8. EMITTER, #1</p>               | <p>STYLE 3:<br/>         PIN 1. DRAIN, DIE #1<br/>         2. DRAIN, #1<br/>         3. DRAIN, #2<br/>         4. DRAIN, #2<br/>         5. GATE, #2<br/>         6. SOURCE, #2<br/>         7. GATE, #1<br/>         8. SOURCE, #1</p>                            | <p>STYLE 4:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. ANODE<br/>         4. ANODE<br/>         5. ANODE<br/>         6. ANODE<br/>         7. ANODE<br/>         8. COMMON CATHODE</p>   |
| <p>STYLE 5:<br/>         PIN 1. DRAIN<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. DRAIN<br/>         5. GATE<br/>         6. GATE<br/>         7. SOURCE<br/>         8. SOURCE</p>   | <p>STYLE 6:<br/>         PIN 1. SOURCE<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. SOURCE<br/>         5. SOURCE<br/>         6. GATE<br/>         7. GATE<br/>         8. SOURCE</p>  | <p>STYLE 7:<br/>         PIN 1. INPUT<br/>         2. EXTERNAL BYPASS<br/>         3. THIRD STAGE SOURCE<br/>         4. GROUND<br/>         5. DRAIN<br/>         6. GATE 3<br/>         7. SECOND STAGE Vd<br/>         8. FIRST STAGE Vd</p>                    | <p>STYLE 8:<br/>         PIN 1. COLLECTOR, DIE #1<br/>         2. BASE, #1<br/>         3. BASE, #2<br/>         4. COLLECTOR, #2<br/>         5. COLLECTOR, #2<br/>         6. EMITTER, #2<br/>         7. EMITTER, #1<br/>         8. COLLECTOR, #1</p>                              |
| <p>STYLE 9:<br/>         PIN 1. EMITTER, COMMON<br/>         2. COLLECTOR, DIE #1<br/>         3. COLLECTOR, DIE #2<br/>         4. EMITTER, COMMON<br/>         5. EMITTER, COMMON<br/>         6. BASE, DIE #2<br/>         7. BASE, DIE #1<br/>         8. EMITTER, COMMON</p> | <p>STYLE 10:<br/>         PIN 1. GROUND<br/>         2. BIAS 1<br/>         3. OUTPUT<br/>         4. GROUND<br/>         5. GROUND<br/>         6. BIAS 2<br/>         7. INPUT<br/>         8. GROUND</p>  | <p>STYLE 11:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. DRAIN 2<br/>         7. DRAIN 1<br/>         8. DRAIN 1</p>   | <p>STYLE 12:<br/>         PIN 1. SOURCE<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 13:<br/>         PIN 1. N.C.<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>  | <p>STYLE 14:<br/>         PIN 1. N-SOURCE<br/>         2. N-GATE<br/>         3. P-SOURCE<br/>         4. P-GATE<br/>         5. P-DRAIN<br/>         6. P-DRAIN<br/>         7. N-DRAIN<br/>         8. N-DRAIN</p>   | <p>STYLE 15:<br/>         PIN 1. ANODE 1<br/>         2. ANODE 1<br/>         3. ANODE 1<br/>         4. ANODE 1<br/>         5. CATHODE, COMMON<br/>         6. CATHODE, COMMON<br/>         7. CATHODE, COMMON<br/>         8. CATHODE, COMMON</p>               | <p>STYLE 16:<br/>         PIN 1. EMITTER, DIE #1<br/>         2. BASE, DIE #1<br/>         3. EMITTER, DIE #2<br/>         4. BASE, DIE #2<br/>         5. COLLECTOR, DIE #2<br/>         6. COLLECTOR, DIE #2<br/>         7. COLLECTOR, DIE #1<br/>         8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:<br/>         PIN 1. VCC<br/>         2. V2OUT<br/>         3. V1OUT<br/>         4. TXE<br/>         5. RXE<br/>         6. VEE<br/>         7. GND<br/>         8. ACC</p>  | <p>STYLE 18:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. CATHODE<br/>         8. CATHODE</p>   | <p>STYLE 19:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. MIRROR 2<br/>         7. DRAIN 1<br/>         8. MIRROR 1</p>   | <p>STYLE 20:<br/>         PIN 1. SOURCE (N)<br/>         2. GATE (N)<br/>         3. SOURCE (P)<br/>         4. GATE (P)<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 21:<br/>         PIN 1. CATHODE 1<br/>         2. CATHODE 2<br/>         3. CATHODE 3<br/>         4. CATHODE 4<br/>         5. CATHODE 5<br/>         6. COMMON ANODE<br/>         7. COMMON ANODE<br/>         8. CATHODE 6</p>  | <p>STYLE 22:<br/>         PIN 1. I/O LINE 1<br/>         2. COMMON CATHODE/VCC<br/>         3. COMMON CATHODE/VCC<br/>         4. I/O LINE 3<br/>         5. COMMON ANODE/GND<br/>         6. I/O LINE 4<br/>         7. I/O LINE 5<br/>         8. COMMON ANODE/GND</p> | <p>STYLE 23:<br/>         PIN 1. LINE 1 IN<br/>         2. COMMON ANODE/GND<br/>         3. COMMON ANODE/GND<br/>         4. LINE 2 IN<br/>         5. LINE 2 OUT<br/>         6. COMMON ANODE/GND<br/>         7. COMMON ANODE/GND<br/>         8. LINE 1 OUT</p> | <p>STYLE 24:<br/>         PIN 1. BASE<br/>         2. EMITTER<br/>         3. COLLECTOR/ANODE<br/>         4. COLLECTOR/ANODE<br/>         5. CATHODE<br/>         6. CATHODE<br/>         7. COLLECTOR/ANODE<br/>         8. COLLECTOR/ANODE</p>                                      |
| <p>STYLE 25:<br/>         PIN 1. VIN<br/>         2. N/C<br/>         3. REXT<br/>         4. GND<br/>         5. IOUT<br/>         6. IOUT<br/>         7. IOUT<br/>         8. IOUT</p>   | <p>STYLE 26:<br/>         PIN 1. GND<br/>         2. dv/dt<br/>         3. ENABLE<br/>         4. ILIMIT<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. VCC</p>  | <p>STYLE 27:<br/>         PIN 1. ILIMIT<br/>         2. OVLO<br/>         3. UVLO<br/>         4. INPUT+<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. DRAIN</p>  | <p>STYLE 28:<br/>         PIN 1. SW_TO_GND<br/>         2. DASIC_OFF<br/>         3. DASIC_SW_DET<br/>         4. GND<br/>         5. V_MON<br/>         6. VBULK<br/>         7. VBULK<br/>         8. VIN</p>  |
| <p>STYLE 29:<br/>         PIN 1. BASE, DIE #1<br/>         2. EMITTER, #1<br/>         3. BASE, #2<br/>         4. EMITTER, #2<br/>         5. COLLECTOR, #2<br/>         6. COLLECTOR, #2<br/>         7. COLLECTOR, #1<br/>         8. COLLECTOR, #1</p>                        | <p>STYLE 30:<br/>         PIN 1. DRAIN 1<br/>         2. DRAIN 1<br/>         3. GATE 2<br/>         4. SOURCE 2<br/>         5. SOURCE 1/DRAIN 2<br/>         6. SOURCE 1/DRAIN 2<br/>         7. SOURCE 1/DRAIN 2<br/>         8. GATE 1</p>                           |  |  |

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