

# SCR

2N5204-07

**SOLID STATE INC.**  
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The 2N5204-07 series of silicon controlled rectifiers are reverse blocking triode thyristor semiconductor devices for use in medium power switching and phase control applications requiring blocking voltage up to 1200 volts, and average load current (single-phase, 180° conduction angle) up to 22 amperes.



### MAXIMUM ALLOWABLE RATINGS

Type	Repetitive Peak Off-State Voltage, $V_{DRM}^{(1) (2)}$ $T_C = -40^{\circ}\text{C to } +125^{\circ}\text{C}$	Repetitive Peak Reverse Voltage $V_{RRM}^{(1) (2)}$ $T_C = -40^{\circ}\text{C to } +125^{\circ}\text{C}$	Non-repetitive Peak Reverse Voltage $V_{RSM}^{(1) (3)}$ $T_C = -40^{\circ}\text{C to } +125^{\circ}\text{C}$
2N5204	600 Volts†	600 Volts†	720 Volts†
2N5205	800 Volts†	800 Volts†	960 Volts†
2N5206	1000 Volts†	1000 Volts†	1200 Volts†
2N5207	1200 Volts†	1200 Volts†	1440 Volts†

- (1) Values apply for gate terminal open-circuited. (Negative gate bias is permissible.)
- (2) Maximum case-to-ambient thermal resistance for which maximum  $V_{DRM}$  and  $V_{RRM}$  ratings apply equals 5.0°C per watt for full sine wave or full-wave rectified sinusoidal voltage waveform. (3.0°C per watt is maximum case-to-ambient thermal resistance for pure dc voltage waveform.)
- (3) Half sine wave voltage pulse, 10 millisecond maximum duration.
- (4) di/dt rating is established in accordance with EIA Standard RS-397, Section 5.2.2.6. Off-state (blocking) voltage capability may be temporarily lost immediately after each current pulse for duration less than the period of the applied pulse repetition rate. The pulse repetition rate for this test is 400 Hz. The duration of the JEDEC di/dt test condition is 5.0 seconds (minimum).

RMS On-State Current, $I_{T(RMS)}$ .....	35 Amperes (all conduction angles)
Average On-State Current, $I_{T(AV)}$ .....	Depends on conduction angle (See Charts 3 and 5)
Critical Rate-of-Rise of On-State Current, di/dt:(4) .....	
Gate triggered operation .....	(See Chart 6)
Switching from 1200 volts .....	75 Amperes per microsecond†
1000 volts .....	80 Amperes per microsecond†
800 volts .....	90 Amperes per microsecond†
600 volts .....	100 Amperes per microsecond†
Breakover voltage triggered operation .....	10 Amperes per microsecond
Peak One Cycle Surge (non-rep) On-State Current, $I_{TSM}$ .....	300 Amperes†
$I^2t$ (for fusing), for time = 1.0 milliseconds (See Chart 9) .....	200 Ampere <sup>2</sup> seconds
for time = 8.3 milliseconds (See Chart 9) .....	375 Ampere <sup>2</sup> seconds
Peak Gate Power Dissipation, $P_{GM}$ .....	60 Watts for 500 microseconds†
Average Gate Power Dissipation, $P_{G(AV)}$ .....	10 Watts†
Peak Negative Gate Voltage, $V_{GM}$ .....	5 Volts†
Storage Temperature, $T_{STG}$ .....	-40°C to +150°C†
Operating Temperature, $T_J$ .....	-40°C to +125°C†
Maximum Stud Torque .....	30 Lb-in (35 Kg-cm)

†Indicates data included on JEDEC Type Number Registration.

CHARACTERISTICS

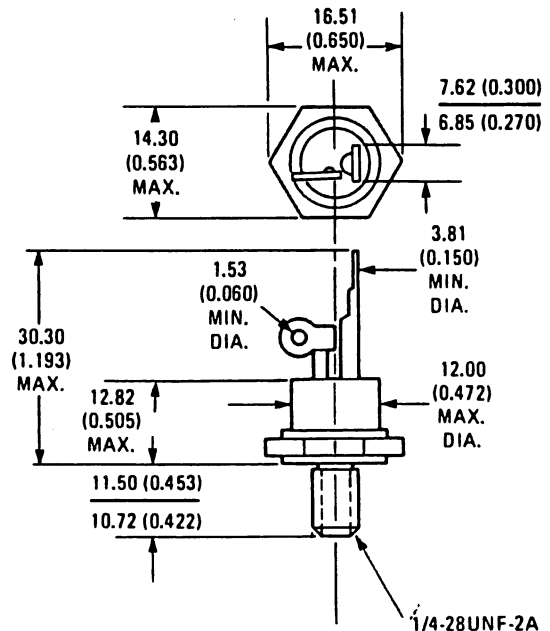
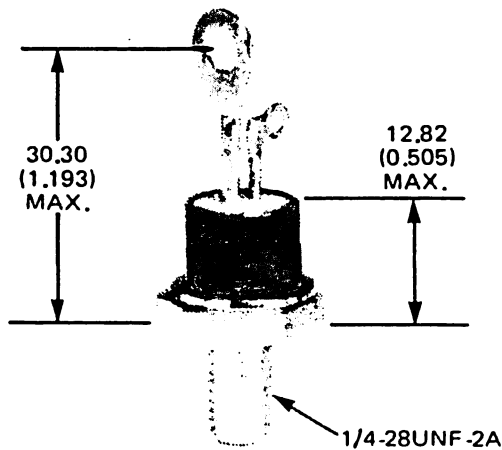
Test	Symbol	Min.	Max.	Units	Test Conditions
Peak Off-State or Reverse Current (1)(2)	$I_{DPM}$ or $I_{RPM}$			mA	$T_c = -40^\circ$ to $+125^\circ\text{C}$  $V_{DPM} = V_{RPM} = 600$ Volts Peak 800 1000 1200
D.C. Gate Trigger Current	$I_T$	—	40	mA dc	$T_c = +25^\circ\text{C}$ , $V_D = 12$ Vdc, $R_L = 12$ ohms
		—	80†		$T_c = -40^\circ\text{C}$ , $V_D = 12$ Vdc, $R_L = 12$ ohms
D.C. Gate Trigger Voltage	$V_{GT}$	—	3.0	Vdc	$T_c = +25^\circ\text{C}$ , $V_D = 12$ Vdc, $R_L = 12$ ohms
		—	3.0†		$T_c = -40^\circ\text{C}$ , $V_D = 12$ Vdc, $R_L = 12$ ohms
		0.25†	—		$T_c = +125^\circ\text{C}$ , Rated $V_{DPM}$ , $R_L = 1000$ ohms
Peak On-State Voltage	$V_{TM}$	—	2.3†	Volts	$T_c = +25^\circ\text{C}$ , $I_{TM} = 70$ A peak, 1 msec wide pulse. Duty cycle $\leq 2\%$ .
Holding Current	$I_H$	—	100	mA dc	Anode supply = 24 Vdc, Gate supply = 10 V, 20 ohms. Initial Forward Current Pulse = 0.5 A, 0.1 to 10.0 msec. wide.
		—	200†		$T_c = +25^\circ\text{C}$
		—	—		$T_c = -40^\circ\text{C}$
Critical Rate of Rise of Forward Blocking Voltage. (Higher values may cause device switching.)	dv/dt	100†	—	Volts/ $\mu\text{sec}$	$T_c = +125^\circ\text{C}$ , Rated $V_{DPM}$ , Gate open circuited.
Thermal Resistance	$\theta_{J-C}$	—	1.5†	$^\circ\text{C}/\text{watt}$	Junction-to-case, dc

(1) Values apply for gate terminal open-circuited. (Negative gate bias is permissible.)

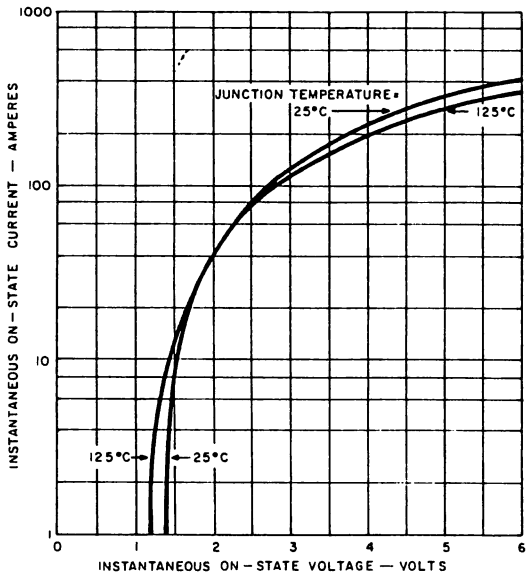
(2) Maximum case-to-ambient thermal resistance for which maximum  $V_{DPM}$  and  $V_{RPM}$  ratings apply equals  $5.0^\circ\text{C}$  per watt for full sine wave or full-wave rectified sinusoidal voltage waveform. ( $3.0^\circ\text{C}$  per watt is maximum case-to-ambient thermal resistance for pure dc voltage waveform.)

†Indicates data included on JEDEC Type Number Registration.

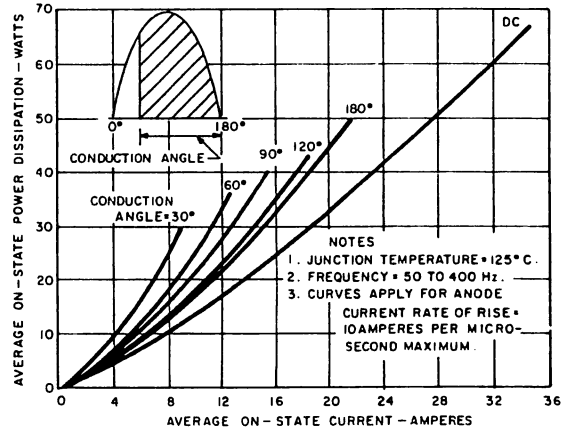
CASE STYLE AND DIMENSIONS



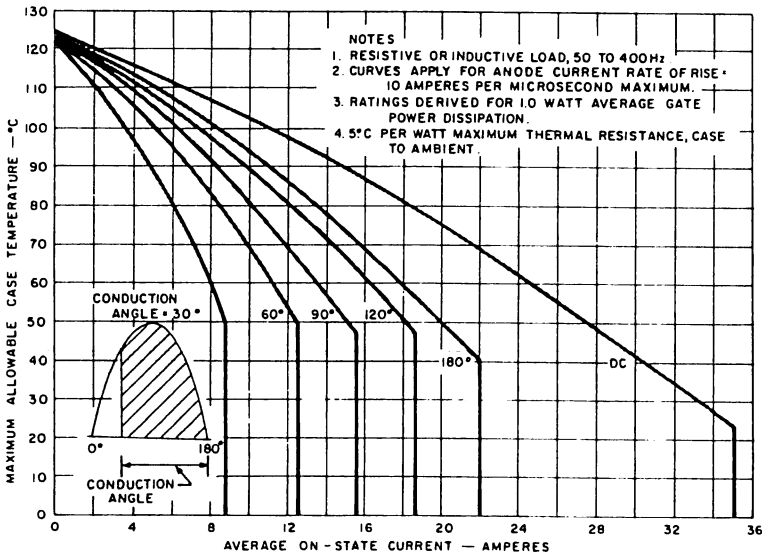
Conforms to JEDEC Outline TO-208AA (TO-48)  
Dimensions in Millimeters and (Inches)



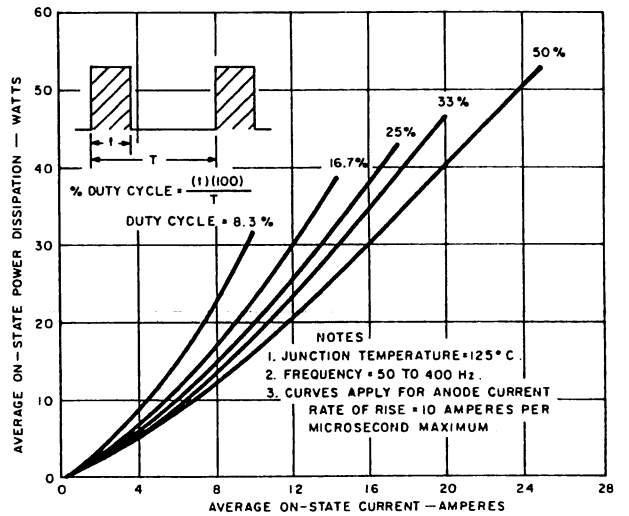
1. MAXIMUM ON-STATE CHARACTERISTICS



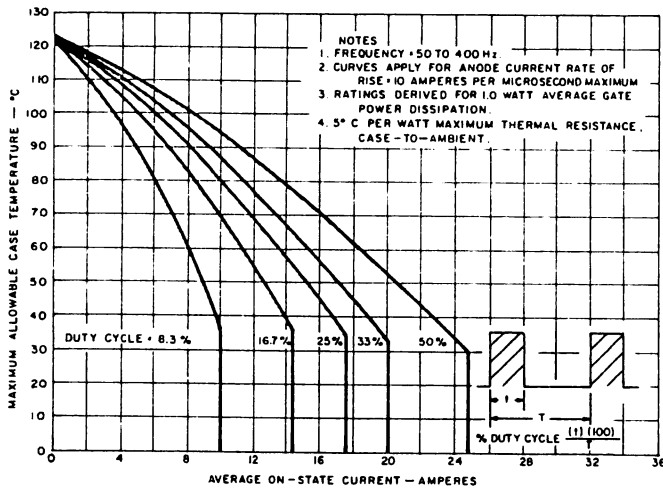
2. MAXIMUM ON-STATE POWER DISSIPATION FOR HALF-WAVE RECTIFIED SINE WAVE OF CURRENT



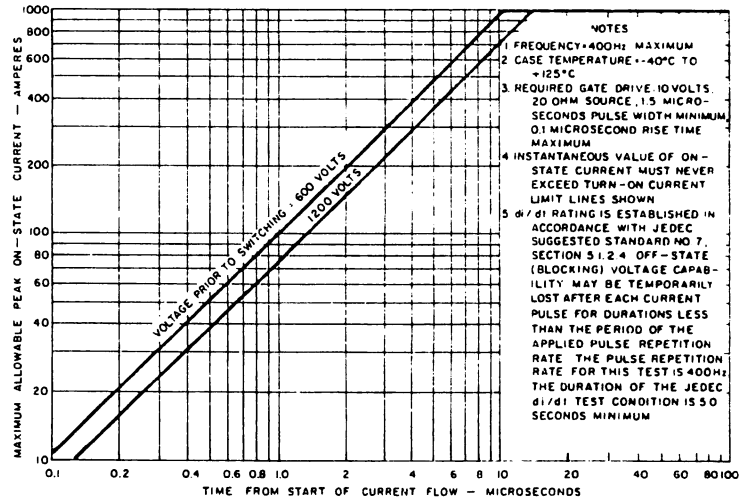
3. MAXIMUM ALLOWABLE CASE TEMPERATURE FOR HALF-WAVE RECTIFIED SINE WAVE OF CURRENT



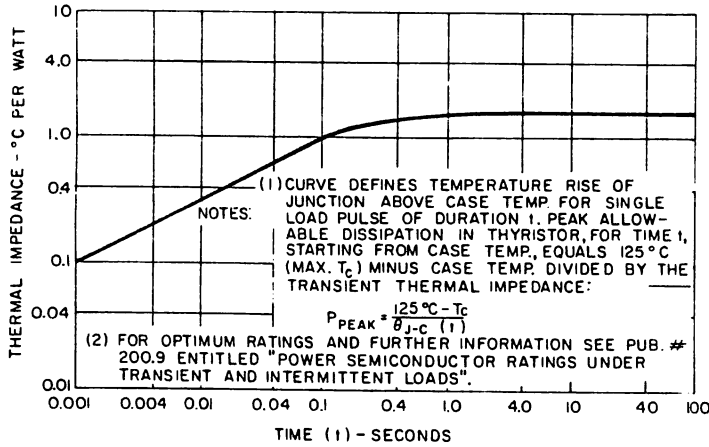
4. MAXIMUM ON-STATE POWER DISSIPATION FOR RECTANGULAR CURRENT WAVEFORM



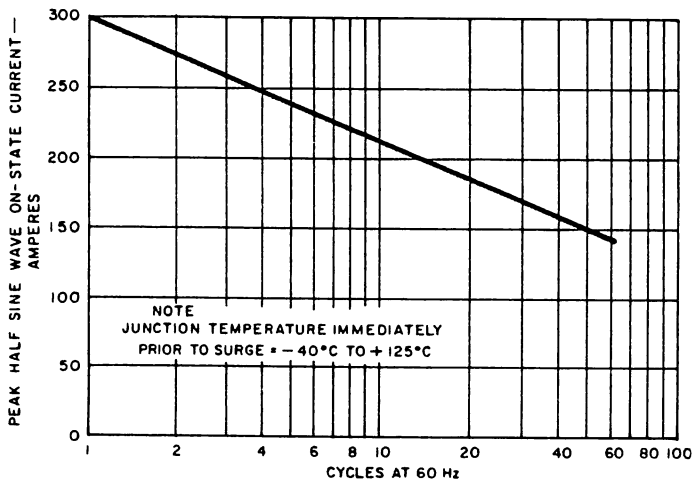
5. MAXIMUM ALLOWABLE CASE TEMPERATURE FOR RECTANGULAR CURRENT WAVEFORM



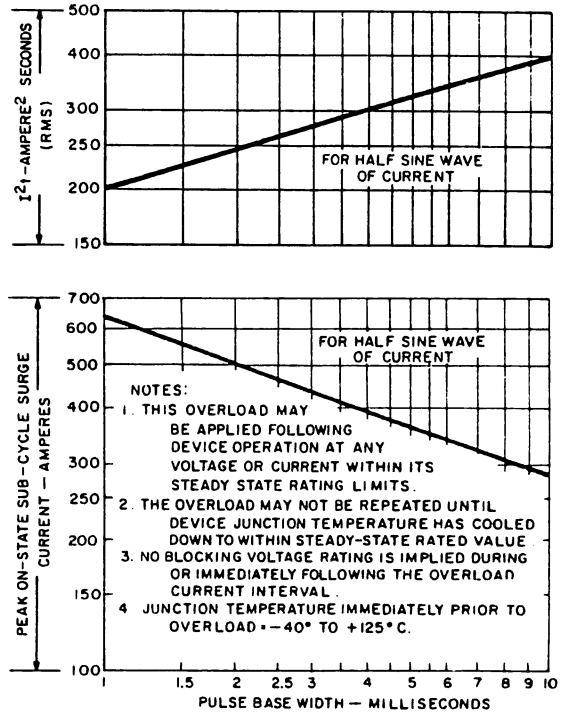
6. TURN-ON CURRENT LIMIT



7. MAXIMUM TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE



8. MAXIMUM ALLOWABLE SURGE (NON-REPETITIVE) ON-STATE CURRENT



9. MAXIMUM ALLOWABLE SUB-CYCLE SURGE (NON-REPETITIVE) ON-STATE CURRENT AND I<sup>2</sup>T RATING