

<b>V<sub>DS</sub></b>	<b>1200 V</b>
<b>I<sub>DS</sub></b>	<b>480 A</b>

# CAS480M12HM3

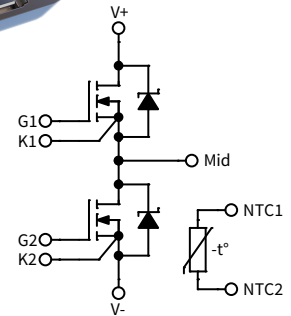
## 1200 V, 480 A, Silicon Carbide

### High-Performance, Switching Optimized, Half-Bridge Module

#### Technical Features

- Low Inductance, Low Profile 62mm Footprint
- High Junction Temperature (175 °C) Operation
- Implements Switching Optimized Third Generation SiC MOSFET Technology
- Zero Reverse Recovery from Diodes
- Light Weight AlSiC Baseplate
- High Reliability Silicon Nitride Insulator

#### Package 110mm x 65 mm x 12.2 mm



#### Applications

- Railway & Traction
- Solar
- EV Chargers
- Industrial Automation & Testing

#### System Benefits

- Lightweight, Compact Form Factor with 62mm Compatible Baseplate Enables System Retrofit
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC
- High Reliability Material Selection

#### Key Parameters (T<sub>C</sub> = 25 °C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
V <sub>DS max</sub>	Drain-Source Voltage			1200	V		Fig. 33
V <sub>GS max</sub>	Gate-Source Voltage, Maximum Value	-8		+19		Transient, <100 ns	
V <sub>GS op</sub>	Gate-Source Voltage, Recommended Op. Value	-4		+15		Static	
I <sub>DS</sub>	DC Continuous Drain Current		640		A	V <sub>GS</sub> = 15 V, T <sub>C</sub> = 25 °C, T <sub>VJ</sub> ≤ 175 °C	Fig. 20
			481			V <sub>GS</sub> = 15 V, T <sub>C</sub> = 90 °C, T <sub>VJ</sub> ≤ 175 °C	
I <sub>SD</sub>	DC Source-Drain Current		640			V <sub>GS</sub> = 15 V, T <sub>C</sub> = 25 °C, T <sub>VJ</sub> ≤ 175 °C	
I <sub>F</sub>	Schottky Diode DC Forward Current		464			V <sub>GS</sub> = -4 V, T <sub>C</sub> = 25 °C, T <sub>VJ</sub> ≤ 175 °C	
I <sub>DS (pulsed)</sub>	Maximum Pulsed Drain-Source Current			960		t <sub>Pmax</sub> limited by T <sub>VJ max</sub>	
I <sub>F (pulsed)</sub>	Maximum Pulsed Diode Current			960	V <sub>GS</sub> = 15 V, T <sub>C</sub> = 25 °C		
T <sub>VJ op</sub>	Maximum Virtual Junction Temperature under Switching Conditions	-40		175	°C		

### MOSFET Characteristics (Per Position) ( $T_{VJ} = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	$V_{GS} = 0\text{ V}, T_{VJ} = -40^\circ\text{C}$	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.5	3.6		$V_{DS} = V_{GS}, I_D = 160\text{ mA}$	
			2.0			$V_{DS} = V_{GS}, I_D = 160\text{ mA}, T_{VJ} = 175^\circ\text{C}$	
$I_{DSS}$	Zero Gate Voltage Drain Current		10	280	$\mu\text{A}$	$V_{GS} = 0\text{ V}, V_{DS} = 1200\text{ V}$	
$I_{GSS}$	Gate-Source Leakage Current		0.1	2		$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$	
$R_{DS(on)}$	Drain-Source On-State Resistance (Devices Only)		2.29	2.97	m $\Omega$	$V_{GS} = 15\text{ V}, I_D = 480\text{ A}$	Fig. 2 Fig. 3
			3.66			$V_{GS} = 15\text{ V}, I_D = 480\text{ A}, T_{VJ} = 175^\circ\text{C}$	
$g_{fs}$	Transconductance		356		S	$V_{DS} = 20\text{ V}, I_{DS} = 480\text{ A}$	Fig. 4
			345			$V_{DS} = 20\text{ V}, I_{DS} = 480\text{ A}, T_{VJ} = 175^\circ\text{C}$	
$E_{On}$	Turn-On Switching Energy, $T_{VJ} = 25^\circ\text{C}$ $T_{VJ} = 125^\circ\text{C}$ $T_{VJ} = 175^\circ\text{C}$		11.3		mJ	$V_{DS} = 600\text{ V},$ $I_D = 500\text{ A},$ $V_{GS} = -4\text{ V}/15\text{ V},$ $R_{G(ext)} = 1.0\ \Omega,$ $L = 13.7\ \mu\text{H}$	Fig. 11 Fig. 13
			9.6				
			9.9				
$E_{Off}$	Turn-Off Switching Energy, $T_{VJ} = 25^\circ\text{C}$ $T_{VJ} = 125^\circ\text{C}$ $T_{VJ} = 175^\circ\text{C}$		7.2		mJ	$V_{DS} = 600\text{ V},$ $I_D = 500\text{ A},$ $V_{GS} = -4\text{ V}/15\text{ V},$ $R_{G(ext)} = 1.0\ \Omega,$ $L = 13.7\ \mu\text{H}$	Fig. 11 Fig. 13
			7.3				
			7.4				
$R_{G(int)}$	Internal Gate Resistance		0.8		$\Omega$	$V_{AC} = 25\text{ mV}, f = 100\text{ kHz}$	
$C_{iss}$	Input Capacitance		43.1		nF	$V_{GS} = 0\text{ V}, V_{DS} = 800\text{ V},$ $V_{AC} = 25\text{ mV}, f = 100\text{ kHz}$	Fig. 9
$C_{oss}$	Output Capacitance		2.76				
$C_{rss}$	Reverse Transfer Capacitance		70.7				
$Q_{GS}$	Gate to Source Charge		448		nC	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 480\text{ A}$ Per IEC60747-8-4 pg 21	
$Q_{GD}$	Gate to Drain Charge		539				
$Q_G$	Total Gate Charge		1590				
$R_{thJC}$	FET Thermal Resistance, Junction to Case		0.1	0.115	$^\circ\text{C}/\text{W}$		Fig. 17

### Diode Characteristics (Per Position) ( $T_{VJ} = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_F$	Diode Forward Voltage		1.95		V	$V_{GS} = -4\text{ V}, I_F = 480\text{ A}$	Fig. 7
			3.10			$V_{GS} = -4\text{ V}, I_F = 480\text{ A}, T_{VJ} = 175^\circ\text{C}$	
$t_{RR}$	Reverse Recovery Time		28		ns	$V_{GS} = -4\text{ V}, I_{SD} = 500\text{ A}, V_R = 600\text{ V}$ $di_F/dt = 17\text{ A/ns}, T_{VJ} = 175^\circ\text{C}$	Fig. 32
$Q_{RR}$	Reverse Recovery Charge		4.5		$\mu\text{C}$		
$I_{RRM}$	Peak Reverse Recovery Current		270		A		
$E_{RR}$	Diode Energy $T_{VJ} = 25^\circ\text{C}$ $T_{VJ} = 125^\circ\text{C}$ $T_{VJ} = 175^\circ\text{C}$		1.1		mJ	$V_{DS} = 600\text{ V}, I_D = 500\text{ A},$ $V_{GS} = -4\text{ V}/15\text{ V}, R_{G(ext)} = 1.0\ \Omega,$ $L = 13.7\ \mu\text{H}$	Fig. 14 Note 1
			1.3				
			1.5				
$R_{thJC}$	Diode Thermal Resistance, Junction to Case		0.11	0.13	$^\circ\text{C}/\text{W}$		

Note 1 SiC Schottky diodes do not have reverse recovery energy but still contribute capacitive energy.



## Module Physical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
R <sub>1-2</sub>	Package Resistance, M1		106.5		μΩ	T <sub>C</sub> = 125 °C, Note 2
R <sub>2-3</sub>	Package Resistance, M2		126.3			T <sub>C</sub> = 125 °C, Note 2
L <sub>Stray</sub>	Stray Inductance		4.8		nH	Between Terminals 1 and 3
T <sub>C</sub>	Case Temperature	-40		125	°C	
W	Weight		180		g	
M <sub>S</sub>	Mounting Torque	3	4.5	5	N-m	Baseplate, M6 bolts
		0.9	1.1	1.3		Power Terminals, M4 bolts
V <sub>isol</sub>	Case Isolation Voltage	4			kV	AC, 50 Hz, 1 min
CTI	Comparative Tracking Index	600				
	Clearance Distance	13.07			mm	Terminal to Terminal
		6.00				Terminal to Baseplate
	Creepage Distance	14.27				Terminal to Terminal
		12.34				Terminal to Baseplate

Note 2 Total Effective Resistance (Per Switch Position) = MOSFET R<sub>DS(on)</sub> + Switch Position Package Resistance.

## Temperature Sensor (NTC) Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
R <sub>25</sub>	Resistance at 25°C		4700		Ω	T <sub>NTC</sub> = 25 °C
	Tolerance of R <sub>25</sub>			±1	%	
B <sub>25/85</sub>	Beta Value for 25°C to 85°C		3435		K	
B <sub>0/100</sub>	Beta Value for 0°C to 100°C		3399		K	
	Tolerance of B <sub>25/85</sub>			±1	%	
P <sub>25</sub>	Maximum Power Dissipation			50	mW	

## Steinhart & Hart Coefficients for NTC Resistance & NTC Temperature Computation (T in K)

$$\ln\left(\frac{R}{R_{25}}\right) = A + \frac{B}{T} + \frac{C}{T^2} + \frac{D}{T^3}$$

$$\frac{1}{T} = A_1 + B_1 \ln\left(\frac{R}{R_{25}}\right) + C_1 \ln^2\left(\frac{R}{R_{25}}\right) + D_1 \ln^3\left(\frac{R}{R_{25}}\right)$$

A	B	C	D
-1.289E+01	4.245E+03	-8.749E+04	-9.588E+06

A <sub>1</sub>	B <sub>1</sub>	C <sub>1</sub>	D <sub>1</sub>
3.354E-03	3.001E-04	5.085E-06	2.188E-07

**Typical Performance**

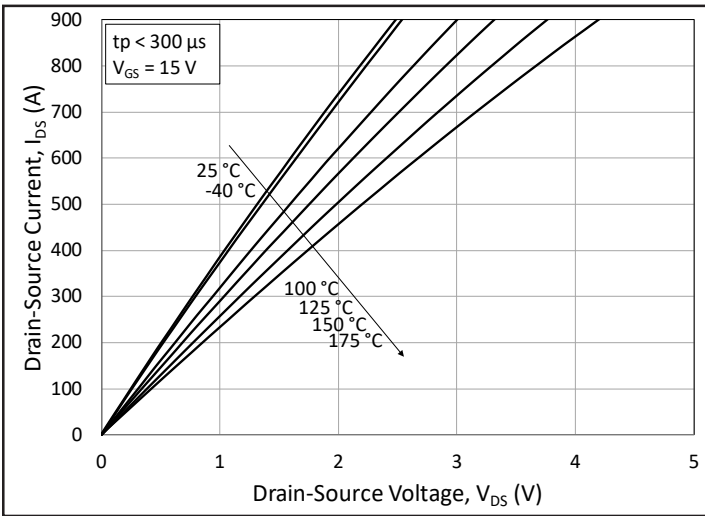


Figure 1. Output Characteristics for Various Junction Temperatures

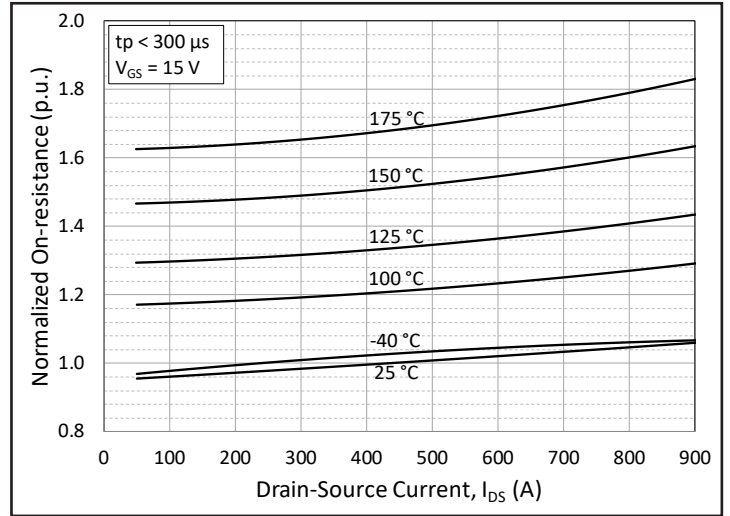


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

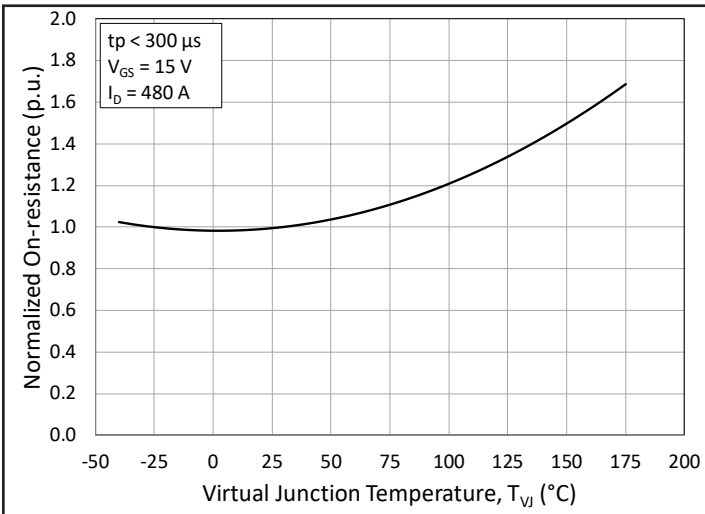


Figure 3. Normalized On-State Resistance vs. Junction Temperature

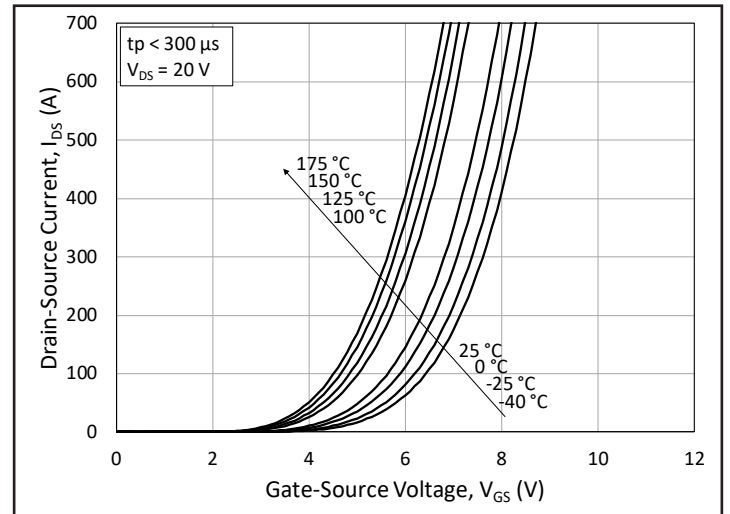


Figure 4. Transfer Characteristic for Various Junction Temperatures

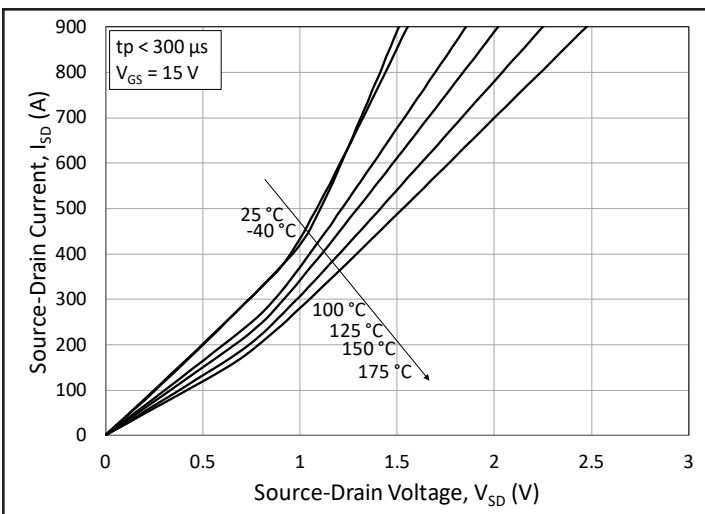


Figure 5. 3<sup>rd</sup> Quadrant Characteristic vs. Junction Temperatures at  $V_{GS} = 15\text{ V}$

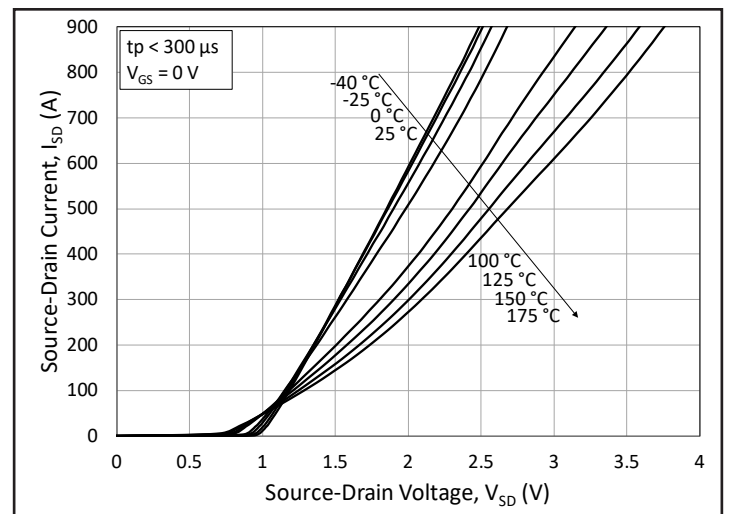


Figure 6. 3<sup>rd</sup> Quadrant Characteristic vs. Junction Temperatures at  $V_{GS} = 0\text{ V}$  (Diode)

**Typical Performance**

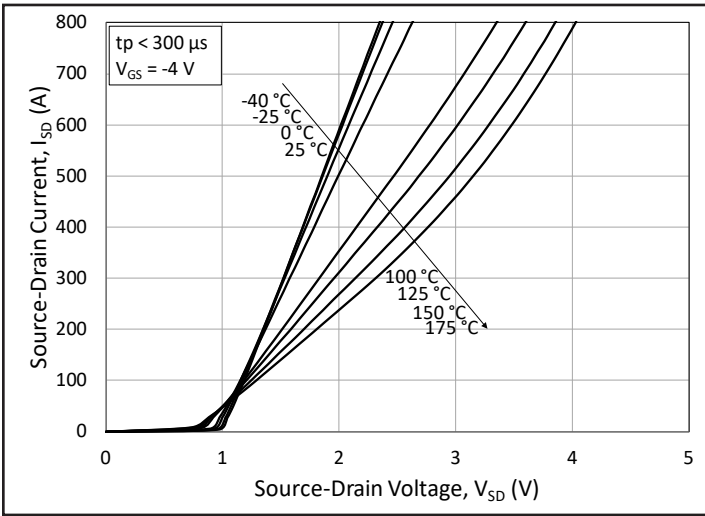


Figure 7. 3<sup>rd</sup> Quadrant Characteristic vs. Junction Temperatures at  $V_{GS} = -4\text{ V}$  (Diode)

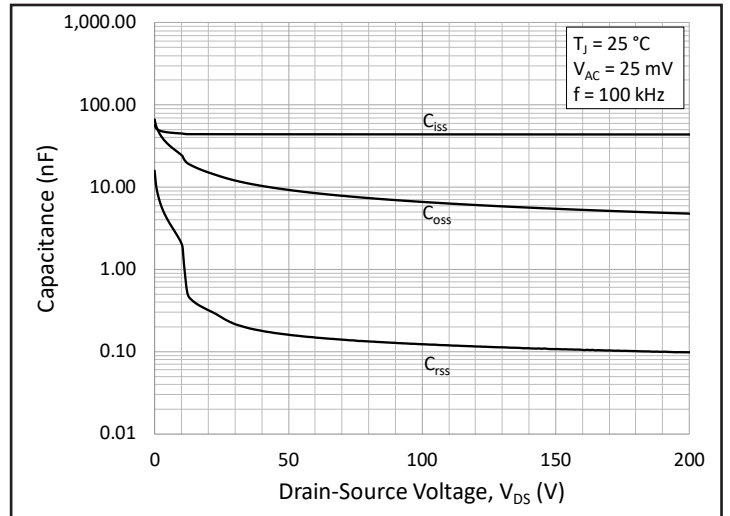


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200V)

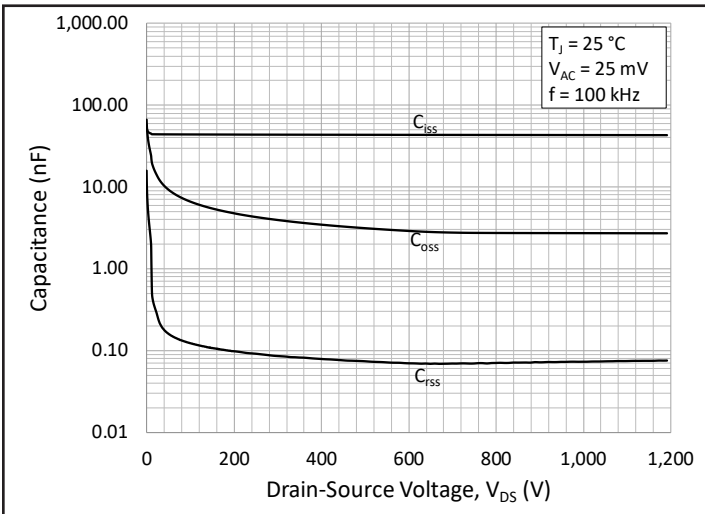


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200V)

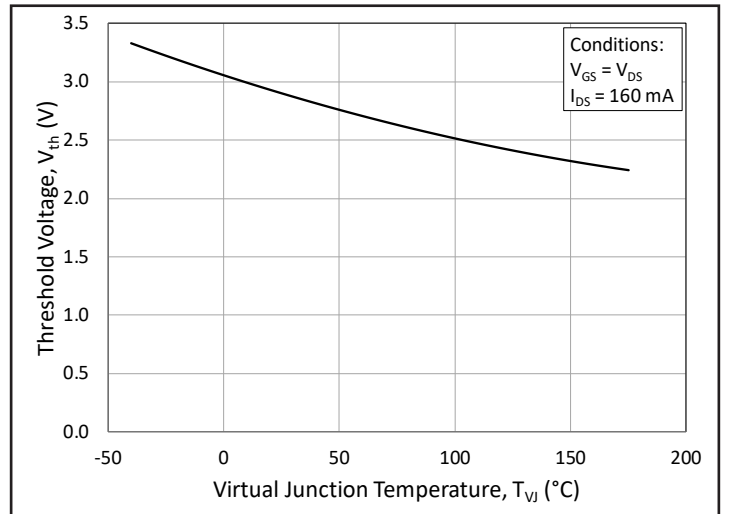


Figure 10. Threshold Voltage vs. Junction Temperature

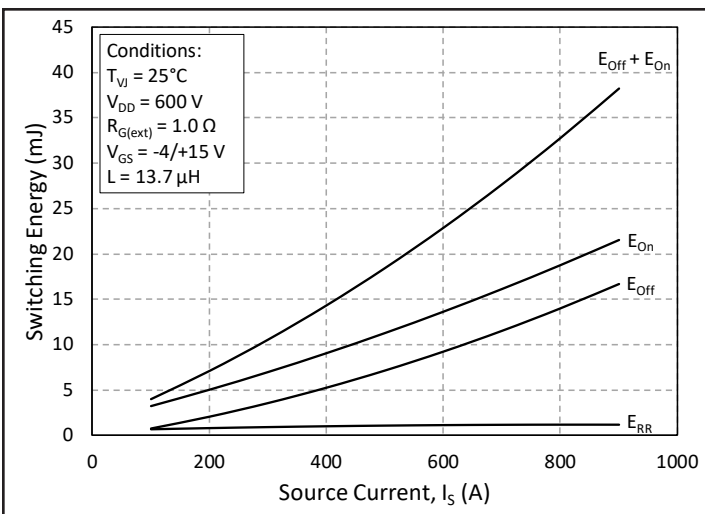


Figure 11. Switching Energy vs. Drain Current ( $V_{DS} = 600\text{ V}$ )

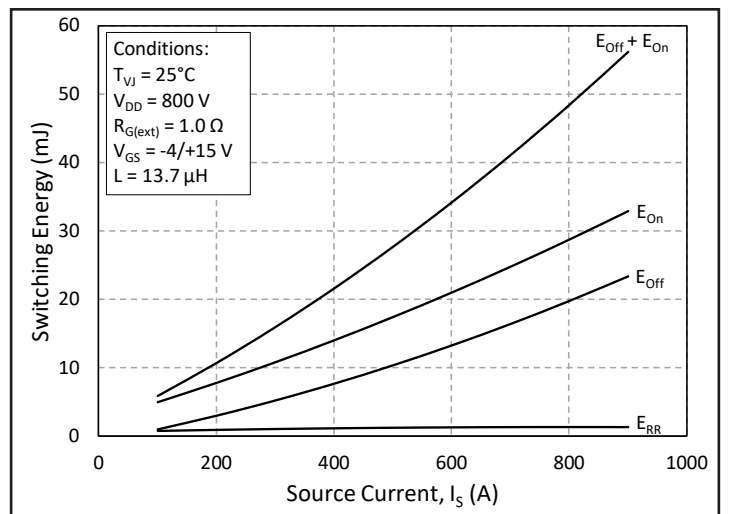


Figure 12. Switching Energy vs. Drain Current ( $V_{DS} = 800\text{ V}$ )

**Typical Performance**

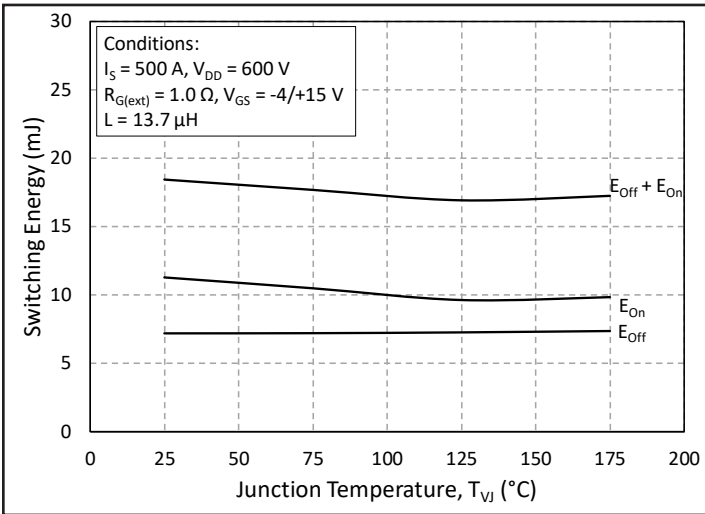


Figure 13. MOSFET Switching Energy vs. Junction Temperature

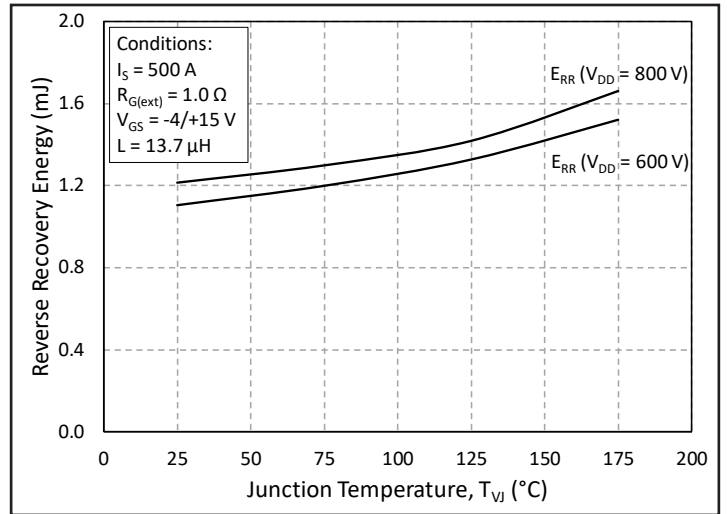


Figure 14. Reverse Recovery Energy vs. Junction Temperature

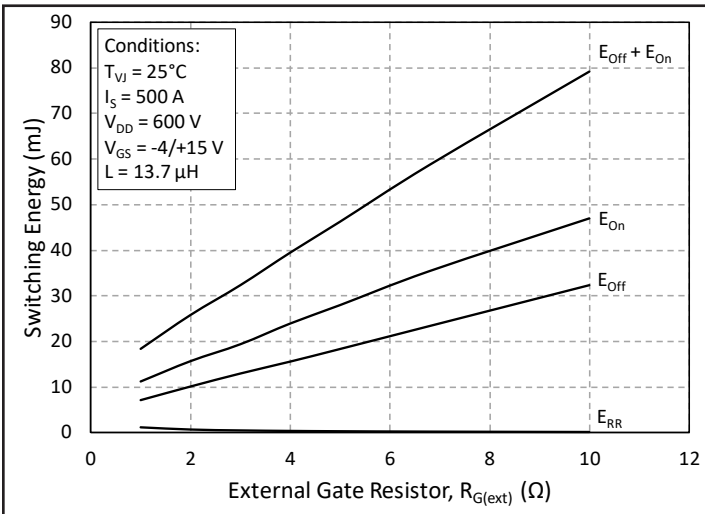


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

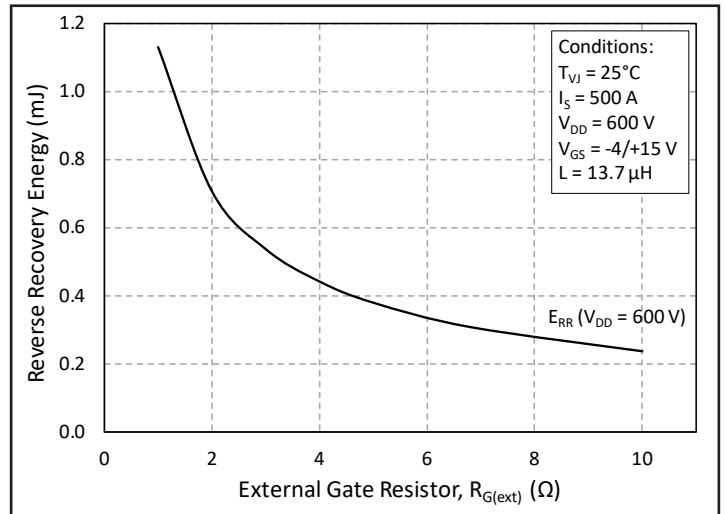


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

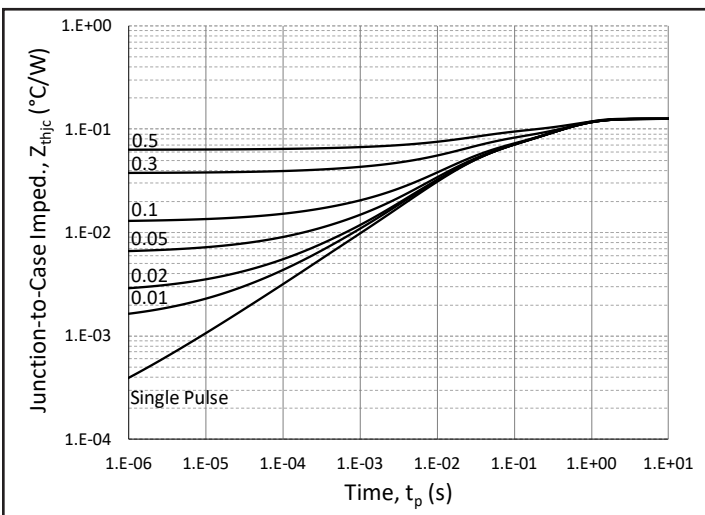


Figure 17. MOSFET Junction to Case Transient Thermal Impedance,  $Z_{thJC}$  (°C/W)

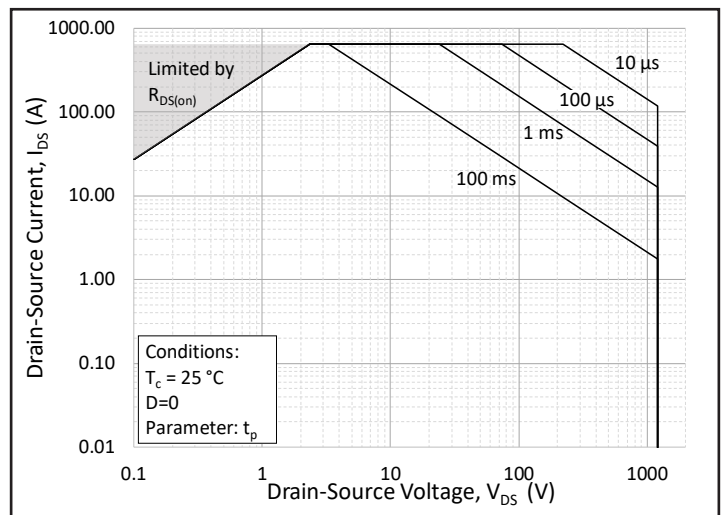


Figure 18. Forward Bias Safe Operating Area (FBSOA)

**Typical Performance**

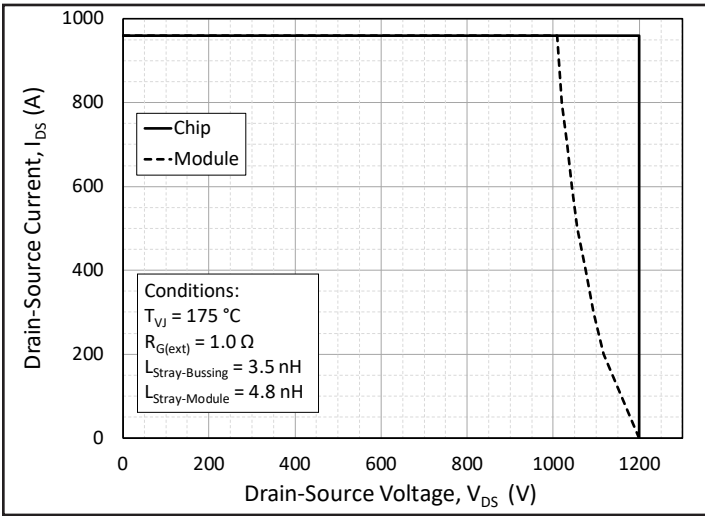


Figure 19. Reverse Bias Safe Operating Area (RBSOA)

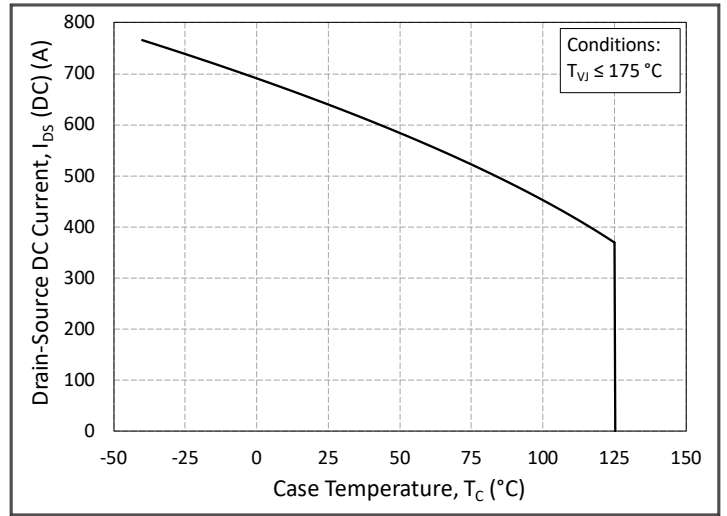


Figure 20. Continuous Drain Current Derating vs. Case Temperature

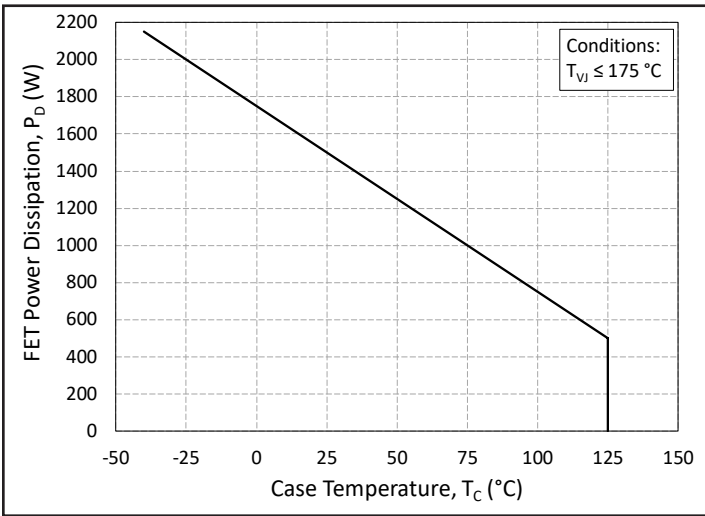


Figure 21. Maximum Power Dissipation Derating vs. Case Temperature

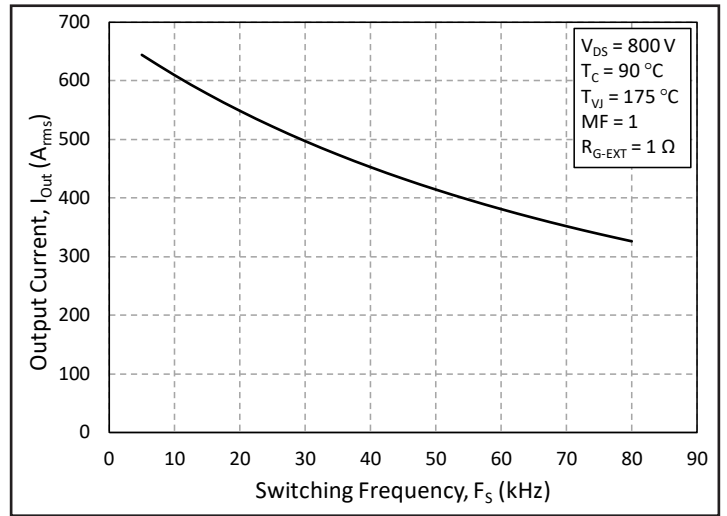


Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

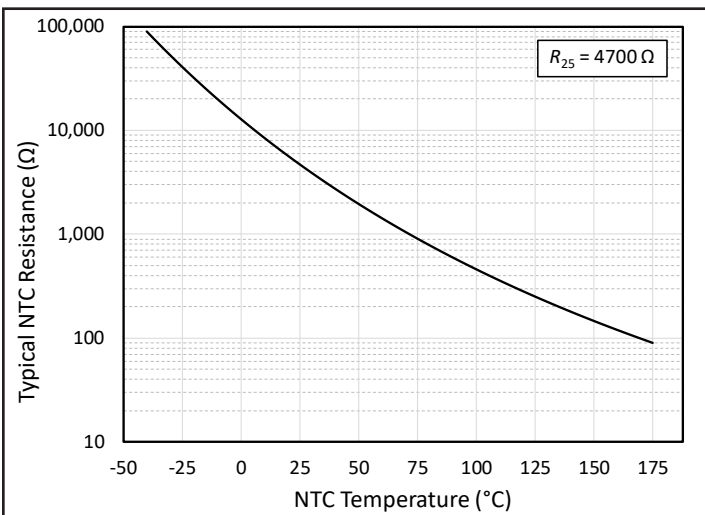


Figure 23. Typical NTC Resistance vs. Temperature



**Timing Characteristics**

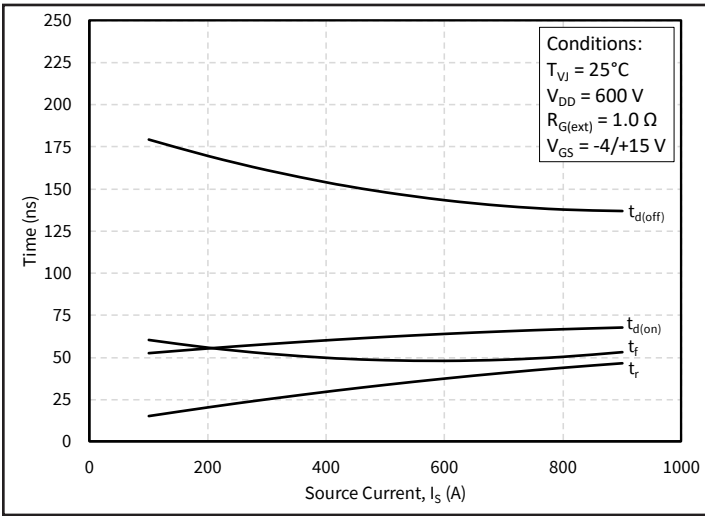


Figure 24. Timing vs. Source Current

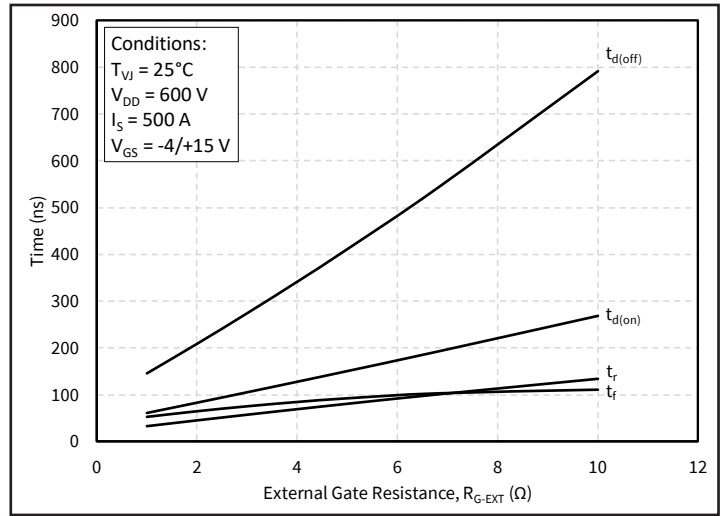


Figure 25. Timing vs. External Gate Resistance

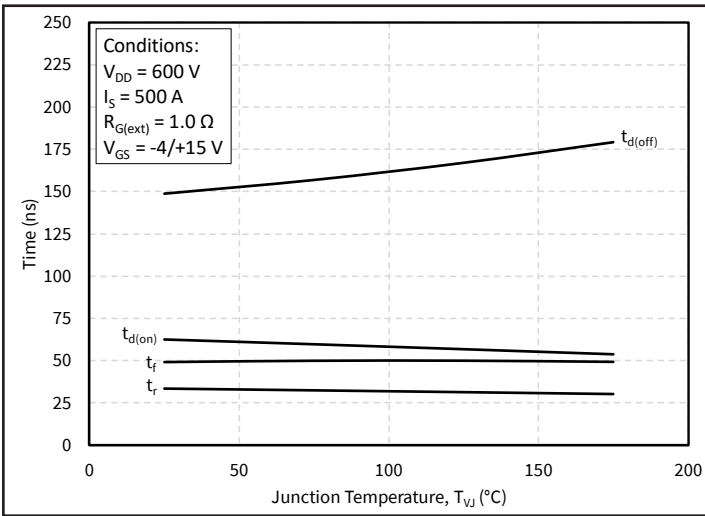


Figure 26. Timing vs. Junction Temperature

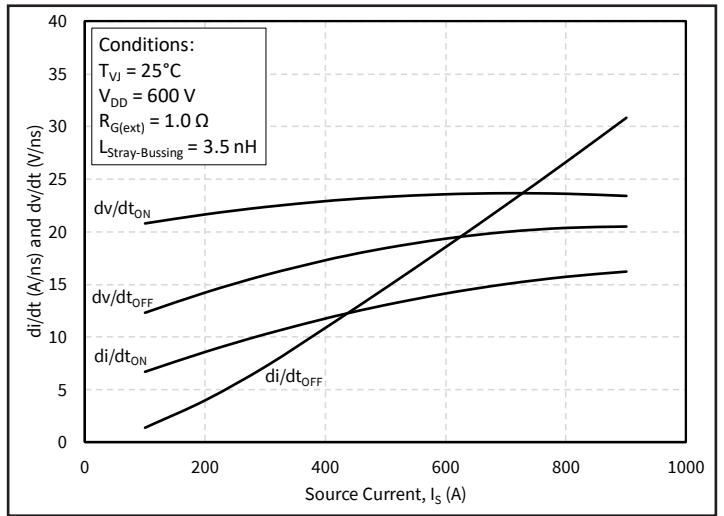


Figure 27. dv/dt and di/dt vs. Source Current

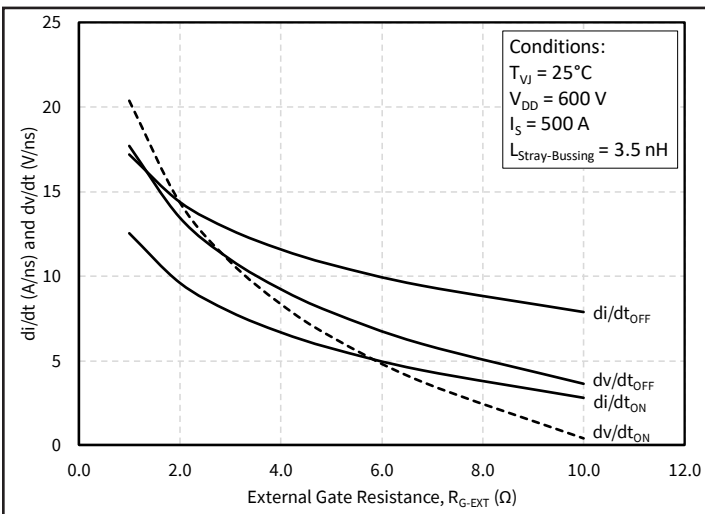


Figure 28. dv/dt and di/dt vs. External Gate Resistance

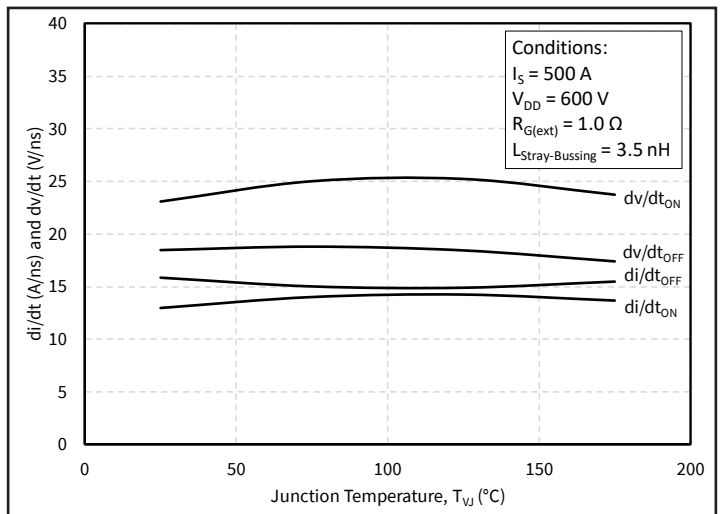


Figure 29. dv/dt and di/dt vs. Junction Temperature





**Definitions**

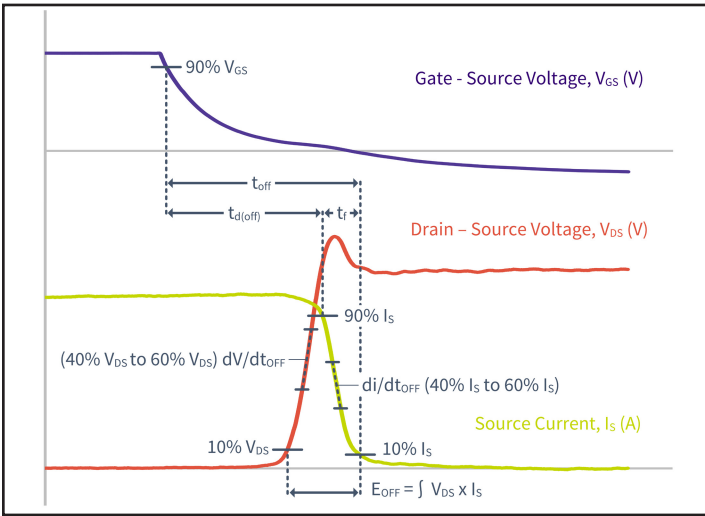


Figure 30. Turn-off Transient Definitions

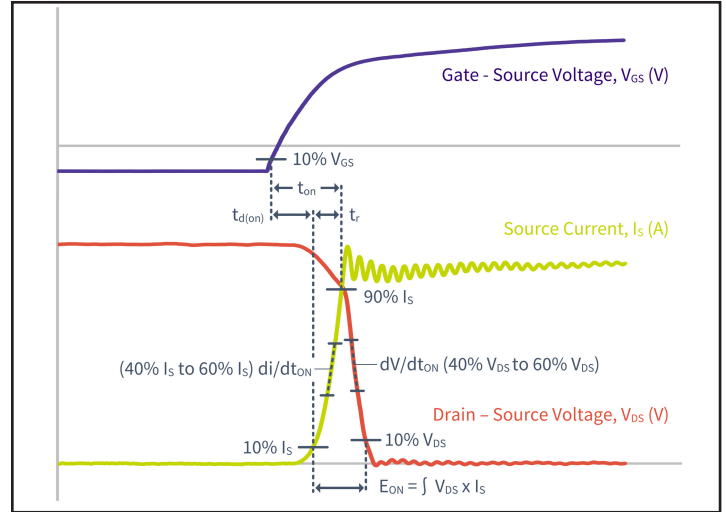


Figure 31. Turn-on Transient Definitions

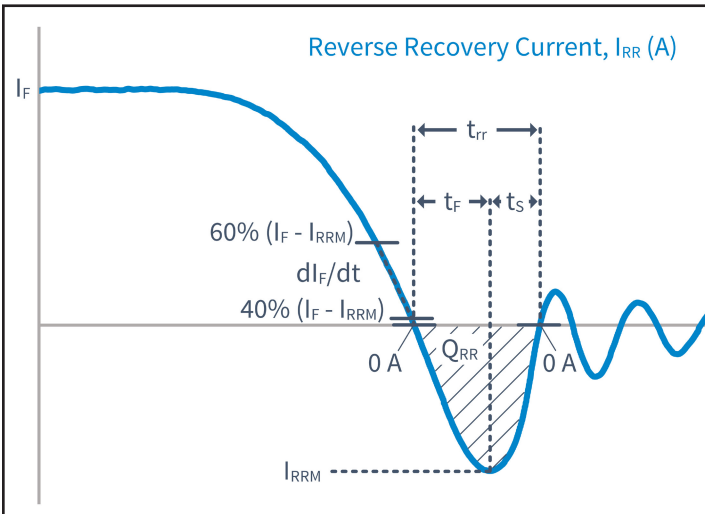


Figure 32. Reverse Recovery Definitions

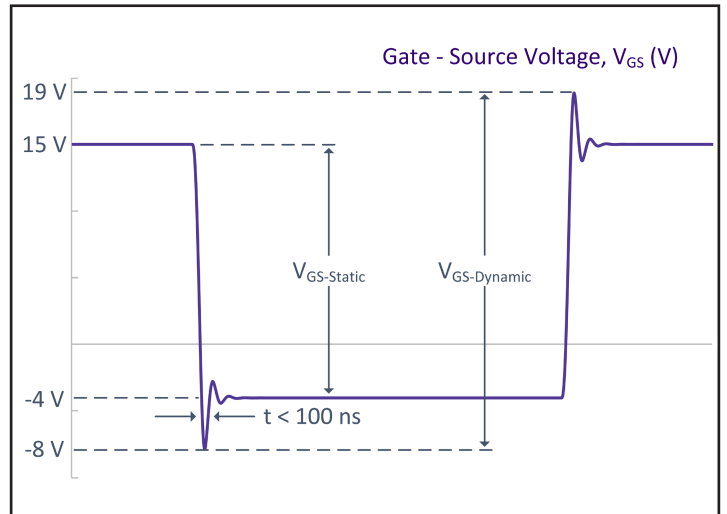
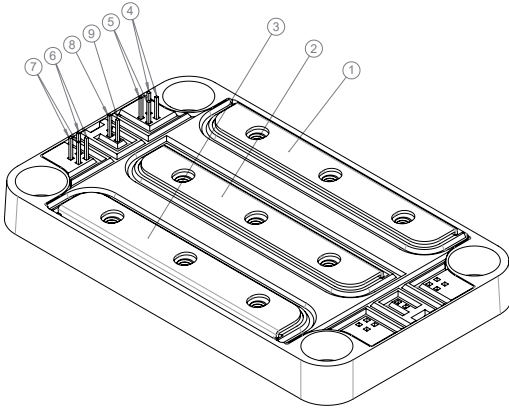


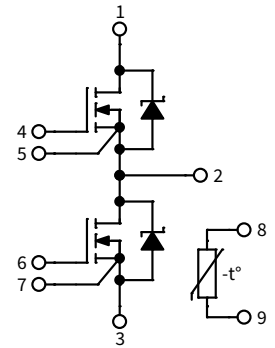
Figure 33.  $V_{GS}$  Transient Definitions



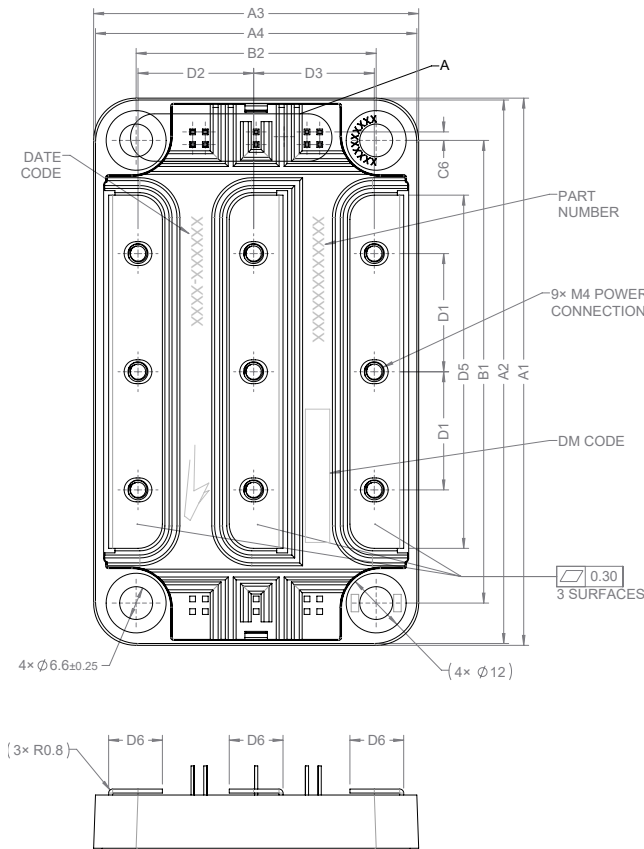
## Schematic and Pin Out



PIN OUT SCHEME	
PIN	LABEL
①	V+
②	Mid
③	V-
④	G1, Top row pins (2)
⑤	K1, Bottom row pins (2)
⑥	G2, Top row pins (2)
⑦	K2, Bottom row pins (2)
⑧	NTC1
⑨	NTC2

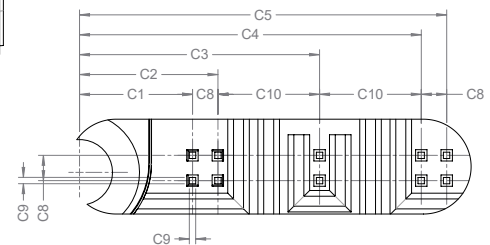
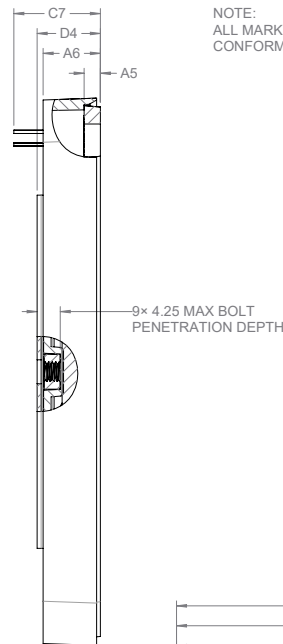


## Package Dimensions (mm)



NOTE:  
ALL MARKINGS SHALL  
CONFORM TO PRC-00786.

DIMENSION TABLE		
SYMBOL	DIMENSION	TOLERANCE
A1	110.00	$\pm 0.60$
A2	109.25	$\pm 0.60$
A3	65.00	$\pm 0.60$
A4	64.25	$\pm 0.60$
A5	3.25	$\pm 0.30$
A6	11.45	$\pm 0.60$
B1	93.00	$\pm 0.30$
B2	48.00	$\pm 0.30$
C1	11.30	$\pm 0.40$
C2	13.84	$\pm 0.40$
C3	24.00	$\pm 0.40$
C4	34.16	$\pm 0.40$
C5	36.70	$\pm 0.40$
C6	1.71	$\pm 0.40$
C7	17.30	$\pm 0.50$
C8	2.54	$\pm 0.30$
C9	0.64	$\pm 0.30$
C10	10.16	$\pm 0.40$
D1	23.75	$\pm 0.50$
D2	23.13	$\pm 0.50$
D3	24.13	$\pm 0.50$
D4	12.20	$\pm 0.50$
D5	71.00	$\pm 0.30$
D6	10.75	$\pm 0.30$



DETAIL A  
SCALE: 4:1

## Supporting Links & Tools

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- [CGD1700HB3P-HM3 Evaluation Gate Driver](#)
- [CGD12HB00D: Differential Transceiver Board](#)
- [CPWR-AN35: Thermal Interface Material Application Note](#)
- [CPWR-AN39: KIT-CRD-CIL12N-HM User Guide](#)
- [KIT-CRD-CIL12N-HM: Dynamic Performance Evaluation Board for the HM2 and HM3 Module](#)
- [CAS480M12HM3 PLECS Models](#)

## Notes

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