

74VHC125 Quad Buffer with TRI-STATE® Outputs

General Description

The VHC125 contains four independent non-inverting buffers with TRI-STATE outputs. It is an advanced high-speed CMOS device fabricated with silicon gate CMOS technology and achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

An input protection circuit insures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

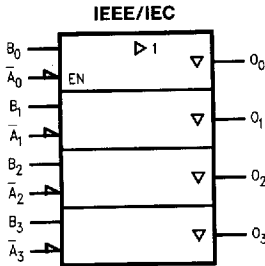
- Lower power dissipation:
 $I_{CC} = 4 \mu A$ (max) at $T_A = 25^\circ C$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- All inputs are equipped with a power down protection function
- Balanced propagation delays: $t_{PLH} \cong t_{PHL}$
- Low noise: $V_{OLP} = 0.8V$ (max)
- Pin and function compatible with 74HC125

Ordering Code: See Section 6

Commercial	Package Number	Package Description
74VHC125M	M14A	14-Lead Molded JEDEC SOIC
74VHC125SJ	M14D	14-Lead Molded EIAJ SOIC
74VHC125MTC	MTC14	14-Lead Molded JEDEC Type 1 TSSOP
74VHC125N	N14A	14-Lead Molded DIP

Note: Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

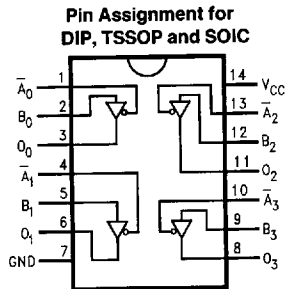
Logic Symbol



TL/F/11632-1

Pin Names	Description
\bar{A}_n, B_n	Inputs
O_n	Outputs

Connection Diagram



TL/F/11632-2

Function Table

Inputs		Output
A_n	B_n	O_n
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 Z = HIGH Impedance
 X = Immaterial

Absolute Maximum Ratings (Note 1)

Supply Voltage (V _{CC})	-0.5V to +7.0V
DC Input Voltage (V _{IN})	-0.5V to +7.0V
DC Output Voltage (V _{OUT})	-0.5V to V _{CC} + 0.5V
Input Diode Current (I _{IK})	-20 mA
Output Diode Current (I _{OK})	±20 mA
DC Output Current (I _{OUT})	±25 mA
DC V _{CC} /GND Current (I _{CC})	±50 mA
Storage Temperature (T _{STG})	-65°C to +150°C
Lead Temperature (T _L) (Soldering, 10 seconds)	260°C

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V _{CC})	2.0V to +5.5V
Input Voltage (V _{IN})	0V to +5.5V
Output Voltage (V _{OUT})	0V to V _{CC}
Operating Temperature (T _{OPR})	-40°C to +85°C
Input Rise and Fall Time (t _r , t _f)	
V _{CC} = 3.3V ±0.3V	0 ~ 100 ns/V
V _{CC} = 5.0V ±0.5V	0 ~ 20 ns/V

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V _{CC} (V)	74VHC				Units	Conditions	
			T _A = 25°C			T _A = -40°C to +85°C			
			Min	Typ	Max	Min			Max
V _{IH}	High Level Input Voltage	2.0 3.0-5.5	1.50 0.7 V _{CC}			1.50 0.7 V _{CC}	V		
V _{IL}	Low Level Input Voltage	2.0 3.0-5.5		0.50 0.3 V _{CC}		0.50 0.3 V _{CC}	V		
V _{OH}	High Level Output Voltage	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4	V	V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA	
		3.0 4.5	2.58 3.94			2.48 3.80	V		I _{OH} = -4 mA I _{OH} = -8 mA
V _{OL}	Low Level Output Voltage	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1	0.1 0.1 0.1	V	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA	
		3.0 4.5			0.36 0.36	0.44 0.44	V		I _{OL} = 4 mA I _{OL} = 8 mA
I _{OZ}	TRI-STATE Output Off-State Current	5.5		±0.25		±2.5	μA	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	
I _{IN}	Input Leakage Current	0-5.5		±0.1		±1.0	μA	V _{IN} = 5.5V or GND	
I _{CC}	Quiescent Supply Current	5.5		4.0		40.0	μA	V _{IN} = V _{CC} or GND	

DC Characteristics for 'VHC Family Devices: See Section 2 for Waveforms

Symbol	Parameter	V _{CC} (V)	74VHC		Units	Conditions	Fig. No.
			T _A = 25°C				
			Typ	Limits			
V _{OLP} **	Quiet Output Maximum Dynamic V _{OL}	5.0	0.5	0.8	V	C _L = 50 pF	2-11, 12
V _{OLV} **	Quiet Output Minimum Dynamic V _{OL}	5.0	-0.5	-0.8	V	C _L = 50 pF	2-11, 12
V _{IHD} **	Minimum High Level Dynamic Input Voltage	5.0		3.5	V	C _L = 50 pF	2-11, 12
V _{ILD} **	Maximum High Level Dynamic Input Voltage	5.0		1.5	V	C _L = 50 pF	2-11, 12

**Parameter guaranteed by design.

AC Electrical Characteristics for 'VHC Family Devices: See Section 2 for Waveforms

Symbol	Parameter	V _{CC} (V)	74VHC		74VHC		Units	Conditions	Fig. No.	
			T _A = 25°C			T _A = -40°C to +85°C				
			Min	Typ	Max	Min				Max
t _{PLH} , t _{PHL}	Propagation Delay Time	3.3 ± 0.3	5.6	8.0	1.0	9.5	ns	C _L = 15 pF C _L = 50 pF	2-5	
		5.0 ± 0.5	8.1	11.5	1.0	13.0				
			3.8	5.5	1.0	6.5	ns	C _L = 15 pF C _L = 50 pF		
			5.3	7.5	1.0	8.5				
t _{PZL} , t _{PZH}	TRI-STATE Output Enable Time	3.3 ± 0.3	5.4	8.0	1.0	9.5	ns	R _L = 1 kΩ C _L = 15 pF C _L = 50 pF	2-7, 8	
		5.0 ± 0.5	7.9	11.5	1.0	13.0				
			3.6	5.1	1.0	6.0	ns	C _L = 15 pF C _L = 50 pF		
			5.1	7.1	1.0	8.0				
t _{PLZ} , t _{PHZ}	TRI-STATE Output Disable Time	3.3 ± 0.3	9.5	13.2	1.0	15.0	ns	R _L = 1 kΩ C _L = 50 pF C _L = 50 pF	2-7, 8	
		5.0 ± 0.5	6.1	8.8	1.0	10.0				
t _{OSLH} , t _{OSSL}	Output to Output Skew	3.3 ± 0.3		1.5		1.5	ns	(Note 1) C _L = 50 pF C _L = 50 pF		
		5.0 ± 0.5		1.0		1.0				
C _{IN}	Input Capacitance		4	10		10	pF	V _{CC} = Open		
C _{OUT}	Output Capacitance		6				pF	V _{CC} = 5.0V		
C _{PD}	Power Dissipation Capacitance		14				pF	(Note 2)		

Note 1: Parameter guaranteed by design. t_{OSLH} = |t_{PLHmax} - t_{PLHmin}|; t_{OSSL} = |t_{PHLmax} - t_{PHLmin}|.

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (OPR.) = C_{PD} * V_{CC} * f_{IN} + I_{CC}/4 (per bit).