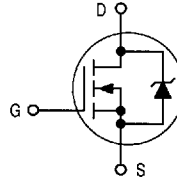


*Designer's™ Data Sheet*  
**Fully Isolated TMOS E-FET™**  
**High Energy Power MOSFET**  
**N-Channel Enhancement-Mode Silicon Gate**

This advanced TMOS E-FET is designed to withstand high energy in the avalanche mode and operate reliably. This new high energy device also offers a drain-to-source diode with fast recovery time. The device is designed for high speed switching applications such as switching power supplies, PWM motor controls and other inductive loads. The avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients. The device is housed in a fully isolated TO-220 package which has an isolation voltage rating of up to 4500 Volts.

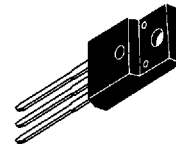
- Avalanche Energy Specified
- Low Stored Gate Charge for Efficient Switching
- Source-to-Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode
- Isolated Version of the MTP50N06E



**MTA30N06E**

Motorola Preferred Device

**TMOS POWER FET**  
**30 AMPERES**  
**60 VOLTS**  
 **$R_{DS(on)} = 0.025 \text{ OHM MAX}$**



**CASE 221D-02, Style 1**  
**(ISOLATED TO-220 TYPE)**

**MAXIMUM RATINGS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	60	Volts
Drain-to-Gate Voltage ( $R_{GS} = 1.0 \text{ M}\Omega$ )	$V_{DGR}$	60	Volts
Gate-to-Source Voltage — Continuous	$V_{GS}$	$\pm 20$	Volts
Drain Current — Continuous	$I_D$	30	Amps
— Continuous @ $100^\circ\text{C}$	$I_{D1}$	20	
— Pulsed	$I_{DM}$	160	
RMS Isolation Voltage ( $t = 1$ second, R.H. $\leq 30\%$ , $T_A = 25^\circ\text{C}$ )	$V_{ISO1}$ $V_{ISO2}$ $V_{ISO3}$	4500 3500 1500	Volts
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	50 0.4	Watts $\text{W}/^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy — Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 25 \text{ V}$ , $V_{GS} = 10 \text{ V}$ , Peak $I_L = 30 \text{ A}$ , $L = 889 \mu\text{H}$ , $R_G = 25 \Omega$ )	$E_{AS}$	400	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

**Designer's Data for "Worst Case" Conditions** — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

# MTA30N06E

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Drain-to-Source Breakdown Voltage (V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	60 —	— 65	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0) (V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>	— —	— —	10 100	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ± 20 Vdc, V <sub>DS</sub> = 0)	I <sub>GSS</sub>	—	—	100	nAdc

### ON CHARACTERISTICS (1)

Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Threshold Temperature Coefficient (negative)	V <sub>GS(th)</sub>	2.0 —	— 7.0	4.0 —	Vdc mV/°C
Static Drain-to-Source On-Resistance (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 25 Adc)	R <sub>DS(on)</sub>	—	0.017	0.025	Ohm
Drain-to-Source On-Voltage (V <sub>GS</sub> = 10 Vdc) (I <sub>D</sub> = 50 Adc) (I <sub>D</sub> = 25 Adc, T <sub>J</sub> = 100°C)	V <sub>DS(on)</sub>	— —	— —	1.6 1.2	Vdc
Forward Transconductance (V <sub>DS</sub> ≥ 8.0 Vdc, I <sub>D</sub> = 25 Adc)	g <sub>FS</sub>	17	—	—	mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0, f = 1.0 MHz)	C <sub>iss</sub>	—	2500	3500	pF
Output Capacitance		C <sub>oss</sub>	—	1000	1400	
Transfer Capacitance		C <sub>rss</sub>	—	250	500	

### SWITCHING CHARACTERISTICS (2)

Turn-On Delay Time	(V <sub>DD</sub> = 25 V, I <sub>D</sub> = 50 A, V <sub>GS</sub> = 10 V, R <sub>G</sub> = 9.1 Ω)	t <sub>d(on)</sub>	—	23	46	ns
Rise Time		t <sub>r</sub>	—	160	320	
Turn-Off Delay Time		t <sub>d(off)</sub>	—	70	140	
Fall Time		t <sub>f</sub>	—	120	240	
Gate Charge	(V <sub>DS</sub> = 48 V, I <sub>D</sub> = 50 A, V <sub>GS</sub> = 10 V)	Q <sub>T</sub>	—	75	100	nC
		Q <sub>1</sub>	—	15	—	
		Q <sub>2</sub>	—	45	—	
		Q <sub>3</sub>	—	30	—	

### SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I <sub>S</sub> = 50 A, V <sub>GS</sub> = 0)	V <sub>SD</sub>	—	1.1	2.5	Vdc
	(I <sub>S</sub> = 50 A, V <sub>GS</sub> = 0, T <sub>J</sub> = 125°C)		—	1.0	—	
Reverse Recovery Time	(I <sub>S</sub> = 25 A, di/dt = 100 A/μs)	t <sub>rr</sub>	—	120	—	ns

### INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from screw on tab to center of die)	L <sub>D</sub>	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L <sub>S</sub>	—	7.5	—	

### ISOLATION CAPACITANCE

Isolation Capacitance, Drain-to-Heat Sink	C <sub>iso</sub>	—	15	—	pF
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(1) Pulse Test: Pulse Width ≤ 300 μs max, Duty Cycle = 2.0%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

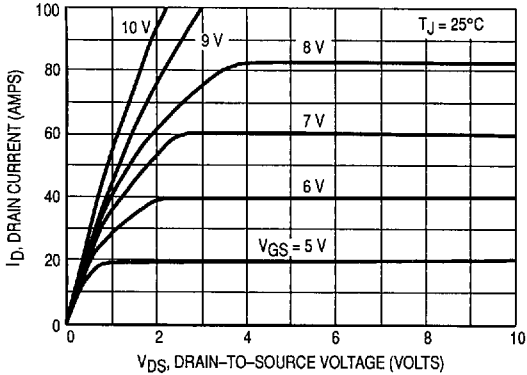


Figure 1. On-Region Characteristics

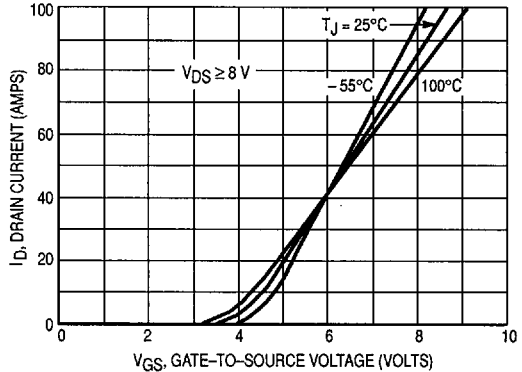


Figure 2. Transfer Characteristics

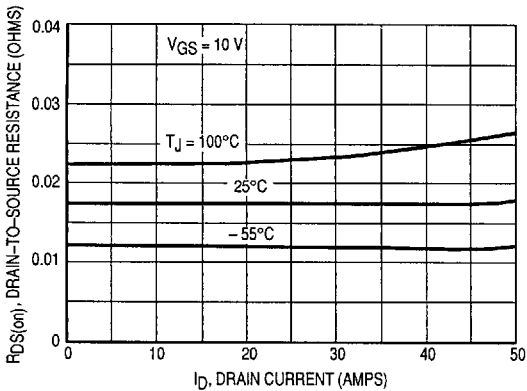


Figure 3. On-Resistance versus Drain Current

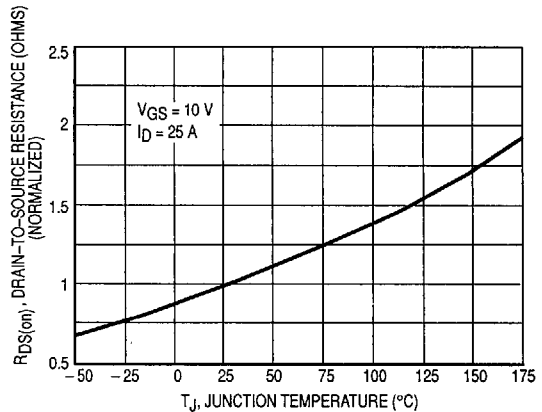


Figure 4. On-Resistance Variation With Temperature

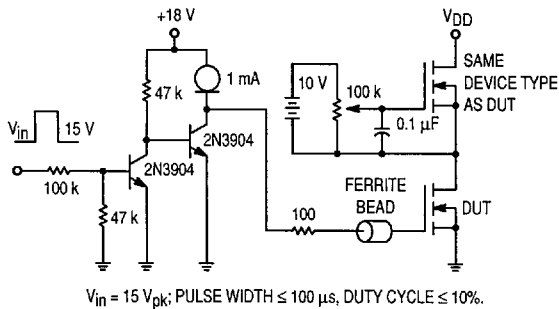


Figure 5. Gate Charge Test Circuit

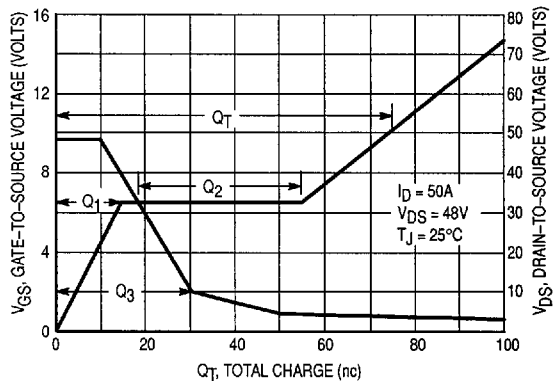


Figure 6. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

SAFE OPERATING AREA INFORMATION

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance—General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current,  $I_{DM}$  and the breakdown voltage,  $BV_{DSS}$ . The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

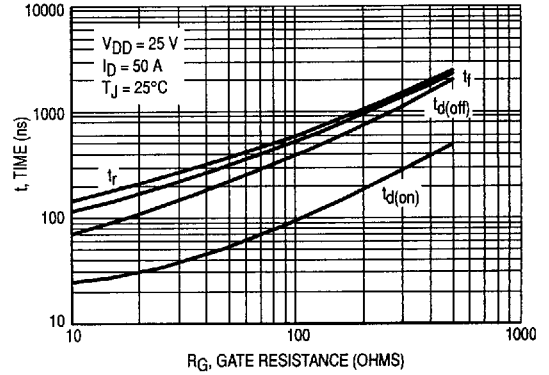


Figure 7. Resistive Switching Time Variation versus Gate Resistance

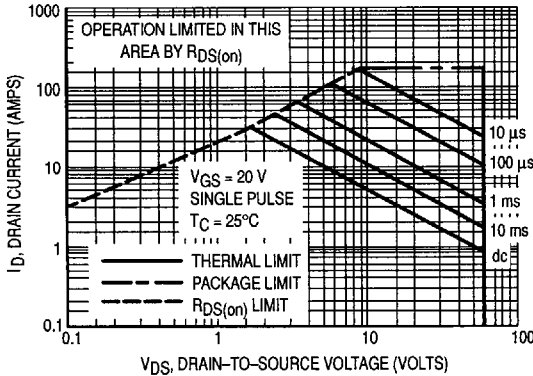


Figure 8. Maximum Rated Forward Biased Safe Operating Area

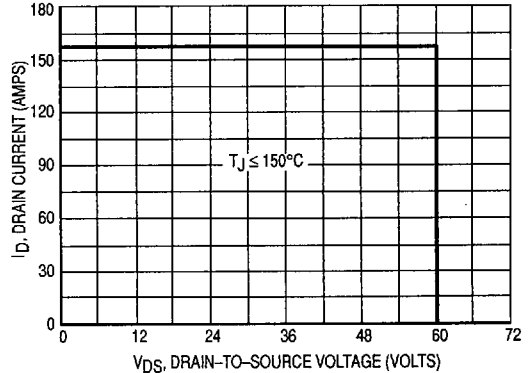


Figure 9. Maximum Rated Switching Safe Operating Area

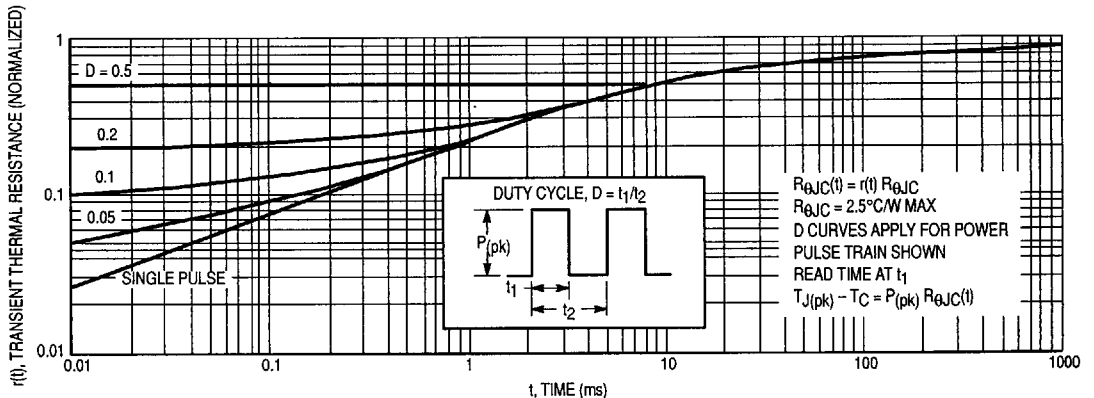


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of  $I_{FM}$  and peak  $V_{DS}$  for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so  $di_s/dt$  is specified with a maximum value. Higher values of  $di_s/dt$  require an appropriate derating of  $I_{FM}$ , peak  $V_{DS}$  or both. Ultimately  $di_s/dt$  is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during  $t_{rr}$  as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$  is the peak drain-to-source voltage that the device must sustain during commutation;  $I_{FM}$  is the maximum forward source-drain diode current just prior to the onset of commutation.

$V_R$  is specified at rated  $V_{(BR)DSS}$  to ensure that the CSOA stress is maximized as  $I_S$  decays from  $I_{RM}$  to zero.

$R_{GS}$  should be minimized during commutation.  $T_J$  has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums.  $dV_{DS}/dt$  in excess of 10 V/ns was attained with  $di_s/dt$  of 400 A/ $\mu$ s.

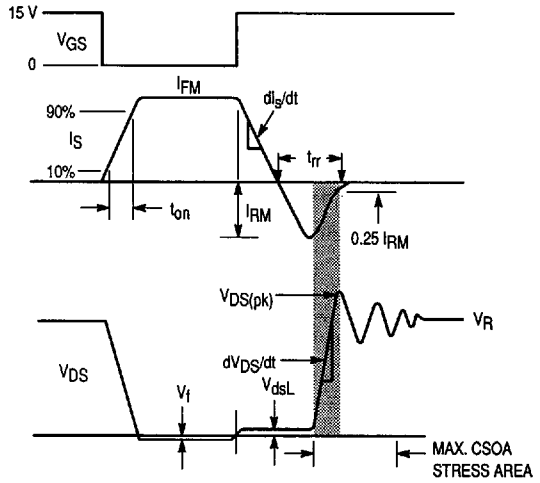


Figure 11. Commutating Waveforms

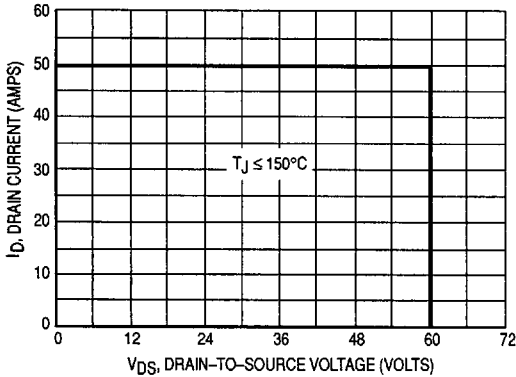


Figure 12. Commutating Safe Operating Area (CSOA)

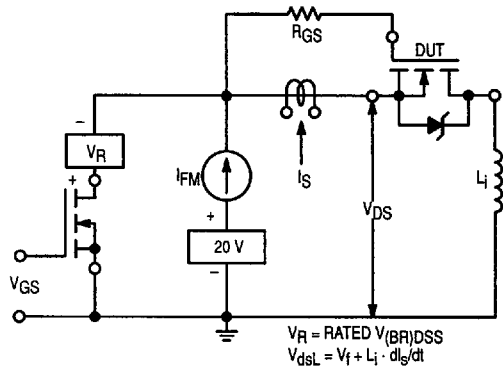
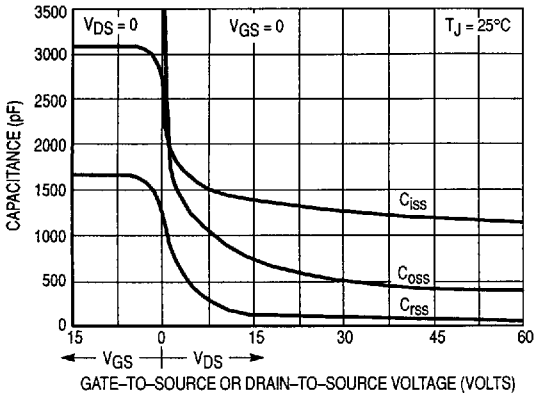
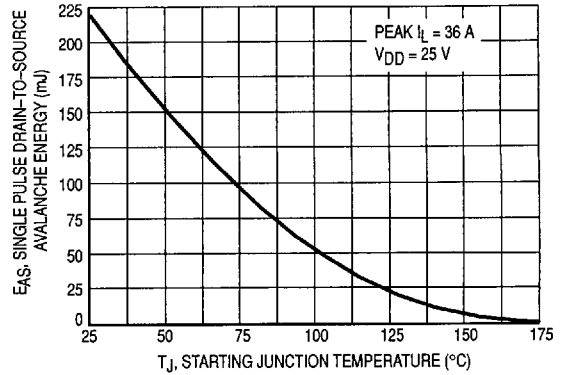


Figure 13. Commutating Safe Operating Area Test Circuit

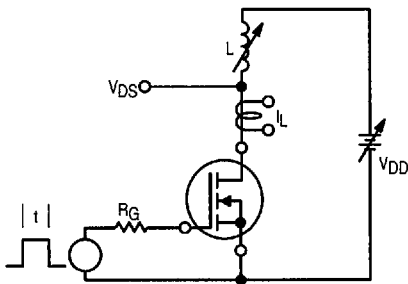
**MTA30N06E**



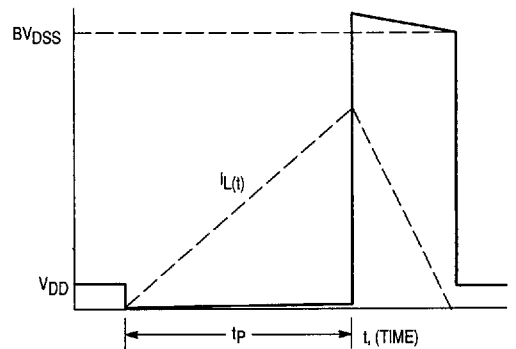
**Figure 14. Capacitance Variation**



**Figure 15. Maximum Avalanche Energy versus Starting Junction Temperature**

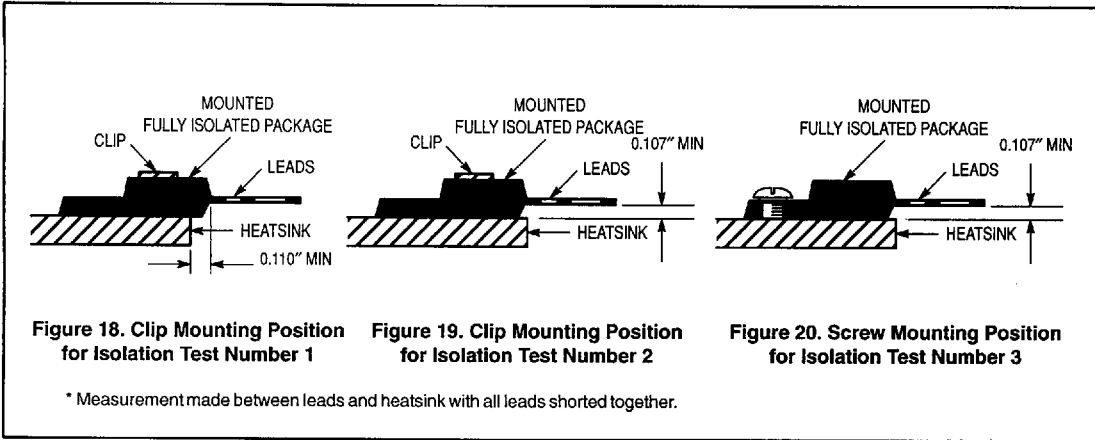


**Figure 16. Unclamped Inductive Switching Test Circuit**

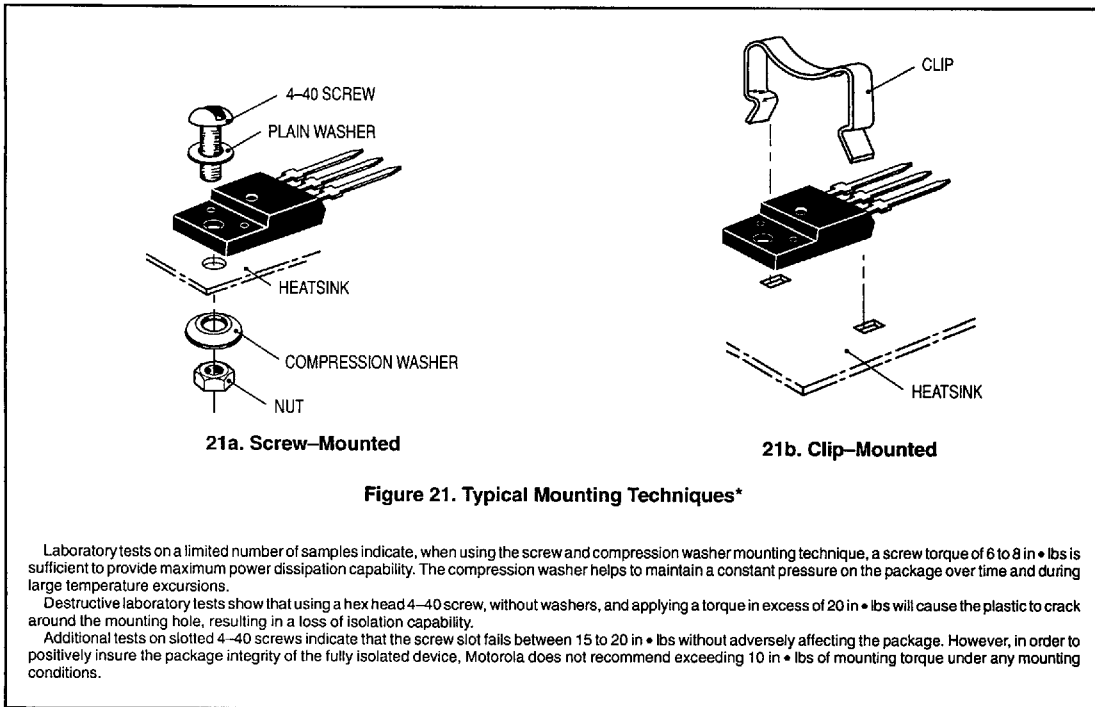


**Figure 17. Unclamped Inductive Switching Waveforms**

TEST CONDITIONS FOR ISOLATION TESTS\*



MOUNTING INFORMATION\*\*



\*\* For more information about mounting power semiconductors see Application Note AN1040.