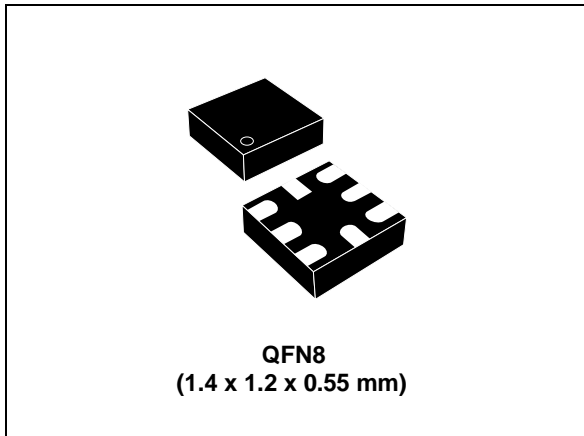


## 2-bit dual supply level translator without direction control pin, push-pull output

Datasheet - production data



### Features

- 45 MHz: 90 Mbps (max.) data rate at  $V_L = 1.8\text{ V}$ ,  $V_{CC} = 3.3\text{ V}$
- Bi-directional level translation without direction control pin
- Wide voltage range ( $V_L \leq V_{CC}$ ):
  - $V_L$  ranges from 1.65 to 3.6 V
  - $V_{CC}$  ranges from  $V_L$  to 5.5 V
- Totem pole driving
- 5.5 V tolerant Enable pin

- ESD performance on all pins:  $\pm 2\text{ kV HBM}$
- Small package and footprint  
QFN8 1.4 x 1.2 x 0.55 mm

### Applications

- Low-voltage system level translation
- Mobile phones and other mobile devices

### Description

The ST2129B device is a 2-bit dual supply level translator which provides the level shifting capability to allow data transfer in a multi-voltage system. Externally applied voltages,  $V_{CC}$  and  $V_L$ , set the logic levels on either side of the device. Its architecture allows bi-directional level translation without a control pin.

The ST2129B device accepts  $V_L$  from 1.65 to 3.6 V and  $V_{CC}$  from  $V_L$  to 5.5 V, making it ideal for data transfer between low-voltage ASICs/PLD and higher voltage systems. This device has a tristate output mode which can be used to disable all I/Os.

**Table 1. Device summary**

Order code	Package	Packing	Package topmark
ST2129BQTR	QFN8 (1.4 x 1.2 x 0.55 mm)	Tape and reel (3000 parts per reel)	1A

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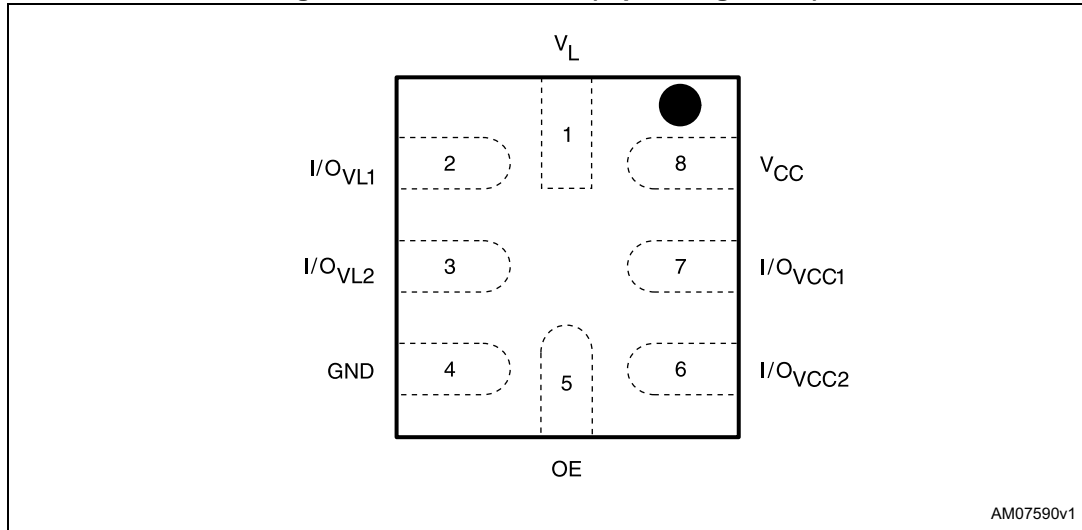
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# 1 Pin settings

## 1.1 Pin connection

Figure 1. Pin connection (top through view)



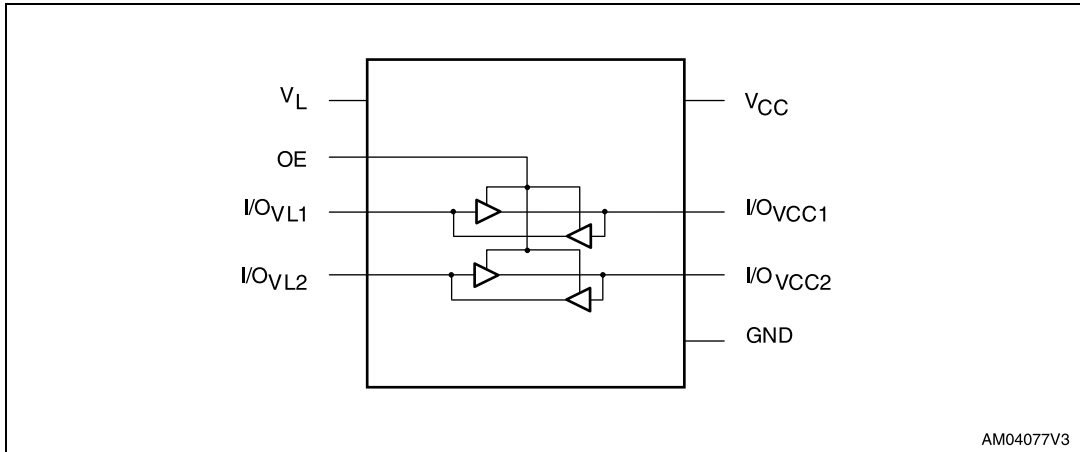
## 1.2 Pin description

Table 2. Pin description

Pin number	Symbol	Name and function
1	$V_L$	Supply voltage
2	$I/O_{VL1}$	Data input/output
3	$I/O_{VL2}$	Data input/output
4	GND	Ground
5	OE	Output enable
6	$I/O_{VCC2}$	Data input/output
7	$I/O_{VCC1}$	Data input/output
8	$V_{CC}$	Supply voltage

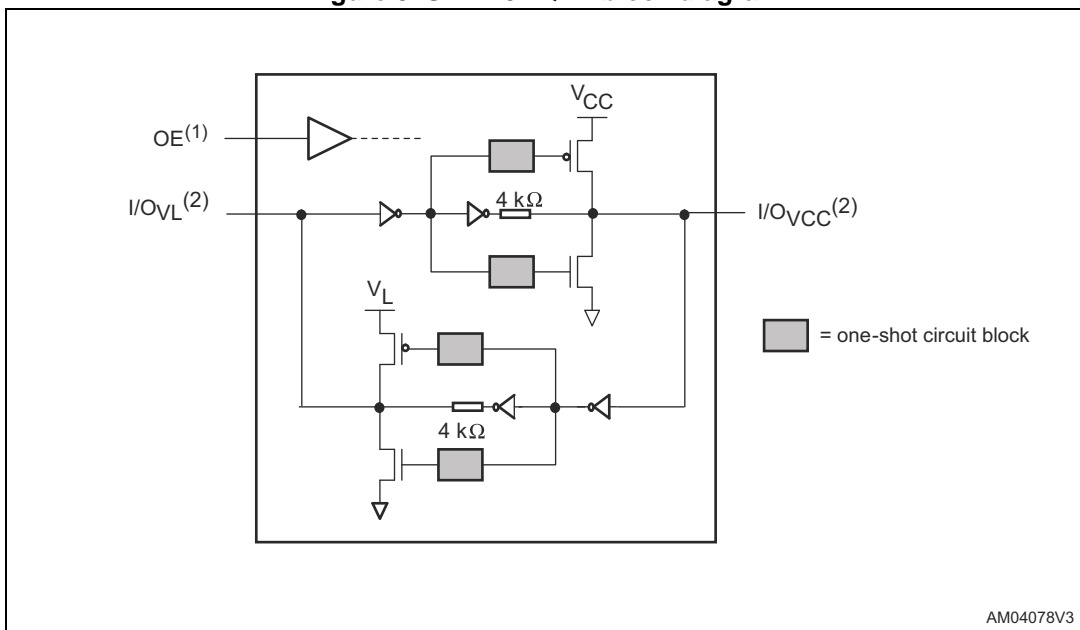
## 2 Logic diagram

Figure 2. Logic block diagram



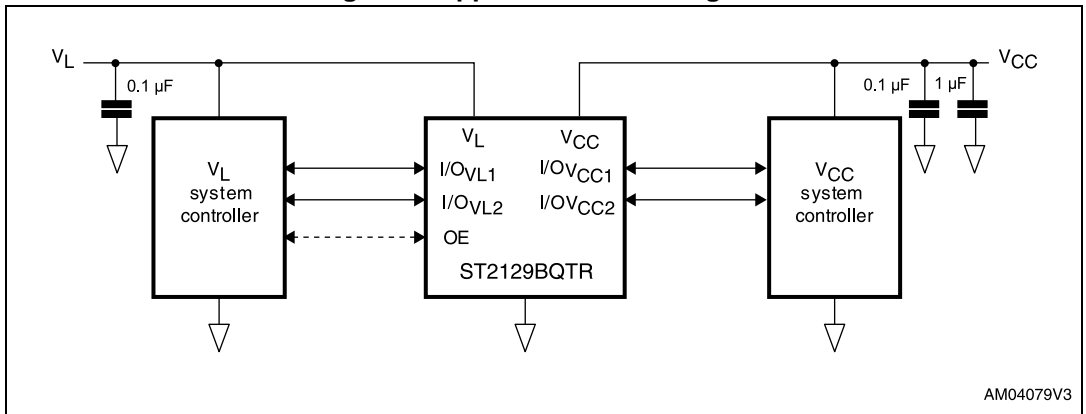
### Device block diagrams

Figure 3. ST2129BQTR block diagram



1. When OE is LOW, all I/Os are in high-impedance mode.
2. ST2129BQTR has 2 channels. For simplicity, the above diagram shows only 1 channel.

Figure 4. Application block diagram



### 3 Supplementary notes

#### 3.1 Driver requirement

For proper operation, the driver from each side of the device must have the capability to source and sink a minimum of 1 mA current. The device architecture requires the driver to source/sink maximum current of  $(V_{CC}/4)$  mA to/from the weak 4 k $\Omega$  output buffer.

#### 3.2 Load driving capability

To support the architecture that allows level translation without direction pin, the one-shot transistor is turned ON only during state transition at the output side. After the one-shot transistor is turned OFF, only the 4 k $\Omega$  resistor maintains the output logic state. So, a resistive load or pull-up resistor less than 50 k $\Omega$  is not recommended for proper operation.

#### 3.3 Truth table

Table 3. Truth table

Enable	Bi-directional input/output	
OE	I/O <sub>VCC</sub>	I/O <sub>VL</sub>
H <sup>(1)</sup>	H <sup>(2)</sup>	H <sup>(1)</sup>
H <sup>(1)</sup>	L	L
L	Z <sup>(3)</sup>	Z <sup>(3)</sup>

1. High level  $V_L$  power supply referred.
2. High level  $V_{CC}$  power supply referred.
3. Z = high impedance.



## 4 Maximum ratings

Stressing the device above the rating listed in [Table 4: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in [Table 5: Recommended operating conditions](#) of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_L$	Supply voltage	-0.3 to 4.6	V
$V_{CC}$	Supply voltage	-0.3 to 6.5	V
$V_{OE}$	DC control input voltage	-0.3 to 6.5	V
$V_{I/OVL}$	DC I/O <sub>VL</sub> input voltage (OE = GND or $V_L$ )	-0.3 to $V_L + 0.3$	V
$V_{I/OVCC}$	DC I/O <sub>VCC</sub> input voltage (OE = GND or $V_L$ )	-0.3 to $V_{CC} + 0.3$	V
$I_{IK}$	DC input diode current	-20	mA
$I_{I/OVL}$	DC output current	±25	mA
$I_{I/OVCC}$	DC output current	±25	mA
$I_{SCTOUT}$	Short-circuit duration, continuous	40	mA
$P_D$	Power dissipation	500	mW
$T_{STG}$	Storage temperature	-65 to 150	°C
$T_L$	Lead temperature (10 seconds)	300	°C
ESD	Electrostatic discharge protection (HBM)	±2	kV

## Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_L$	Supply voltage	1.65	–	3.6	V
$V_{CC}$	Supply voltage	$V_L$	–	5.5	V
$V_{OE}$	Input voltage (OE output enable pin, $V_L$ power supply referred)	0	–	3.6	V
$V_{I/OVL}$	I/O <sub>VL</sub> voltage	0	–	$V_L$	V
$V_{I/OVCC}$	I/O <sub>VCC</sub> voltage	0	–	$V_{CC}$	V
$T_{OP}$	Operating temperature	-40	–	85	°C
dt/dV	Input rise and fall time	0	–	1	ns/V

## 5 Electrical characteristics

### 5.1 DC characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at  $T_A = 25\text{ }^\circ\text{C}$ .

Table 6. DC characteristics

Symbol	Parameter	$V_L$	$V_{CC}$	Test conditions	Value					Unit
					$T_A = 25\text{ }^\circ\text{C}$			$-40\text{ to }85\text{ }^\circ\text{C}$		
					Min.	Typ.	Max.	Min.	Max.	
$V_{IHL}$	High-level input voltage ( $I/O_{VL}$ )	1.65 to 3.6	$V_L$ to 5.5		$0.8 V_L$	–	–	$0.8 V_L$	–	V
$V_{ILL}$	Low-level input voltage ( $I/O_{VL}$ )	1.65 to 3.6	$V_L$ to 5.5		–	–	$0.2 V_L$	–	$0.2 V_L$	V
$V_{IHC}$	High-level input voltage ( $I/O_{VCC}$ )	1.65 to 3.6	$V_L$ to 5.5		$0.8 V_{CC}$	–	–	$0.8 V_{CC}$	–	V
$V_{ILC}$	Low-level input voltage ( $I/O_{VCC}$ )	1.65 to 3.6	$V_L$ to 5.5		–	–	$0.2 V_{CC}$	–	$0.2 V_{CC}$	V
$V_{IH-OE}$	High-level input voltage (OE)	1.65 to 3.6	$V_L$ to 5.5		$0.8 V_L$	–	–	$0.8 V_L$	–	V
$V_{IL-OE}$	Low-level input voltage (OE)	1.65 to 3.6	$V_L$ to 5.5		–	–	$0.2 V_L$	–	$0.2 V_L$	V
$V_{OHL}$	High-level output voltage ( $I/O_{VL}$ )	1.65 to 3.6	$V_L$ to 5.5	$IO = -60\text{ }\mu\text{A}$	$V_L - 0.4$	–	–	$V_L - 0.4$	–	V
$V_{OLL}$	Low-level output voltage ( $I/O_{VL}$ )	1.65 to 3.6	$V_L$ to 5.5	$IO = +60\text{ }\mu\text{A}$	–	–	0.4	–	0.4	V
$V_{OHC}$	High-level output voltage ( $I/O_{VCC}$ )	1.65 to 3.6	$V_L$ to 5.5	$IO = -60\text{ }\mu\text{A}$	$V_{CC} - 0.4$	–	–	$V_{CC} - 0.4$	–	V

Table 6. DC characteristics (continued)

Symbol	Parameter	$V_L$	$V_{CC}$	Test conditions	Value					Unit
					$T_A = 25\text{ }^\circ\text{C}$			$-40\text{ to }85\text{ }^\circ\text{C}$		
					Min.	Typ.	Max.	Min.	Max.	
$V_{OLC}$	Low-level output voltage (I/O <sub>VCC</sub> )	1.65 to 3.6	$V_L$ to 5.5	IO = +60 $\mu\text{A}$	–	–	0.4	–	0.4	V
$I_{OE}$	Control input leakage current (OE)	1.65 to 3.6	$V_L$ to 5.5	$V_I = \text{GND}$ or $V_L$	–	–	0.1	–	1	$\mu\text{A}$
$I_{IO\_LKG}$	High-impedance leakage current (I/O <sub>V<sub>L</sub></sub> , I/O <sub>V<sub>CC</sub></sub> )	1.65 to 3.6	$V_L$ to 5.5	OE = GND I/O <sub>V<sub>L</sub></sub> = high I/O <sub>V<sub>CC</sub></sub> = low	–	–	0.1	–	1	$\mu\text{A}$
				OE = GND I/O <sub>V<sub>L</sub></sub> = low I/O <sub>V<sub>CC</sub></sub> = high	–	–	0.1	–	1	$\mu\text{A}$
$I_{QVCC}$	Quiescent supply current $V_{CC}$	1.65 to 3.6	$V_L$ to 5.5	OE = $V_L$	–	–	3.5	–	4.5	$\mu\text{A}$
$I_{QVL}$	Quiescent supply current $V_L$	1.65 to 3.6	$V_L$ to 5.5	OE = $V_L$	–	–	0.1	–	1	$\mu\text{A}$
$I_{Z-VCC}$	High-impedance quiescent supply current $V_{CC}$	1.65 to 3.6	$V_L$ to 5.5	OE = GND I/O = Hi-Z	–	–	0.1	–	1	$\mu\text{A}$
$I_{Z-VL}$	High-impedance quiescent supply current $V_L$	1.65 to 3.6	$V_L$ to 5.5	OE = GND I/O = Hi-Z	–	–	0.1	–	1	$\mu\text{A}$

## 5.2 AC characteristics

Load  $C_L = 15$  pF; driver  $t_r = t_f \leq 6$  ns over temperature range  $-40$  °C to  $85$  °C.

**Table 7. AC characteristics - test conditions:  $V_L = 1.65 - 1.95$  V**

Symbol	Parameter	$V_{CC} = V_L - 1.95$ V		$V_{CC} = 2.3 - 2.7$ V		$V_{CC} = 3.0 - 3.6$ V		$V_{CC} = 4.5 - 5.5$ V		Unit	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$t_{RVCC}$	Rise time $I/O_{VCC}$	-	5.2	-	3.2	-	2.4	-	1.8	ns	
$t_{FVCC}$	Fall time $I/O_{VCC}$	-	3.2	-	1.5	-	1.3	-	1.2	ns	
$t_{RVL}$	Rise time $I/O_{VL}$	-	3.3	-	3.3	-	3.3	-	3.3	ns	
$t_{FVL}$	Fall time $I/O_{VL}$	-	1.5	-	1.4	-	1.4	-	1.3	ns	
$t_{I/OVL-VCC}$	Propagation delay time										
	$I/O_{VL-LH}$ to $I/O_{VCC-LH}$	$t_{PLH}$	-	7.6	-	5.8	-	5.0	-	4.4	ns
	$I/O_{VL-HL}$ to $I/O_{VCC-HL}$	$t_{PHL}$	-	4.6	-	3.9	-	3.9	-	3.5	ns
$t_{I/OVCC-VL}$	Propagation delay time										
	$I/O_{VCC-LH}$ to $I/O_{VL-LH}$	$t_{PLH}$	-	7.1	-	6.6	-	4.8	-	4.6	ns
	$I/O_{VCC-HL}$ to $I/O_{VL-HL}$	$t_{PHL}$	-	5.3	-	5.1	-	4.3	-	4.1	ns
$t_{PZL}$	Output enable time $t_{PZL}$	-	28	-	28	-	28	-	28	ns	
$t_{PZH}$	Output enable time $t_{PZH}$	-	90	-	90	-	90	-	90	ns	
$t_{PLZ}$	Output disable time $t_{PLZ}$		120	-	120	-	120	-	120	ns	
$t_{PHZ}$	Output disable time $t_{PHZ}$		80	-	60	-	50	-	50	ns	
$D_R$	Data rate <sup>(1)</sup>	56	-	90	-	90	-	90	-	Mbps	

1. Data rate is guaranteed based on the condition that output I/O signal rise/fall time is less than 15% of period of input I/O signal; input I/O signal is at 50% duty cycle and output I/O signal duty cycle deviation is less than  $50\% \pm 10\%$ .

Table 8. AC characteristics - test conditions:  $V_L = 2.3 - 2.7 V$ 

Symbol	Parameter		$V_{CC} = V_L - 2.7 V$		$V_{CC} = 3.0 - 3.6 V$		$V_{CC} = 4.5 - 5.5 V$		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RVCC}$	Rise time $I/O_{VCC}$		-	3.3	-	2.2	-	1.7	ns
$t_{FVCC}$	Fall time $I/O_{VCC}$		-	1.7	-	1.6	-	1.4	ns
$t_{RVL}$	Rise time $I/O_{VL}$		-	2.2	-	2.2	-	1.9	ns
$t_{FVL}$	Fall time $I/O_{VL}$		-	1.3	-	1.2	-	1.2	ns
$t_{I/OVL-VCC}$	Propagation delay time								
	$I/O_{VL-LH}$ to $I/O_{VCC-LH}$	$t_{PLH}$	-	4.8	-	4.3	-	3.9	ns
	$I/O_{VL-HL}$ to $I/O_{VCC-HL}$	$t_{PHL}$	-	3.7	-	3.3	-	2.9	ns
$t_{I/OVCC-VL}$	Propagation delay time								
	$I/O_{VCC-LH}$ to $I/O_{VL-LH}$	$t_{PLH}$	-	3.9	-	3.5	-	3.5	ns
	$I/O_{VCC-HL}$ to $I/O_{VL-HL}$	$t_{PHL}$	-	3.6	-	3.5	-	3.4	ns
$t_{PZL}$	Output enable time $t_{PZL}$		-	25	-	25	-	25	ns
$t_{PZH}$	Output enable time $t_{PZH}$		-	100	-	100	-	70	ns
$t_{PLZ}$	Output disable time $t_{PLZ}$		-	90	-	90	-	90	ns
$t_{PHZ}$	Output disable time $t_{PHZ}$		-	50	-	50	-	50	ns
$D_R$	Data rate <sup>(1)</sup>		90	-	136	-	158	-	Mbps

1. Data rate is guaranteed based on the condition that output I/O signal rise/fall time is less than 15% of period of input I/O signal; input I/O signal is at 50% duty cycle and output I/O signal duty cycle deviation is less than  $50\% \pm 10\%$ .

Table 9. AC characteristics - test conditions:  $V_L = 3.0 - 3.6 V$

Symbol	Parameter		$V_{CC} = V_L - 3.6 V$		$V_{CC} = 4.5 - 5.5 V$		Unit	
			Min.	Max.	Min.	Max.		
$t_{RVCC}$	Rise time $I/O_{VCC}$		-	2.1	-	1.7	ns	
$t_{FVCC}$	Fall time $I/O_{VCC}$		-	1.3	-	1.3	ns	
$t_{RVL}$	Rise time $I/O_{VL}$		-	1.6	-	1.5	ns	
$t_{FVL}$	Fall time $I/O_{VL}$		-	1.1	-	1.1	ns	
$t_{I/O_{VL-VCC}}$	Propagation delay time							
	$I/O_{VL-LH}$ to $I/O_{VCC-LH}$		$t_{PLH}$	-	4.1	-	4.1	ns
	$I/O_{VL-HL}$ to $I/O_{VCC-HL}$		$t_{PHL}$	-	2.9	-	2.6	ns
$t_{I/O_{VCC-VL}}$	Propagation delay time							
	$I/O_{VCC-LH}$ to $I/O_{VL-LH}$		$t_{PLH}$	-	4.0	-	4.0	ns
	$I/O_{VCC-HL}$ to $I/O_{VL-HL}$		$t_{PHL}$	-	2.6	-	2.5	ns
$t_{PZL}$	Output enable time $t_{PZL}$		-	15	-	15	ns	
$t_{PZH}$	Output enable time $t_{PZH}$		-	70	-	15	ns	
$t_{PLZ}$	Output disable time $t_{PLZ}$		-	70	-	70	ns	
$t_{PHZ}$	Output disable time $t_{PHZ}$		-	50	-	50	ns	
$D_R$	Data rate <sup>(1)</sup>		144	-	186	-	Mbps	

1. Data rate is guaranteed based on the condition that output I/O signal rise/fall time is less than 15% of period of input I/O signal; input I/O signal is at 50% duty cycle and output I/O signal duty cycle deviation is less than 50% ± 10%.

## 6 Test circuit

Figure 5. Test circuit

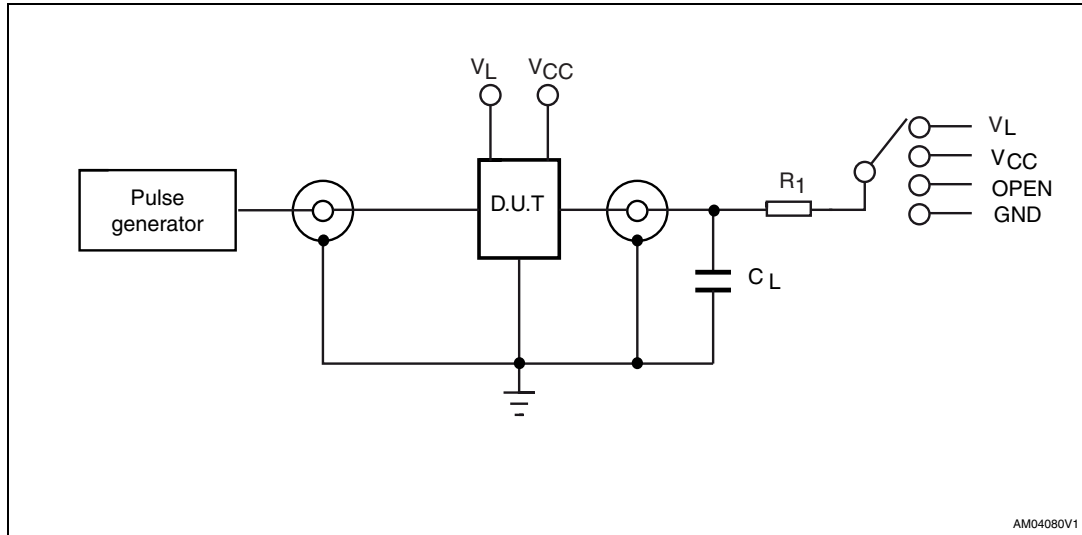


Table 10. Test circuit switches

Test	$C_L$	$R_1$	Switch
$t_{PLH}, t_{PHL}$	15 pF	20 k $\Omega$	Open
$t_r, t_f$	15 pF	20 k $\Omega$	Open
$t_{PZL}, t_{PLZ}$	15 pF	20 k $\Omega$	$V_L$ or $V_{CC}$
$t_{PZH}, t_{PHZ}$	15 pF	20 k $\Omega$	GND

Table 11. Waveform symbol value

Symbol	Driving I/O $_{V_L}$		Driving I/O $_{V_{CC}}$	
	$1.65\text{ V} \leq V_L \leq V_{CC} \leq 2.5\text{ V}$	$3.3\text{ V} \leq V_L \leq V_{CC} \leq 5.5\text{ V}$	$1.65\text{ V} \leq V_L \leq V_{CC} \leq 2.5\text{ V}$	$3.3\text{ V} \leq V_L \leq V_{CC} \leq 5.5\text{ V}$
$V_{IH}$	$V_L$	$V_L$	$V_{CC}$	$V_{CC}$
$V_{IM}$	50% $V_L$	50% $V_L$	50% $V_{CC}$	50% $V_{CC}$
$V_{OM}$	50% $V_{CC}$	50% $V_{CC}$	50% $V_L$	50% $V_L$

Figure 6. Waveform - propagation delay (f = 1 MHz, 50% duty cycle)

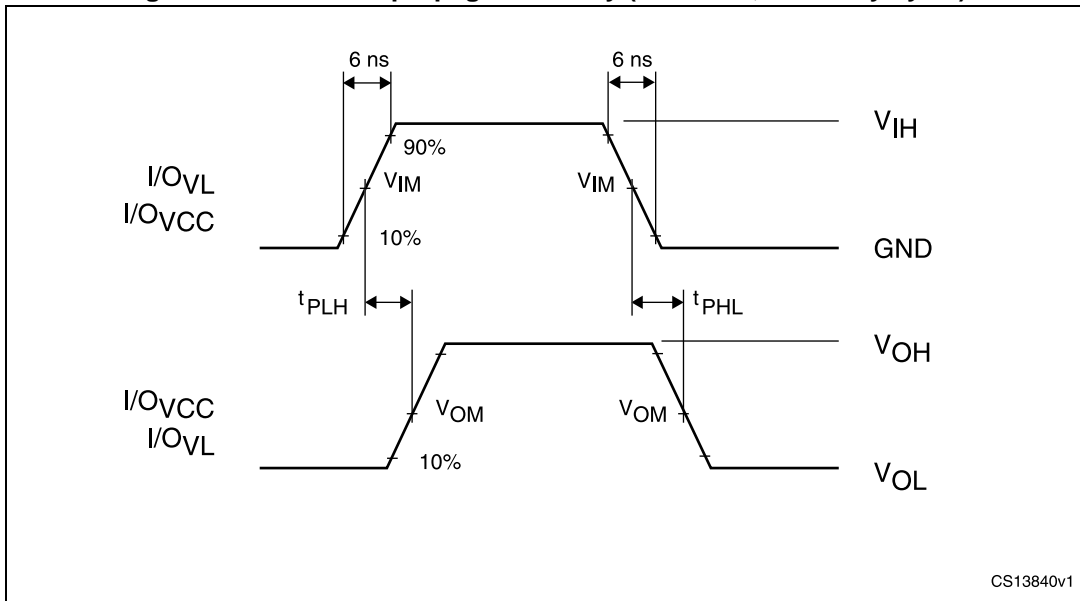
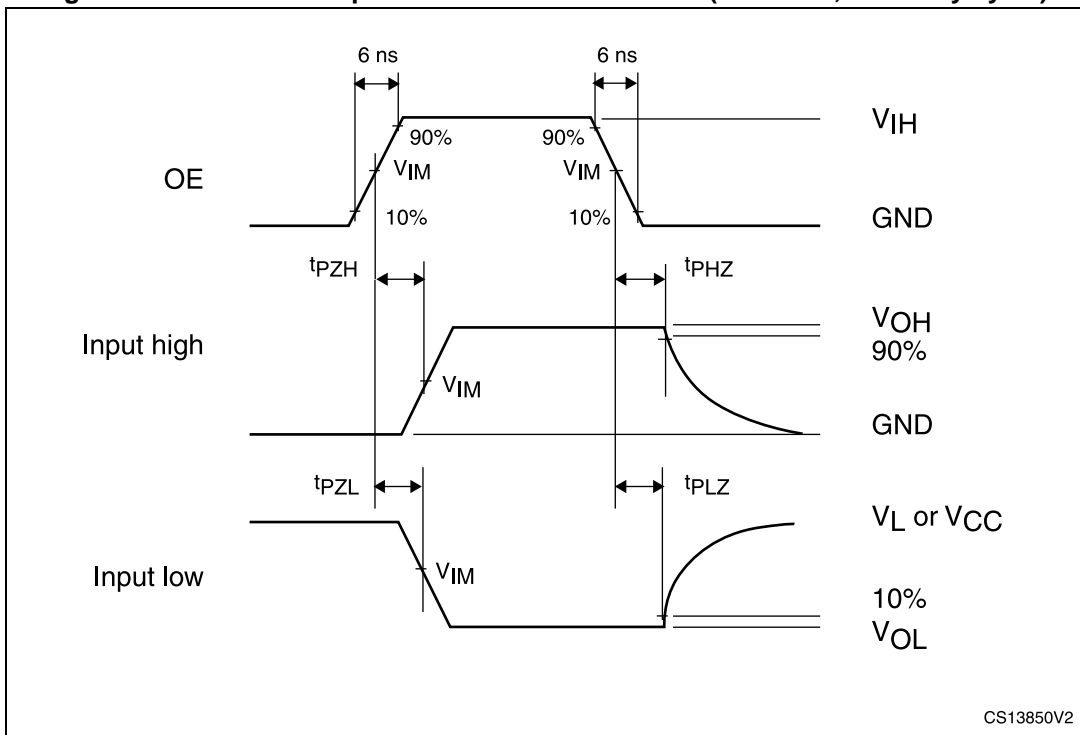


Figure 7. Waveform - output enable and disable time (f = 1 MHz, 50% duty cycle)

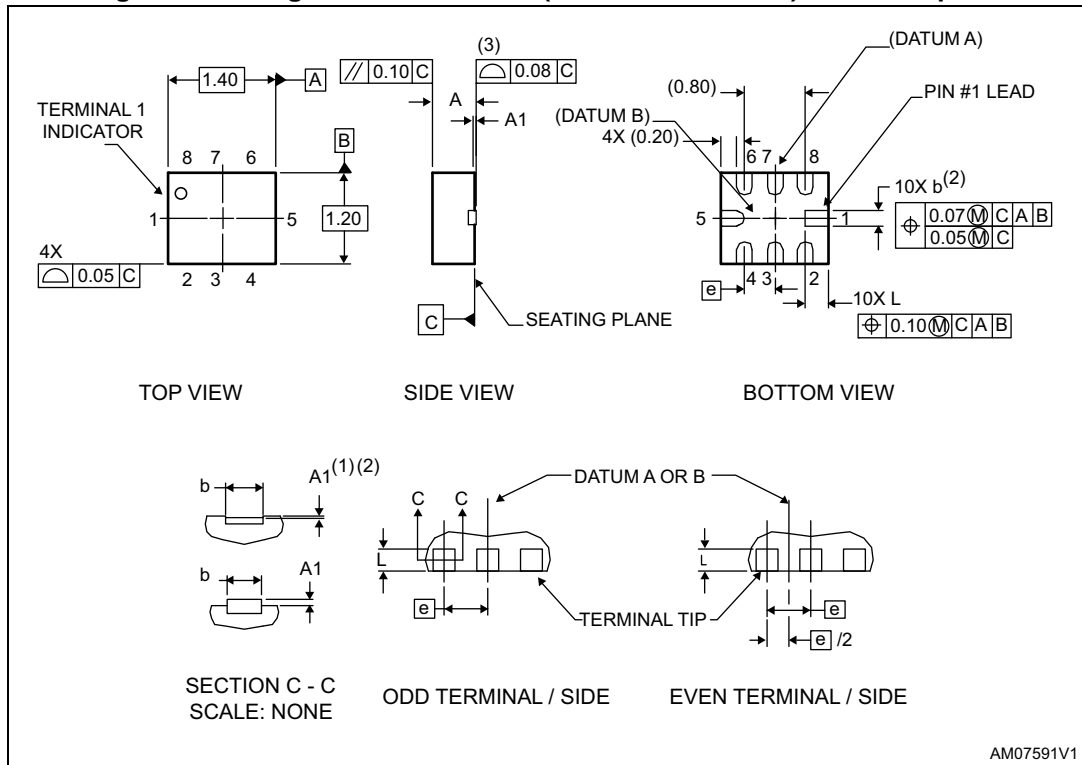




## 7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Figure 8. Package outline for QFN8 (1.4 x 1.2 x 0.55 mm) - 0.40 mm pitch



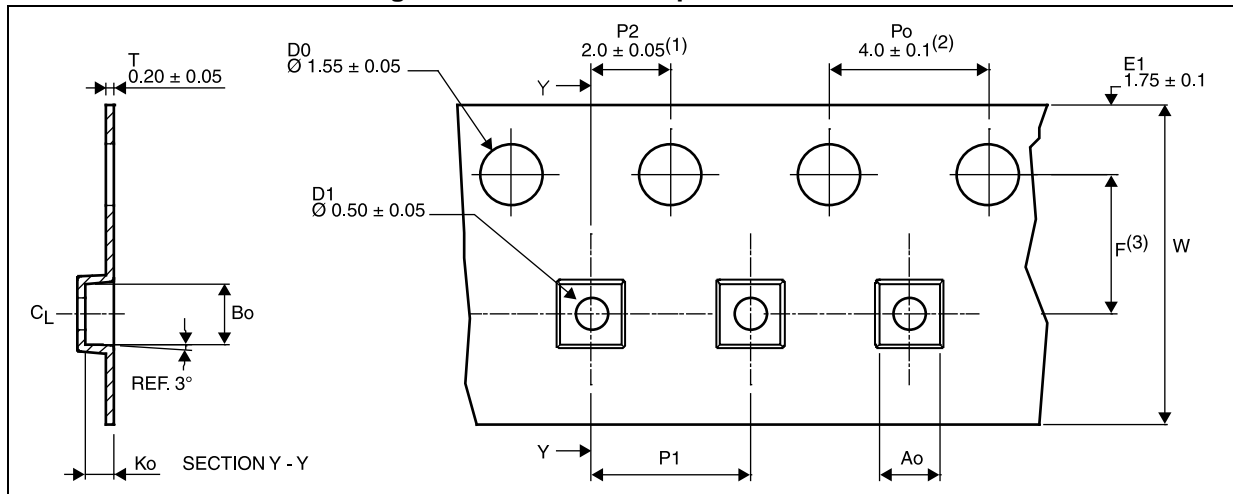
1. Dimension b applies to metallized terminal and is measured between 0.10 and 0.20 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal. Dimension b should not be measured in that radius area.
2. Applied only for terminals.
3. Bilateral coplanarity zone applies to the exposed heatsink slug as well as the terminals.
4. Dimensions and tolerancing conform to ASME Y14.5M - 1994.

Table 12. Mechanical data for QFN8 (1.4 x 1.2 x 0.55 mm) - 0.40 mm pitch

Symbol	Dimensions (mm)			Note
	Min.	Nom.	Max.	
A	0.50	0.55	0.60	
A1	0.00	-	0.05	
b	0.15	0.20	0.25	(1)
B	0	-	12°	(2)
e	0.40 BSC			
N	8			(3)
L	0.25	0.30	0.35	

1. Dimension b applies to the metallized terminal and is measured between 0.10 and 0.20 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal. Dimension b should not be measured in that radius area.
2. All dimensions are in millimeters, B is in degrees.
3. N is the total number of terminals.

Figure 9. QFN8 carrier tape - 8 mm width

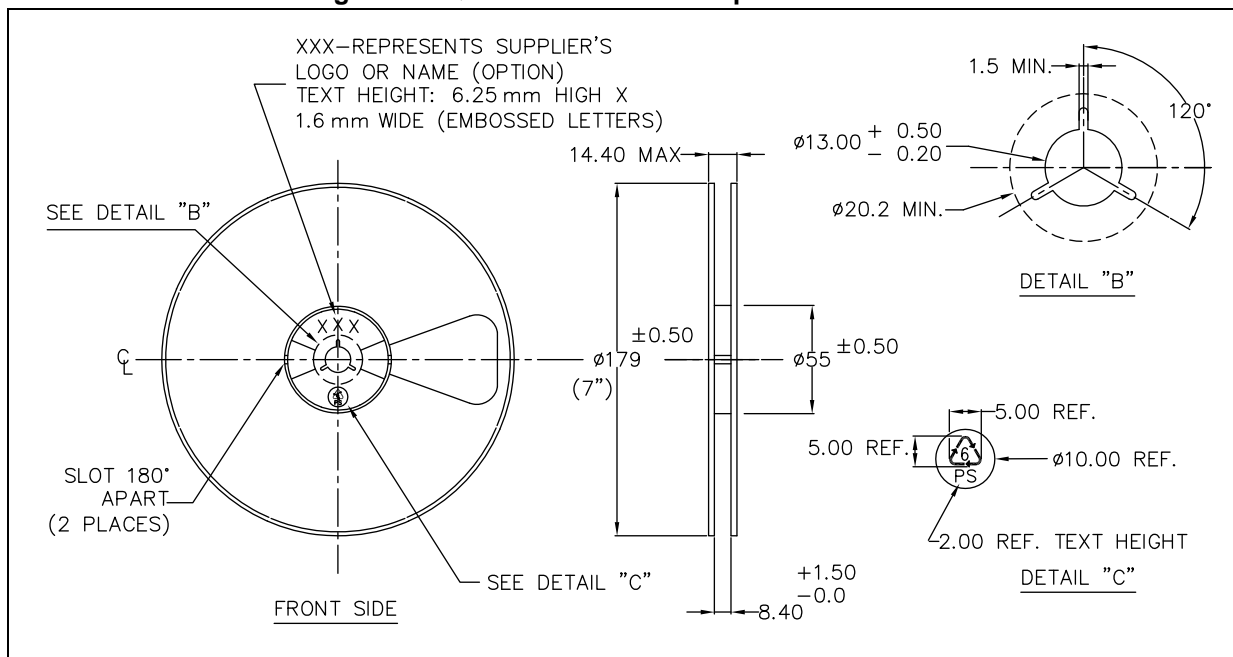


1. Measured from centerline of sprocket hole to centerline of pocket.
2. Cumulative tolerance of 10 sprocket holes is  $\pm 0.20$ .
3. Measured from centerline of sprocket hole to centerline of pocket.
4. Other material available.
5. Typical SR of form tape max.  $10^\circ \Omega/SR$ .
6. All dimensions are in millimeters unless otherwise stated.

Table 13. QFN8 carrier tape dimensions - 8 mm width

Carrier tape						
Symbol	Ao	Bo	Ko	F	P1	W
Dimensions	1.52 ± 0.05	1.52 ± 0.05	0.73 ± 0.05	3.50 ± 0.05	4.00 ± 0.10	8.00 ± 0.10

Figure 10. QFN8 reel for carrier tape - 8 mm width



## 8 Revision history

**Table 14. Document revision history**

Date	Revision	Changes
14-Jun-2012	1	Initial release.
18-Feb-2013	2	Updated document status (production data). Updated <i>Description</i> (corrected RPNs), <i>Description</i> moved to page 1. Added carrier tape ( <i>Figure 9</i> and <i>Table 13</i> ). Minor corrections throughout document.

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