



**CY7C470**  
**CY7C472**  
**CY7C474**

## 8K x 9 FIFO, 16K x 9 FIFO, 32K x 9 FIFO with Programmable Flags

### Features

- 8K x 9, 16K x 9, and 32K x 9 FIFO buffer memory
- Asynchronous read/write
- High-speed 33.3-MHz read/write independent of depth/width
- Low operating power  
—  $I_{CC}$  (max.) = 70 mA
- Programmable Almost Full/Empty flag
- Empty, Almost Empty, Half Full, Almost Full, and Full status flags
- Programmable retransmit
- Expandable in width
- 5V  $\pm$  10% supply
- TTL compatible
- Three-state outputs
- Proprietary 0.8-micron CMOS technology

### Functional Description

The CYC47X FIFO series consists of high-speed, low-power, first-in first-out (FIFO) memories with programmable flags and retransmit mark. The CY7C470, CY7C472, and CY7C474 are 8K, 16K, and 32K words by 9 bits wide, respectively. They are offered in 600-mil DIP, PLCC, and LCC packages. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Three status pins—Empty/Full (E/F), Programmable Almost Full/Empty (PAFE), and Half Full (HF)—are provided to the user. These pins are decoded to determine one of six states: Empty, Almost Empty, Less than Half Full, Greater than Half Full, Almost Full, and Full.

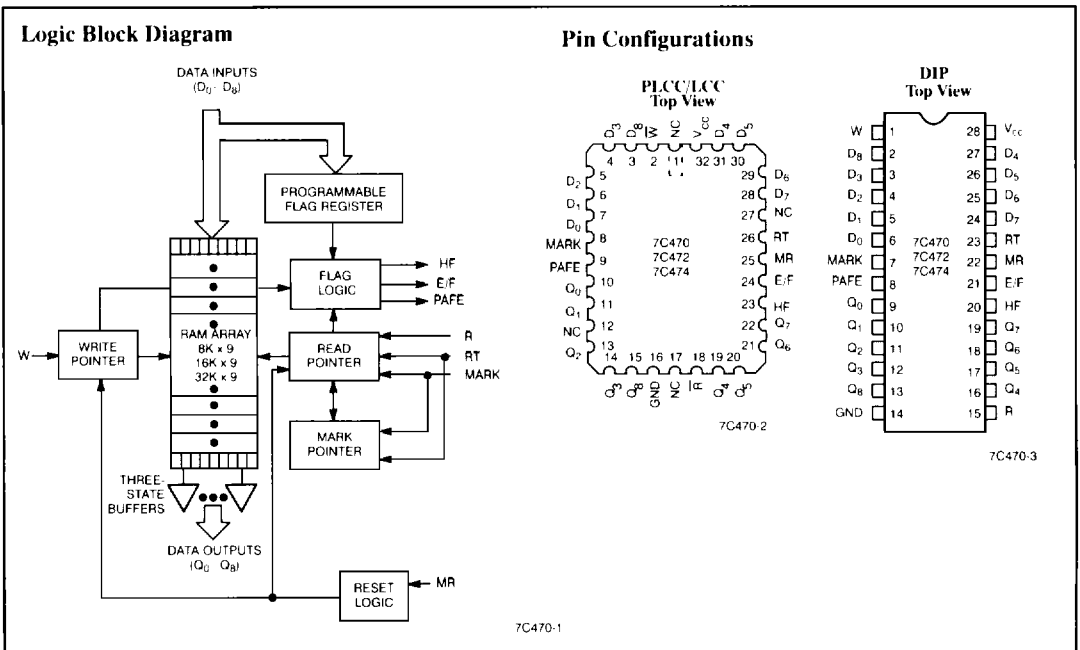
The read and write operations may be asynchronous; each can occur at a rate of 33.3 MHz. The write operation occurs

when the write ( $\bar{W}$ ) signal goes LOW. Read occurs when read ( $\bar{R}$ ) goes LOW. The nine data outputs go into a high-impedance state when  $\bar{R}$  is HIGH.

The user can store the value of the read pointer for retransmit by using the MARK pin. A LOW on the retransmit ( $\bar{RT}$ ) input causes the FIFO to resend data by resetting the read pointer to the value stored in the mark pointer.

In the standalone and width expansion configurations, a LOW on the retransmit ( $\bar{RT}$ ) input causes the FIFO to resend the data. With the mark feature, retransmit can start from any word in the FIFO.

The CYC47X series is fabricated using a proprietary 0.8-micron N-well CMOS technology. Input ESD protection is greater than 2001V and latch-up is prevented by the use of reliable layout techniques, guard rings, and a substrate bias generator.





**Selection Guide**

		7C470-15 7C472-15 7C474-15	7C470-20 7C472-20 7C474-20	7C470-25 7C472-25 7C474-25	7C470-40 7C472-40 7C474-40
Frequency (MHz)		33.3	33.3	28.5	20
Maximum Access Time (ns)		15	20	25	40
Maximum Operating Current (mA)	Commercial	105		90	70
	Military/Industrial		110	95	75

**Maximum Ratings**

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with  
 Power Applied ..... -55°C to +125°C  
 Supply Voltage to Ground Potential ..... -0.5V to +7.0V  
 DC Voltage Applied to Outputs  
 in High Z State ..... -0.5V to +7.0V  
 DC Input Voltage ..... -3.0V to +7.0V  
 Power Dissipation ..... 1.0W  
 Output Current, into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V  
 (per MIL-STD-883, Method 3015)  
 Latch-Up Current ..... >200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%
Military <sup>[1]</sup>	-55°C to +125°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range<sup>[2]</sup>

Parameter	Description	Test Conditions	7C470-15 7C472-15 7C474-15		7C470-20 7C472-20 7C474-20		7C470-25 7C472-25 7C474-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA	2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		Com'l	2.2			2.2		V
			Mil/Ind			2.2		2.2	
V <sub>IL</sub>	Input LOW Voltage			0.8		0.8		0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10	+10	-10	+10	-10	+10	µA
I <sub>OZ</sub>	Output Leakage Current	R̄ ≥ V <sub>IH</sub> , GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub>	-10	+10	-10	+10	-10	+10	µA
I <sub>CC</sub>	Operating Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA	Com'l		105			90	mA
			Mil/Ind				110		95
I <sub>SB1</sub>	Standby Current	All Inputs = V <sub>IH</sub> Min.	Com'l		25			25	mA
			Mil/Ind				30		30
I <sub>SB2</sub>	Power-Down Current	All Inputs = V <sub>CC</sub> - 0.2V	Com'l		20			20	mA
			Mil/Ind				25		25
I <sub>OS</sub> <sup>[3]</sup>	Output Short Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-90		-90		-90	mA

**Notes:**

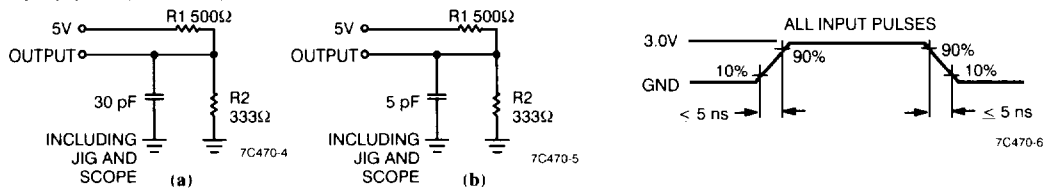
1. T<sub>A</sub> is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.

**Electrical Characteristics** Over the Operating Range<sup>[2]</sup> (continued)

Parameter	Description	Test Conditions	7C470-40 7C472-40 7C474-40		Unit
			Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		Com'l	2.2	V
			Mil/Ind	2.2	
V <sub>IL</sub>	Input LOW Voltage			0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10	+10	μA
I <sub>OZ</sub>	Output Leakage Current	R̄ ≥ V <sub>IH</sub> , GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub>	-10	+10	μA
I <sub>CC</sub>	Operating Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA	Com'l	70	mA
			Mil/Ind	75	
I <sub>SB1</sub>	Standby Current	All Inputs = V <sub>IH</sub> Min.	Com'l	25	mA
			Mil/Ind	30	
I <sub>SB2</sub>	Power-Down Current	All Inputs = V <sub>CC</sub> - 0.2V	Com'l	20	mA
			Mil/Ind	25	
I <sub>OS</sub> <sup>[3]</sup>	Output Short Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-90	mA

**Capacitance**<sup>[4]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 4.5V	10	pF
C <sub>OUT</sub>	Output Capacitance		12	pF

**AC Test Loads and Waveforms**


Equivalent to: THÉVENIN EQUIVALENT  
 200Ω  
 OUTPUT ——— 2V

**Note:**

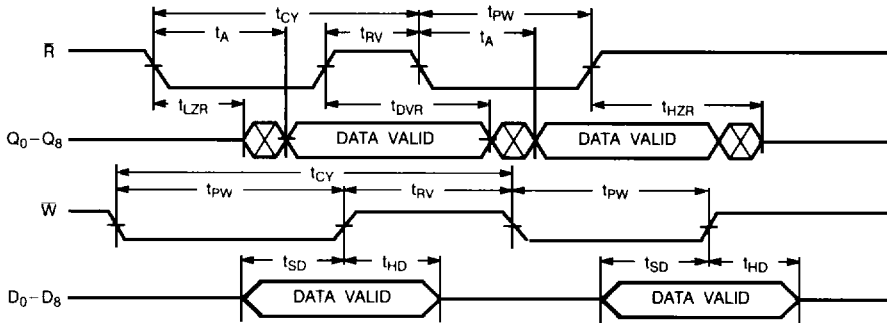
4. Tested initially and after any design or process changes that may affect these parameters.

**Switching Characteristics** Over the Operating Range<sup>[5, 6]</sup>

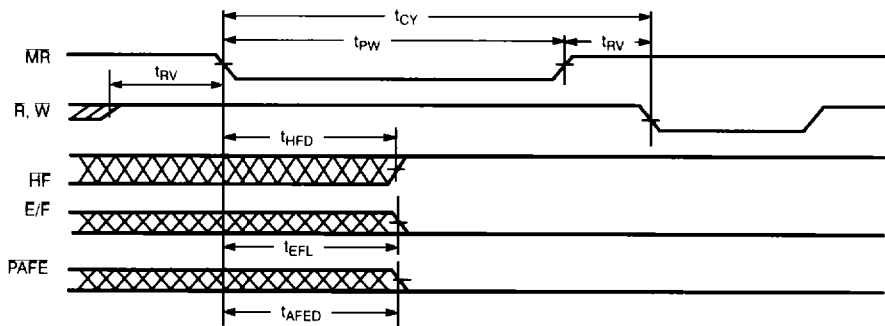
Parameter	Description	7C470-15 7C472-15 7C474-15		7C470-20 7C472-20 7C474-20		7C470-25 7C472-25 7C474-25		7C470-40 7C472-40 7C474-40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>CY</sub>	Cycle Time	30		30		35		50		ns
t <sub>A</sub>	Access Time		15		20		25		40	ns
t <sub>RV</sub>	Recovery Time	15		10		10		10		ns
t <sub>PW</sub>	Pulse Width	15		20		25		40		ns
t <sub>LZR</sub>	Read LOW to Low Z	3		3		3		3		ns
t <sub>DV</sub> <sup>[7]</sup>	Valid Data from Read HIGH	3		3		3		3		ns
t <sub>HZ</sub> <sup>[7]</sup>	Read HIGH to High Z		15		15		18		25	ns
t <sub>HWZ</sub>	Write HIGH to Low Z	5		5		5		5		ns
t <sub>SD</sub>	Data Set-Up Time	11		12		15		20		ns
t <sub>HD</sub>	Data Hold Time	0		0		0		0		ns
t <sub>EFD</sub>	$\bar{E}/\bar{F}$ Delay		15		20		25		40	ns
t <sub>EFL</sub>	$\bar{M}\bar{R}$ to $\bar{E}/\bar{F}$ LOW		25		30		35		50	ns
t <sub>HFD</sub>	$\bar{H}\bar{F}$ Delay		25		30		35		50	ns
t <sub>AFED</sub>	$\bar{P}\bar{A}\bar{F}\bar{E}$ Delay		25		30		35		50	ns
t <sub>RAE</sub>	Effective Read from Write HIGH	15		20		25		40		ns
t <sub>WAF</sub>	Effective Write from Read HIGH	15		20		25		40		ns

**Notes:**

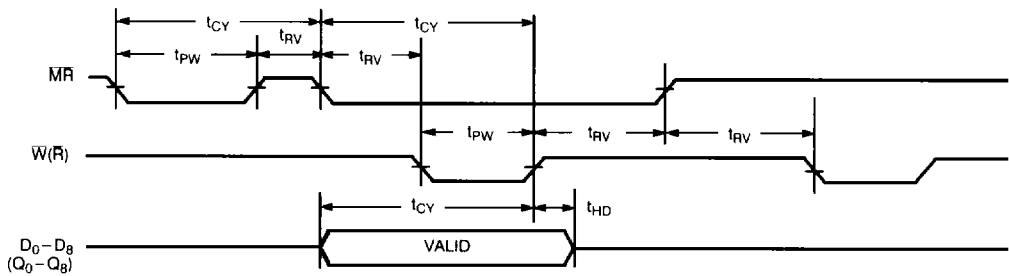
- Test conditions assume signal transmission time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I<sub>OL</sub>/I<sub>OIH</sub> and 30-pF load capacitance, as in part (a) of AC Test Load and Waveforms, unless otherwise specified.
- See the last page of this specification for Group A subgroup testing information.
- t<sub>HZR</sub> and t<sub>PVR</sub> use capacitance loading as in part (b) of AC Test Loads. t<sub>HZR</sub> transition is measured at +500 mV from V<sub>OL</sub> and -500 mV from V<sub>OIH</sub>. t<sub>PVR</sub> transition is measured at the 1.5V level. t<sub>HWZ</sub> and t<sub>LZR</sub> transition is measured at ±100 mV from the steady state.

**Switching Waveforms**  
**Asynchronous Read and Write**


7C470-7

**Master Reset (No Write to Programmable Flag Register)**


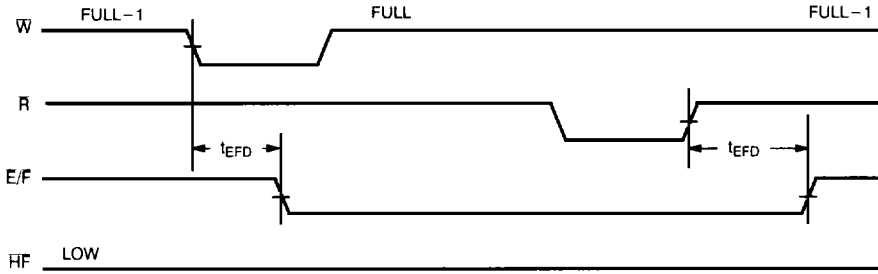
7C470-8

**Master Reset (Write to Programmable Flag Register)<sup>{8, 9}</sup>**


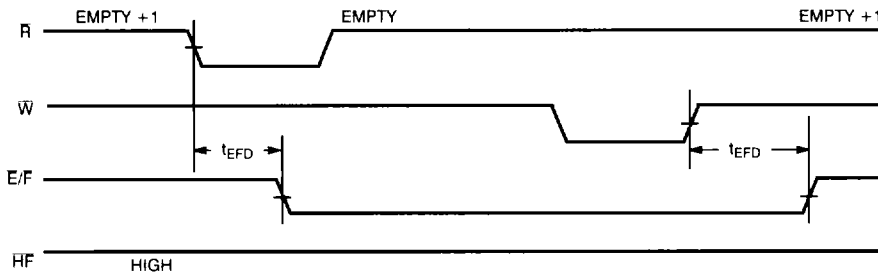
7C470-9

**Note:**

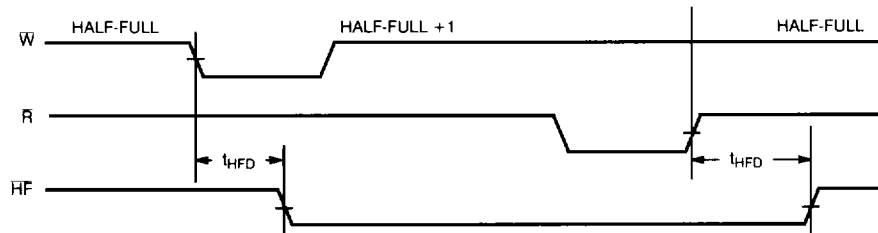
8. Waveform labels in parentheses pertain to writing the programmable flag register from the output port ( $Q_0 - Q_8$ ).
9. Master Reset (MR) must be pulsed LOW once prior to programming.

**Switching Waveforms (continued)**
**E/F Flag (Last Write to First Read Full Flag)**


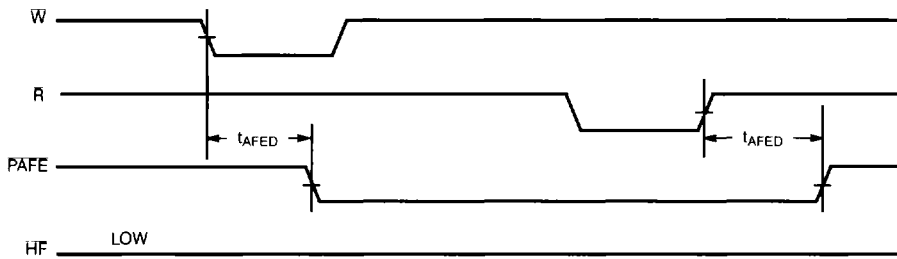
7C470-10

**E/F Flag (Last Read to First Write Empty Flag)**


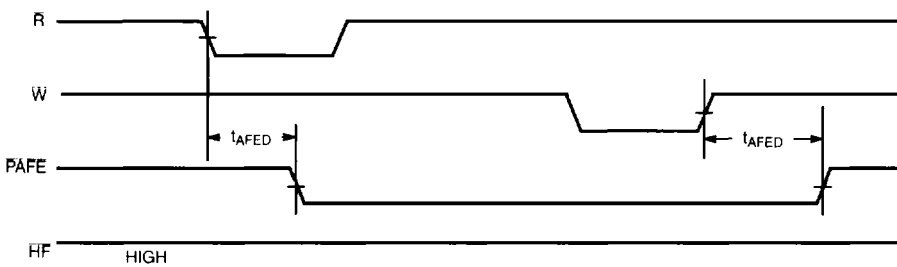
7C470-11

**Half Full Flag**


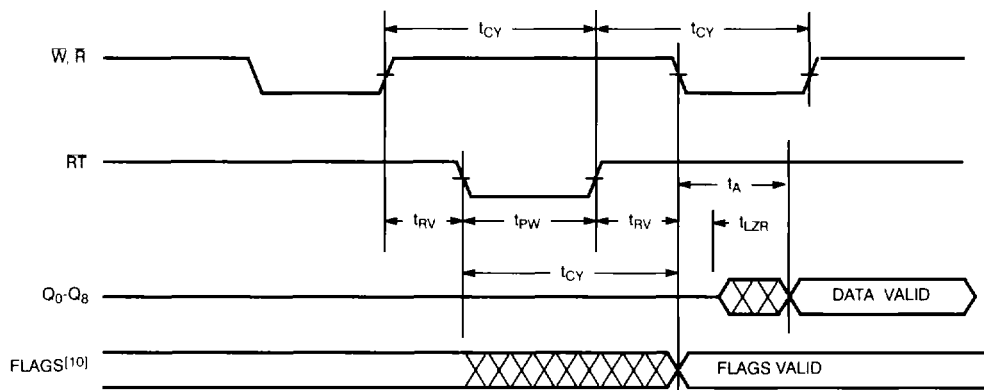
7C470-12

**Switching Waveforms (continued)**
**PAFE Flag (Almost Full)**


7C470-13

**PAFE Flag (Almost Empty)**


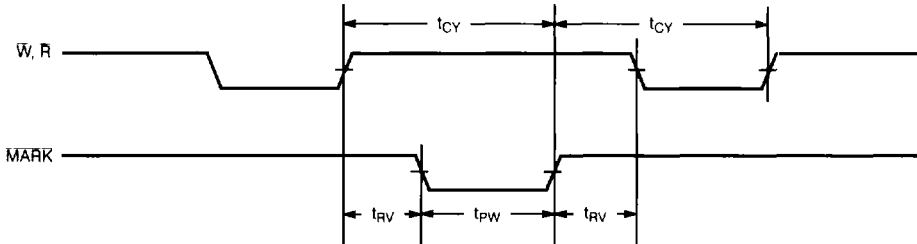
7C470-14

**Retransmit<sup>(10)</sup>**


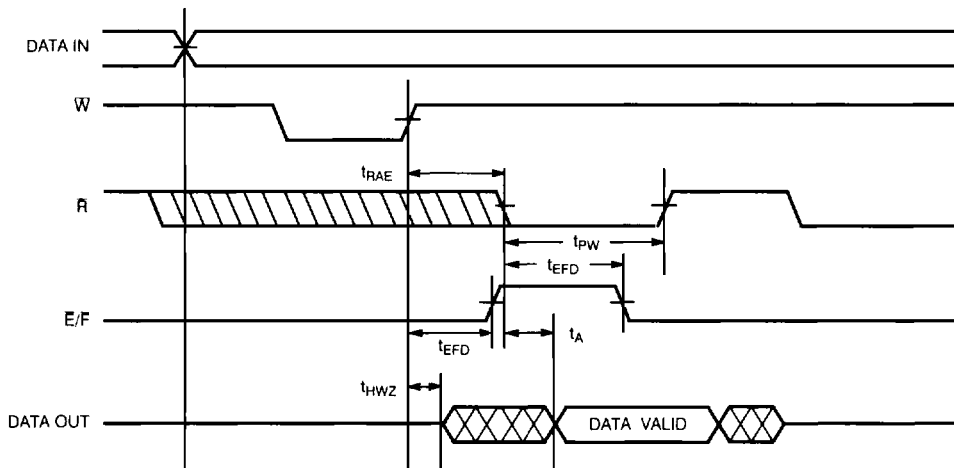
7C470-15

**Notes:**

10. The flags may change state during retransmit, but they will be valid a  $t_{CY}$  later, except for the CY7C47X-20 (Military), whose flags will be valid after  $t_{CY} + 10$  ns.

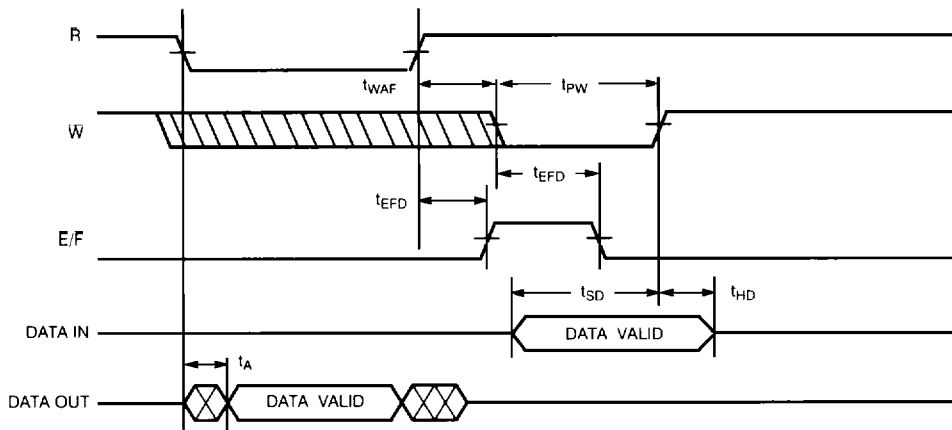
**Switching Waveforms (continued)**
**Mark**


7C470-16

**Empty Flag and Read Data Flow-Through Mode**


7C470-17



**Switching Waveforms (continued)**
**Full Flag and Write Data Flow-Through Mode**


7C470-18

**Architecture**

The CY7C470, CY7C472, and CY7C474 FIFOs consist of an array of 8,192, 16,384, and 32,768 words of 9 bits each, respectively. The control consists of a read pointer, a write pointer, a retransmit pointer, control signals (i.e., write, read, mark, retransmit, and master reset), and flags (i.e., Empty/Full, Half Full, and Programmable Almost Full/Empty).

**Resetting the FIFO**

Upon power-up, the FIFO must be reset with a Master Reset ( $\overline{MR}$ ) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag (E/F) and Almost Full/Empty flag (PAFE) being LOW, and Half Full flag (HF) being HIGH. The read pointer, write pointer, and retransmit pointer are reset to zero. For a valid reset, Read ( $\overline{R}$ ) and Write ( $\overline{W}$ ) must be HIGH  $t_{RPW}/t_{WPW}$  before the falling edge and  $t_{RMR}$  after the rising edge of  $\overline{MR}$ .

**Writing Data to the FIFO**

Data can be written to the FIFO when it is not FULL<sup>[11]</sup>. A falling edge of  $\overline{W}$  initiates a write cycle. Data appearing at the inputs ( $D_0-D_8$ )  $t_{SD}$  before and  $t_{HD}$  after the rising edge of  $\overline{W}$  will be stored sequentially in the FIFO.

**Reading Data from the FIFO**

Data can be read from the FIFO when it is not empty<sup>[12]</sup>. A falling edge of  $\overline{R}$  initiates a read cycle. Data outputs ( $Q_0-Q_8$ ) are in a high-impedance condition when the FIFO is empty and between read operations ( $\overline{R}$  HIGH). The falling edge of  $\overline{R}$  during the last read cycle before the empty condition triggers a high-to-low transition of E/F, prohibiting any further read operations until  $t_{RFF}$  after a valid write.

**Retransmit**

The Retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and resent if necessary. Retransmission can start from anywhere in the FIFO and be repeated without limitation.

The retransmit methodology is as follows: mark the current value of the read pointer, after an error in subsequent read operations return to that location and resume reading. This effectively re-sends all of the data from the mark point. When  $\overline{MARK}$  is LOW, the current value of the read pointer is stored. This operation marks the beginning of the packet to be resent. When  $\overline{RT}$  is LOW, the read pointer is updated with the mark location. During each subsequent read cycle, data is read and the read pointer incremented.

Care must be taken when using the retransmit feature. Use the mark function such that the write pointer does not pass the mark pointer, because further write operations will overwrite data.

**Programmable Almost Full/Empty Flag**

The CY7C470/2/4 offer a variable offset for the Almost Empty and the Almost Full condition. The offset is loaded into the programmable flag register (PFR) during a master reset cycle. While  $\overline{MR}$  is LOW, the PFR can be loaded from  $Q_8-Q_0$  by pulsing  $\overline{R}$  LOW or from  $D_8-D_0$  by pulsing  $\overline{W}$  LOW. The offset options are listed in Table 2. See Table 1 for a description of the six FIFO states. If the PFR is not loaded during master reset ( $\overline{R}$  and  $\overline{W}$  HIGH) the default offset will be 256 words from Full and Empty.

**Notes:**

11. When the FIFO is less than half full, the flags make a LOW-to-HIGH transition on the rising edge of  $\overline{W}$  and make the HIGH-to-LOW transition on the falling edge of  $\overline{R}$ . If the FIFO is more than half full, the flags make the LOW-to-HIGH transition on the rising edge of  $\overline{R}$  and HIGH-to-LOW transition on the falling edge of  $\overline{W}$ .

12. Full and empty states can be decoded from the Half-Full (HF) and Empty/Full (E/F) flags.

**Table 1. Flag Truth Table<sup>[13]</sup>**

$\overline{HF}$	$\overline{E/F}$	$\overline{PAFE}$	State	CY77C470 (8K x 9) Number of Words in FIFO	CY77C472 (16K x 9) Number of Words in FIFO	CY77C474 (32K x 9) Number of Words in FIFO
1	0	0	Empty	0	0	0
1	1	0	Almost Empty	$1 \blacklozenge (P - 1)$	$1 \blacklozenge (P - 1)$	$1 \blacklozenge (P - 1)$
1	1	1	Less than Half Full	$P \blacklozenge 4096$	$P \blacklozenge 8192$	$P \blacklozenge 16384$
0	1	1	Greater than Half Full	$4097 \blacklozenge (8192 - P)$	$8193 \blacklozenge (16384 - P)$	$16385 \blacklozenge (32768 - P)$
0	1	0	Almost Full	$(8192 - P + 1) \blacklozenge 8191$	$(16384 - P + 1) \blacklozenge 16383$	$(32768 - P + 1) \blacklozenge 32767$
0	0	0	Full	8192	16384	32768

**Table 2. Programmable Almost Full/Empty Options<sup>[14]</sup>**

D3	D2	D1	D0	PAFE Active when:	P
0	0	0	0	256 or less locations from Empty/Full (default)	256
0	0	0	1	16 or less locations from Empty/Full	16
0	0	1	0	32 or less locations from Empty/Full	32
0	0	1	1	64 or less locations from Empty/Full	64
0	1	0	0	128 or less locations from Empty/Full	128
0	1	0	1	256 or less locations from Empty/Full (default)	256
0	1	1	0	512 or less locations from Empty/Full	512
0	1	1	1	1024 or less locations from Empty/Full	1024
1	0	0	0	2048 or less locations from Empty/Full	2048
1	0	0	1	4098 or less locations from Empty/Full <sup>[15]</sup>	4098
1	0	1	0	8192 or less locations from Empty/Full <sup>[16]</sup>	8192

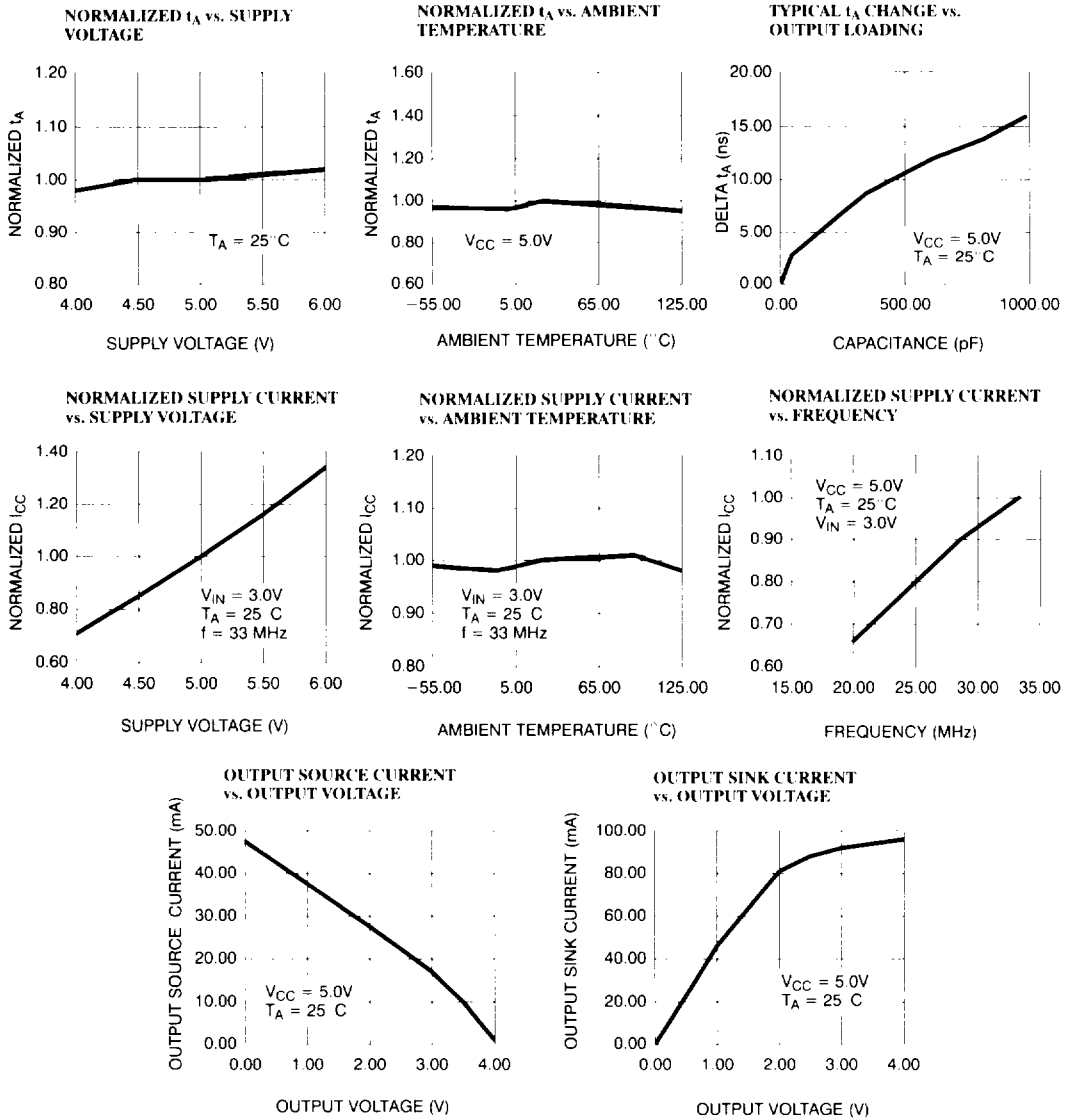
**Notes:**

 13. See *Table 2* for P values.

14. Almost flags default to 256 locations from Empty/Full.

15. Only for CY7C472 and CY7C474.

16. Only for CY7C470.

**Typical AC and DC Characteristics**


**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C470-15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C470-15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C470-15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C470-20DMB	D43	28-Lead (600-Mil) Sidebrazed CerDIP	Military
	CY7C470-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C470-25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C470-25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C470-25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C470-25DMB	D43	28-Lead (600-Mil) Sidebrazed CerDIP	Military
	CY7C470-25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C470-40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C470-40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C470-40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C470-40DMB	D43	28-Lead (600-Mil) Sidebrazed CerDIP	Military
	CY7C470-40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C472-15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C472-15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C472-15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C472-20DMB	D43	28-Lead (600-Mil) Sidebrazed CerDIP	Military
	CY7C472-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C472-25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C472-25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C472-25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C472-25DMB	D43	28-Lead (600-Mil) Sidebrazed CerDIP	Military
	CY7C472-25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C472-40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C472-40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C472-40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C472-40DMB	D43	28-Lead (600-Mil) Sidebrazed CerDIP	Military
	CY7C472-40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	



**Ordering Information** (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C474-15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C474-15PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C474-15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
20	CY7C474-20DMB	D43	28-Lead (600-Mil) Sidebrazed CerDIP	Military
	CY7C474-20LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
25	CY7C474-25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C474-25PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C474-25JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C474-25DMB	D43	28-Lead (600-Mil) Sidebrazed CerDIP	Military
	CY7C474-25LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C474-40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C474-40PC	P15	28-Lead (600-Mil) Molded DIP	
	CY7C474-40JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
	CY7C474-40DMB	D43	28-Lead (600-Mil) Sidebrazed CerDIP	Military
	CY7C474-40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

**MILITARY SPECIFICATIONS**  
**Group A Subgroup Testing**

**DC Characteristics**

Parameter	Subgroups
V <sub>OH</sub>	1, 2, 3
V <sub>OL</sub>	1, 2, 3
V <sub>IH</sub>	1, 2, 3
V <sub>IL Max.</sub>	1, 2, 3
I <sub>Ix</sub>	1, 2, 3
I <sub>OS</sub>	1, 2, 3
I <sub>CC</sub>	1, 2, 3

**Switching Characteristics**

Parameter	Subgroups
t <sub>CY</sub>	9, 10, 11
t <sub>A</sub>	9, 10, 11
t <sub>RV</sub>	9, 10, 11
t <sub>PW</sub>	9, 10, 11
t <sub>LZR</sub>	9, 10, 11
t <sub>DVR</sub>	9, 10, 11
t <sub>HZR</sub>	9, 10, 11
t <sub>HWZ</sub>	9, 10, 11
t <sub>SD</sub>	9, 10, 11
t <sub>HD</sub>	9, 10, 11
t <sub>FD</sub>	9, 10, 11
t <sub>HFD</sub>	9, 10, 11
t <sub>AFED</sub>	9, 10, 11
t <sub>RAF</sub>	9, 10, 11
t <sub>WAF</sub>	9, 10, 11

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