Low Power, 350 MHz Voltage Feedback Amplifier

AD8039-EP

FEATURES

- Low power: 1 mA quiescent current per amplifier
- High speed
  - −3 dB bandwidth (G = +1): 350 MHz
  - Slew rate: 425 V/µs
- Low cost
- Low noise
  - 8 nV/√Hz at 100 kHz
  - 600 fA/√Hz at 100 kHz
- Low input bias current: 750 nA maximum
- Low distortion
  - −90 dB SFDR at 1 MHz
  - −65 dB SFDR at 5 MHz
- Wide supply range: 3 V to 12 V
- Small packaging: 8-lead SOIC
- Supports defense and aerospace applications (AQEC standard)
- Extended temperature range: −55°C to +105°C
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- Battery-powered instrumentation
- Filters
- ADC drivers
- Level shifting
- Buffering
- Photo multipliers

FUNCTIONAL BLOCK DIAGRAM

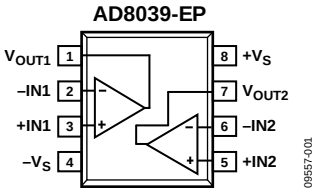

Figure 1. 8-Lead SOIC_N

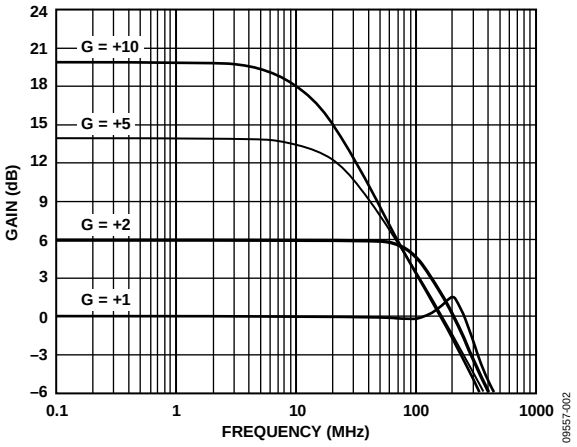

Figure 2. Small Signal Frequency Response for Various Gains, V_{OUT} = 500 mV p-p, V_S = ±5 V

GENERAL DESCRIPTION

The AD8039-EP dual amplifier is a high speed (350 MHz) voltage feedback amplifier with an exceptionally low quiescent current of 1.0 mA per amplifier typical (1.5 mA maximum). Despite its low power and low cost, the amplifier provides excellent overall performance. Additionally, it offers a high slew rate of 425 V/µs and a low input offset voltage of 3 mV maximum.

The Analog Devices, Inc., proprietary XFCB process allows low noise operation (8 nV/√Hz and 600 fA/√Hz) at extremely low quiescent currents. Given its wide supply voltage range (3 V to 12 V), wide bandwidth, and small packaging, the AD8039-EP amplifier is designed to work in a variety of applications where power and space are at a premium.

The AD8039-EP amplifier has a wide input common-mode range of 1 V from either rail and swings to within 1 V of each rail on the output. This amplifier is optimized for driving capacitive loads up to 20 pF. If driving larger capacitive loads, a small series resistor is needed to avoid excessive peaking or overshoot.

The AD8039-EP amplifier is available in an 8-lead SOIC package and is rated to work over the extended temperature range of −55°C to +105°C.

Additional application and technical information can be found in the AD8038/AD8039 data sheet.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

2/11—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = ±5 V, R_L = 2 kΩ, gain = +1, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.5 V p-p, T_{MIN} to T_{MAX}	300	350		MHz
	G = +2, V_{OUT} = 0.5 V p-p		175		MHz
	G = +1, V_{OUT} = 2 V p-p		100		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_{OUT} = 0.2 V p-p		45		MHz
Slew Rate	G = +1, V_{OUT} = 2 V step, R_L = 2 kΩ	400	425		V/µs
	T_{MIN} to T_{MAX}	300	325		V/µs
Overdrive Recovery Time	G = +2, 1 V overdrive		50		ns
Settling Time to 0.1%	G = +2, V_{OUT} = 2 V step		18		ns
NOISE/HARMONIC PERFORMANCE					
SFDR					
Second Harmonic	f_C = 1 MHz, V_{OUT} = 2 V p-p, R_L = 2 kΩ		−90		dBc
Third Harmonic	f_C = 1 MHz, V_{OUT} = 2 V p-p, R_L = 2 kΩ		−92		dBc
Second Harmonic	f_C = 5 MHz, V_{OUT} = 2 V p-p, R_L = 2 kΩ		−65		dBc
Third Harmonic	f_C = 5 MHz, V_{OUT} = 2 V p-p, R_L = 2 kΩ		−70		dBc
Crosstalk, Output-to-Output	f = 5 MHz, G = +2		−70		dB
Input Voltage Noise	f = 100 kHz		8		nV/√Hz
Input Current Noise	f = 100 kHz		600		fA/√Hz
DC PERFORMANCE					
Input Offset Voltage	T_A = 25°C		0.5	3	mV
	T_{MIN} to T_{MAX}			4.5	mV
Input Offset Voltage Drift			4.5		µV/°C
Input Bias Current	T_A = 25°C		400	750	nA
	T_{MIN} to T_{MAX}			2.0	µA
Input Bias Current Drift			3		nA/°C
Input Offset Current			±25		nA
Open-Loop Gain	V_{OUT} = ±2.5 V		70		dB
INPUT CHARACTERISTICS					
Input Resistance			10		MΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range	R_L = 1 kΩ		±4		V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V, T_A = 25°C	61	67		dB
	V_{CM} = ±2.5 V, T_{MIN} to T_{MAX}	59			dB
OUTPUT CHARACTERISTICS					
DC Output Voltage Swing	R_L = 2 kΩ, saturated output		±4		V
Capacitive Load Drive	30% overshoot, G = +2		20		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current per Amplifier	T_A = 25°C		1.0	1.5	mA
	T_{MIN} to T_{MAX}			2.6	mA
Power Supply Rejection Ratio					
−Supply	T_A = 25°C	71	77		dB
	T_{MIN} to T_{MAX}	63			dB
+Supply	T_A = 25°C	64	70		dB
	T_{MIN} to T_{MAX}	63			dB

T_A = 25°C, V_S = 5 V, R_L = 2 kΩ to V_S/2, gain = +1, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.2 V p-p, T_{MIN} to T_{MAX}	275	300		MHz
	G = +2, V_{OUT} = 0.2 V p-p		150		MHz
	G = +1, V_{OUT} = 2 V p-p		30		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_{OUT} = 0.2 V p-p		45		MHz
Slew Rate	G = +1, V_{OUT} = 2 V step, R_L = 2 kΩ	340	365		V/µs
	T_{MIN} to T_{MAX}	275	305		V/µs
Overdrive Recovery Time	G = +2, 1 V overdrive		50		ns
Settling Time to 0.1%	G = +2, V_{OUT} = 2 V step		18		ns
NOISE/HARMONIC PERFORMANCE					
SFDR					
Second Harmonic	f_C = 1 MHz, V_{OUT} = 2 V p-p, R_L = 2 kΩ		−82		dBc
Third Harmonic	f_C = 1 MHz, V_{OUT} = 2 V p-p, R_L = 2 kΩ		−79		dBc
Second Harmonic	f_C = 5 MHz, V_{OUT} = 2 V p-p, R_L = 2 kΩ		−60		dBc
Third Harmonic	f_C = 5 MHz, V_{OUT} = 2 V p-p, R_L = 2 kΩ		−67		dBc
Crosstalk, Output-to-Output	f = 5 MHz, G = +2		−70		dB
Input Voltage Noise	f = 100 kHz		8		nV/√Hz
Input Current Noise	f = 100 kHz		600		fA/√Hz
DC PERFORMANCE					
Input Offset Voltage	T_A = 25°C		0.8	3	mV
	T_{MIN} to T_{MAX}			4.5	mV
Input Offset Voltage Drift			3		µV/°C
Input Bias Current	T_A = 25°C		400	750	nA
	T_{MIN} to T_{MAX}			2.0	µA
Input Bias Current Drift			3		nA/°C
Input Offset Current			±30		nA
Open-Loop Gain	V_{OUT} = ±2.5 V		70		dB
INPUT CHARACTERISTICS					
Input Resistance			10		MΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range	R_L = 1 kΩ		1.0 to 4.0		V
Common-Mode Rejection Ratio	V_{CM} = ±1 V, T_A = 25°C	59	65		dB
	V_{CM} = ±1 V, T_{MIN} to T_{MAX}	59			dB
OUTPUT CHARACTERISTICS					
DC Output Voltage Swing	R_L = 2 kΩ, saturated output		0.9 to 4.1		V
Capacitive Load Drive	30% overshoot, G = +2		20		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current per Amplifier	T_A = 25°C		0.9	1.5	mA
Power Supply Rejection Ratio	T_{MIN} to T_{MAX}	65	71		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	12.6 V
Power Dissipation	See Figure 3
Common-Mode Input Voltage	$\pm V_S$
Differential Input Voltage	±4 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−55°C to +105°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8039-EP package is limited by the associated rise in junction temperature (T_J) on the die. The plastic encapsulating the die locally reaches the junction temperature. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8039-EP. Exceeding a junction temperature of 175°C for an extended time can result in changes in the silicon devices, potentially causing failure.

The still-air thermal properties of the package and PCB (θ_{JA}), ambient temperature (T_A), and total power dissipated in the package (P_D) determine the junction temperature of the die. The junction temperature can be calculated as

$$T_J = T_A + (P_D \times \theta_{JA})$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) multiplied by the quiescent current (I_S). Assuming the load (R_L) is referenced to midsupply, the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$). The difference between the total drive power and the load power is the drive power dissipated in the package.

$$P_D = \textit{quiescent power} + (\textit{total drive power} - \textit{load power})$$

$$P_D = [V_S \times I_S] + [(V_S/2) \times (V_{OUT}/R_L)] - [V_{OUT}^2/R_L]$$

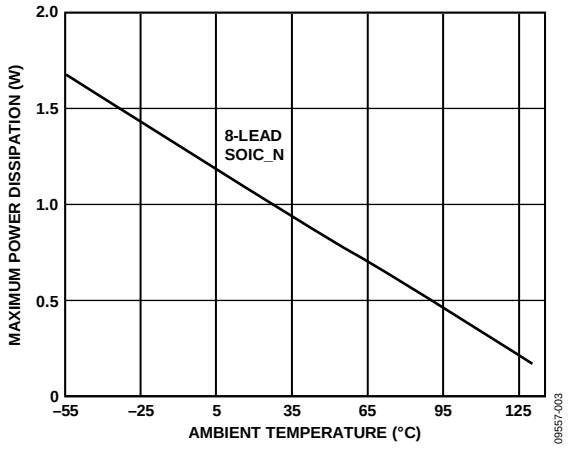

Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

RMS output voltages should be considered. If R_L is referenced to $-V_S$, as in single-supply operation, then the total drive power is $V_S \times I_{OUT}$. If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply.

$$P_D = (V_S \times I_S) + (V_S/4)^2/R_L$$

In single-supply operation with R_L referenced to $-V_S$, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, throughholes, ground, and power planes reduces θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 8-lead SOIC_N (125°C/W) on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

OUTPUT SHORT CIRCUIT

Shorting the output to ground or drawing excessive current from the AD8039-EP will likely cause a catastrophic failure.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±5 V, C_L = 5 pF, R_G = R_F = 1 kΩ, R_L = 2 kΩ, frequency = 1 MHz, T_A = −55°C to +105°C, unless otherwise noted.

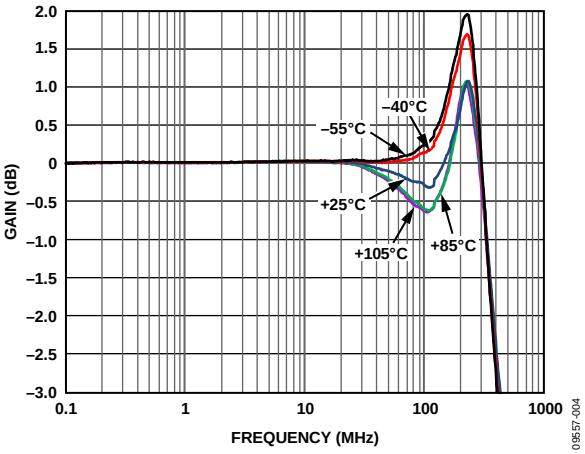

Figure 4. Small Signal Frequency Response vs. Temperature, Gain = +1, V_S = ±5 V, V_{OUT} = 500 mV p-p

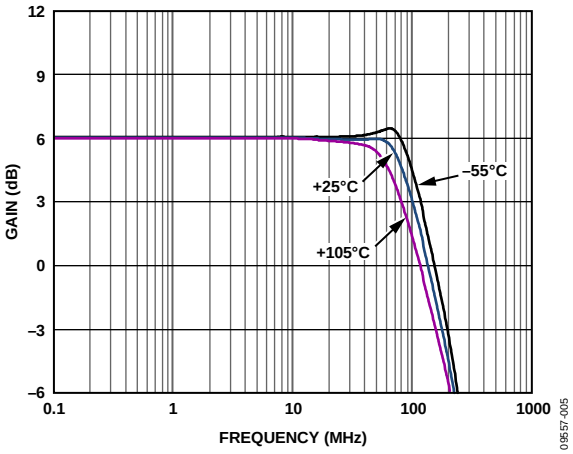

Figure 5. Large Signal Frequency Response vs. Temperature, Gain = +2, V_S = ±5 V, V_{OUT} = 2 V p-p

OUTLINE DIMENSIONS

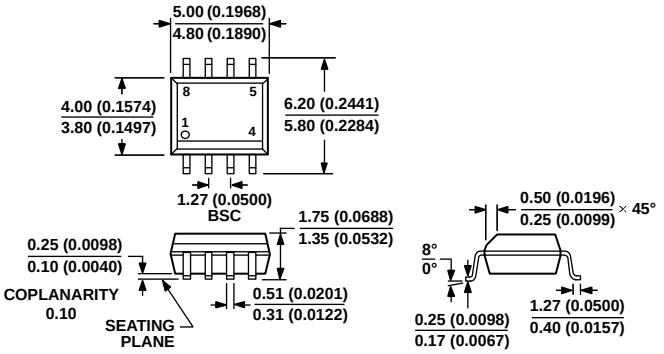

Figure 6. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8039SRZ-EPR7	−55°C to +105°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8

[1] Z = RoHS Compliant Part.

NOTES

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