Am29821/823/825

High Performance Bus Interface Registers

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High-speed parallel registers with positive edge-triggered D-type flip-flops**
  - Noninverting CP-Y t_{PD} = 7.5 ns typ
  - Inverting CP-Y t_{PD} = 7.5 ns typ
- **Buffered common Clock Enable ($\overline{EN}$)**
- **Buffered common asynchronous Clear input ($\overline{CLR}$)**
- **Three-state outputs glitch free during power-up and down**
- **Outputs have Schottky clamp to ground**
- **48 mA Commercial I_{OL}**
- **Low input/output capacitance**
  - 6 pF inputs (typical)
  - 8 pF outputs (typical)
- **Metastable "Hardened" Registers**
- **I_{OH} specified at 2.0 V and 2.4 V**
- **24-pin 0.3" space saving package**
- **IMOX™ high performance IMplanted OXide isolated process**

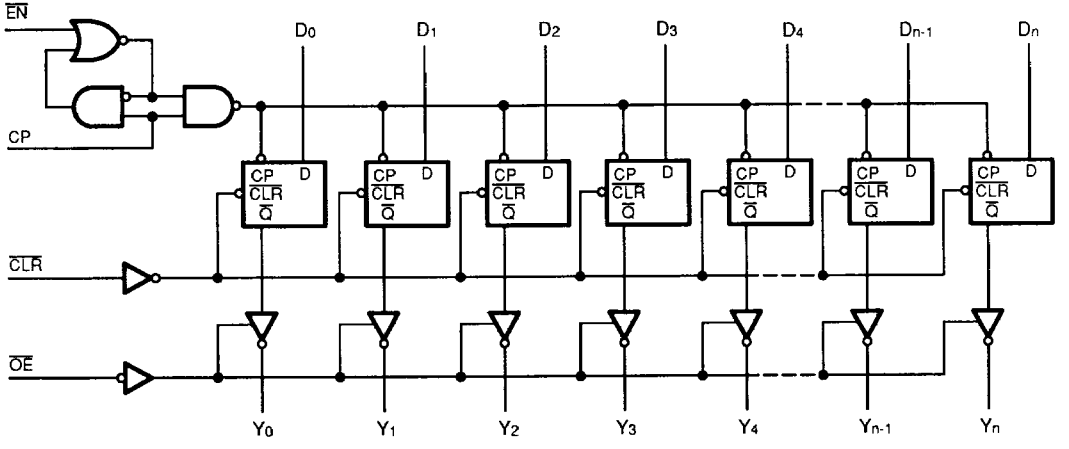
GENERAL DESCRIPTION

The Am29821/823/825 bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The Am29821 is a buffered, 10-bit wide version of the popular '374/'534 functions. The Am29823 is a 9-bit wide buffered register with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high performance microprogrammed systems. The Am29825 is an 8-bit buffered register with all the '823 controls plus multiple enables ($\overline{OE_1}$, $\overline{OE_2}$, $\overline{OE_3}$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. It is ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

BLOCK DIAGRAMS

Am29821



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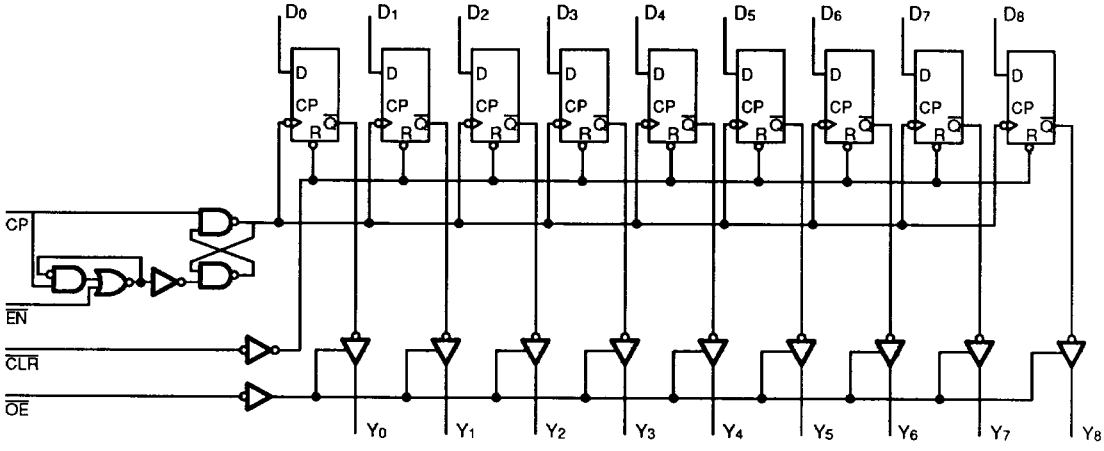
BLOCK DIAGRAMS (Continued)

Am29823



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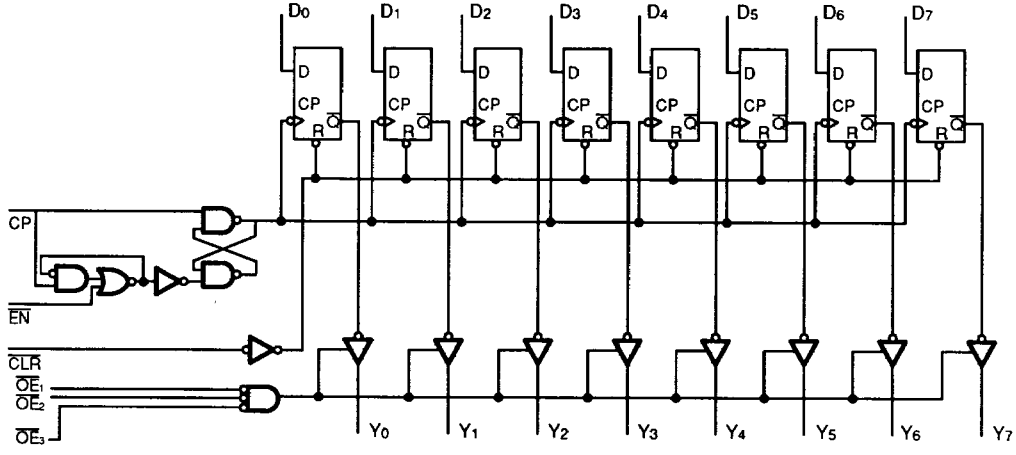
Am29825



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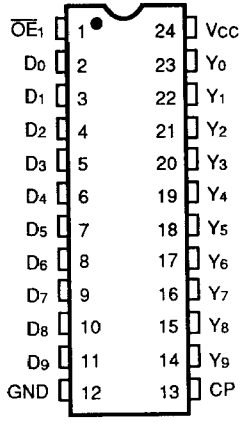
CONNECTION DIAGRAMS
Top View

Am29821

DIP



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Am29823

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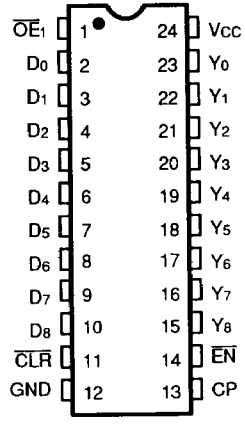

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Am29825

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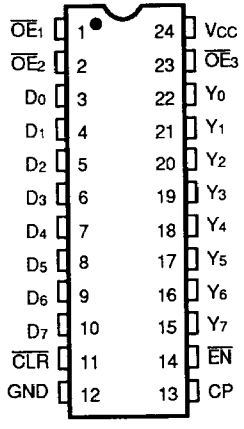

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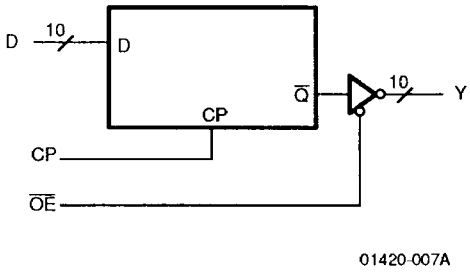
LOGIC SYMBOLS

Am29821
10-Bit Register



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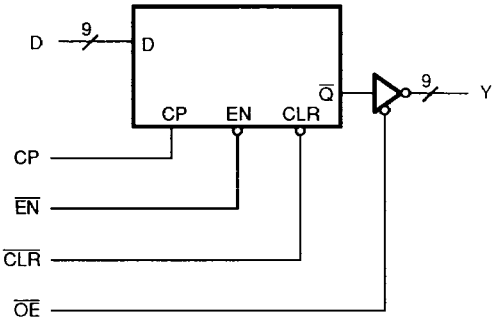
Am29823
9-Bit Register



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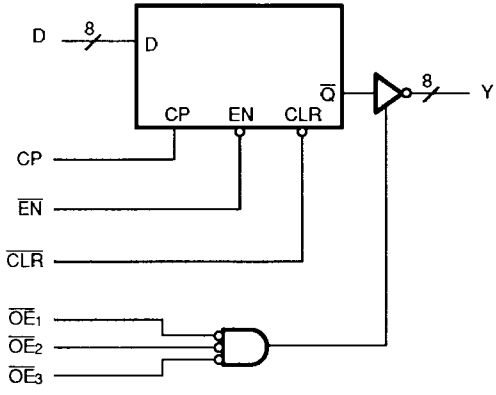
Am29825
8-Bit Register



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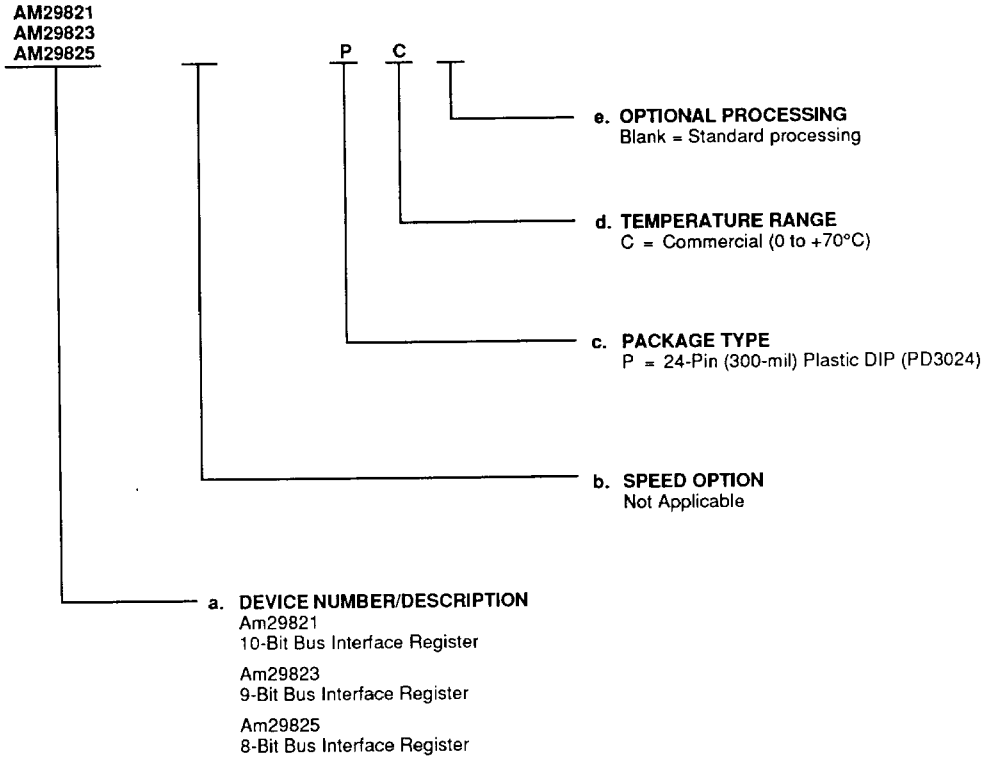
ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29821	PC
AM29823	
AM29825	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

D_i

The D flip-flop data inputs.

$\overline{CLR}$

For both inverting and noninverting register, when the clear input is LOW and $\overline{OE}$ is LOW, the Q_i outputs are LOW. When the clear input is HIGH, data can be entered into the register.

CP

Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.

Y_i

The register three-state outputs.

$\overline{EN}$

Clock Enable. When the clock enable is LOW, data on the D_i input is transferred to the Q_i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_i outputs do not change state, regardless of the data or clock input transitions. (Note 1.)

$\overline{OE}$

Output Control. When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y outputs.

Note:

1. The Am29823 and Am29825 registers achieve short throughput delay and setup time and reduced power consumption by means of a clock gating and latching circuit. This circuit is sensitive to very short (<3 ns) HIGH-to-LOW-to-HIGH going spikes on $\overline{EN}$ while CP is HIGH. The designer should be aware of this and avoid the use of decoders or other potentially glitching devices in the $\overline{EN}$ logic.

FUNCTION TABLE

Inputs					Internal	Outputs	
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_i	CP	Q_i	Y_i	Function
H	X	L	L	↑	L	Z	Hi-Z
H	X	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +5.5 V
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	100 mA
DC Input Current	−30 mA to +5.0 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature, (T_A)	0°C to +70°C
Supply Voltage, (V_{CC})	5.0 V ± 10%
	4.5 V to 5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA	2.4		V
			I_{OH} = −24 mA	2.0		
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48 mA		0.5	V
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0		V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	V
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA			−1.2	V
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.4 V	Data, $\overline{CLR}$		−1.0	mA
			$\overline{OE}$, $\overline{EN}$, CP		−2.0	
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V			50	µA
I_I	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V			1.0	mA
I_{OZ}	Output Off-State (Hi-Z) Output Current	V_{CC} = 5.5 V	V_O = 0.4 V		−50	µA
			V_O = 2.4 V		50	
I_{SC}	Output Short Circuit Current (Note 1)	V_{CC} = 5.5 V		−75	−250	mA
I_{CC}	Supply Current (Note 2)	V_{CC} = 5.5 V, Outputs Open, $\overline{EN}$ = LOW	Over Temperature Range		140	mA
			+70°C		130	mA

Notes:

1. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
2. Clock input, CP, is HIGH after clocking in data to produce outputs = LOW.

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Parameter Symbol	Parameter Description		Test Conditions (Note 1)	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay Clock to Y_i ($\overline{OE}$ = LOW)		C_L = 50 pF	3.5		8.5	ns
t_{PHL}				3.5		10.5	ns
t_{PLH}			C_L = 300 pF			14	ns
t_{PHL}						18	ns
t_S	Data to CP Setup Time		C_L = 50 pF	2.0	0		ns
t_H	Data to CP Hold Time			2.0	0.5		ns
t_S	Enable ($\overline{EN}$ ↓) to CP Setup Time			3.0	1.5		ns
t_S	Enable ($\overline{EN}$ ↑) to CP Setup Time			3.0	1.5		ns
t_H	Enable ($\overline{EN}$) Hold Time			0	–1.5		ns
t_{PHL}	Propagation Delay, Clear to Y_i				12.9	15.0	ns
t_S	Clear Recovery ($\overline{CLR}$ ↑) Time			5.0	1.1		ns
t_{PWH}	Clock Pulse Width	HIGH	C_L = 50 pF	5.0	3.5		ns
t_{PWL}		LOW		5.0	3.0		ns
t_{PWL}	Clear ($\overline{CLR}$ = LOW) Pulse Width			5.0	4.0		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ↓ to Y_i		C_L = 300 pF			17	ns
t_{ZL}						21	ns
t_{ZH}			C_L = 50 pF		11.5	12	ns
t_{ZL}					11.0	12	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ↑ to Y_i		C_L = 50 pF			9	ns
t_{LZ}						9	ns
t_{HZ}			C_L = 5 pF		5.2	8	ns
t_{LZ}					5.5	8	ns

Note:

1. See test circuit and waveforms (Chapter 2).

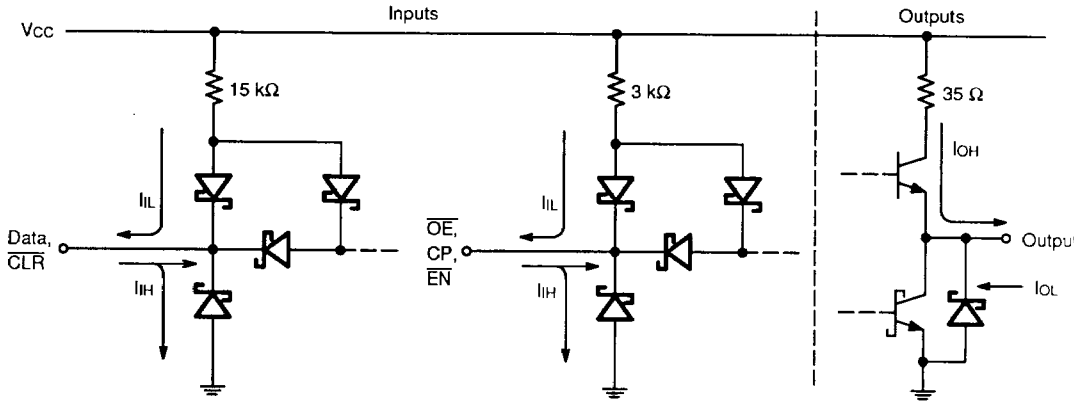
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description		Test Conditions (Note 1)	Min.	Max.	Unit
t_{PLH}	Propagation Delay Clock to Y_i ($\overline{OE}$ = LOW)		C_L = 50 pF	3.5	10	ns
t_{PHL}				3.5	12	ns
t_{PLH}			C_L = 300 pF		16	ns
t_{PHL}					20	ns
t_S	Data to CP Setup Time		C_L = 50 pF	4		ns
t_H	Data to CP Hold Time			2		ns
t_S	Enable ($\overline{EN}$ ↓) to CP Setup Time			4		ns
t_S	Enable ($\overline{EN}$ ↑) to CP Setup Time			4		ns
t_H	Enable ($\overline{EN}$) Hold Time			2		ns
t_{PHL}	Propagation Delay, Clear to Y_i				20	ns
t_S	Clear Recovery ($\overline{CLR}$ ↑) Time			7		ns
t_{PWH}	Clock Pulse Width	HIGH		7		ns
t_{PWL}		LOW		7		ns
t_{PWL}	Clear ($\overline{CLR}$ = LOW) Pulse Width			7		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ↓ to Y_i		C_L = 300 pF		20	ns
t_{ZL}					23	ns
t_{ZH}			C_L = 50 pF		14	ns
t_{ZL}					14	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ↑ to Y_i		C_L = 50 pF		16	ns
t_{LZ}					12	ns
t_{HZ}			C_L = 5 pF		9	ns
t_{LZ}					9	ns

Note:

1. See test circuit and waveforms (Chapter 2).

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



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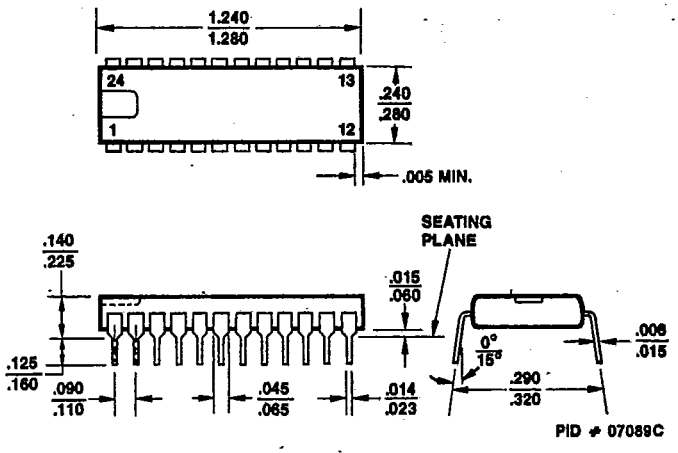
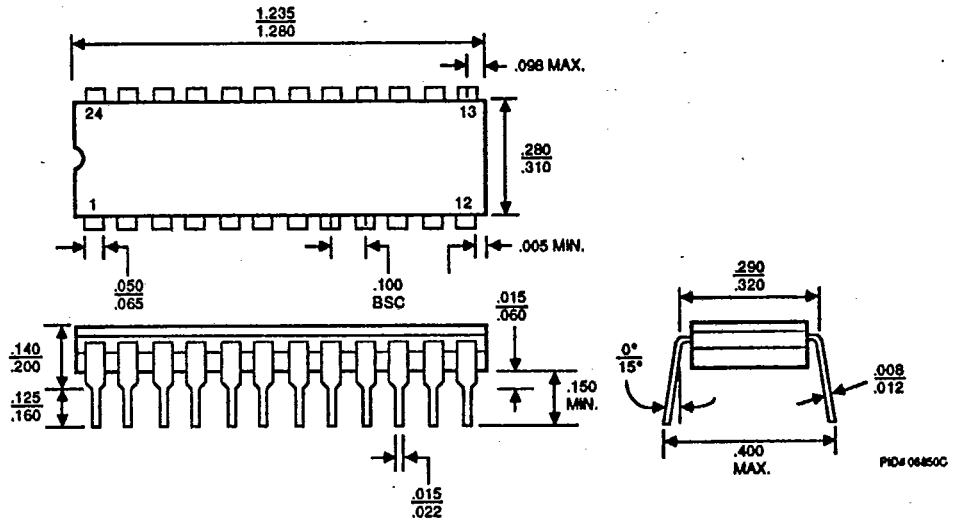
PACKAGE OUTLINES*

T-90-20

PD3024



CD3024

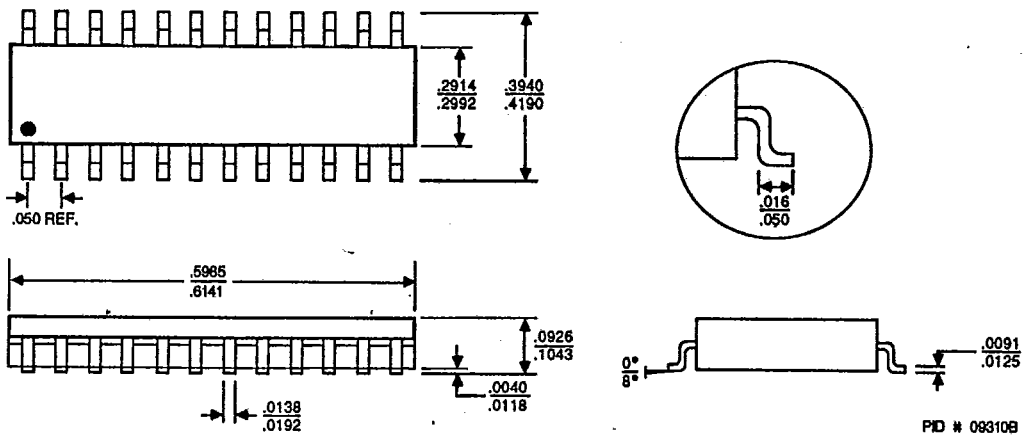


*For reference only.

PACKAGE OUTLINES (Cont'd.)

T-90-20

SO 024



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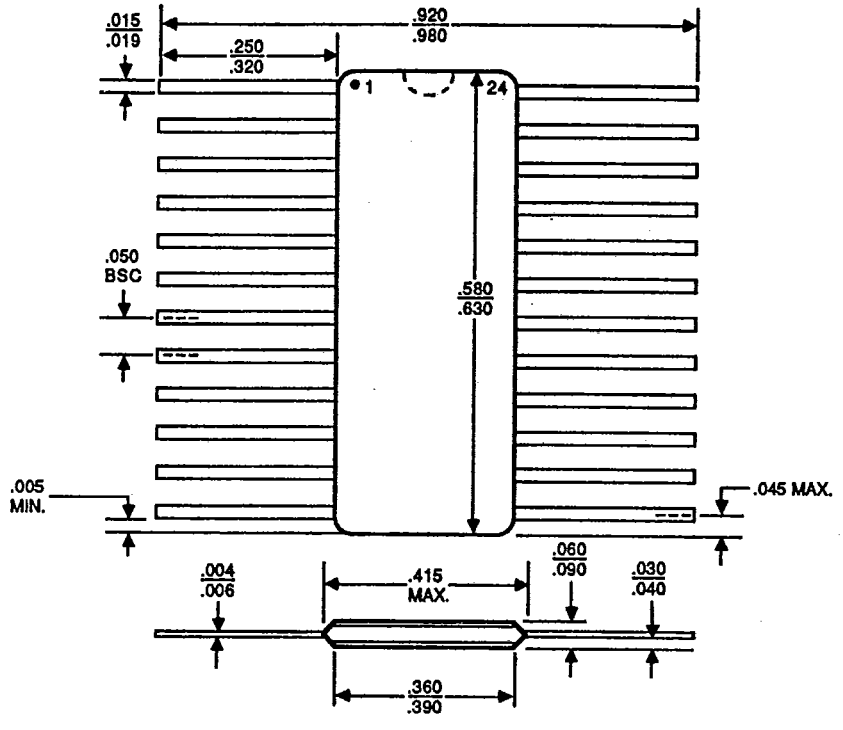

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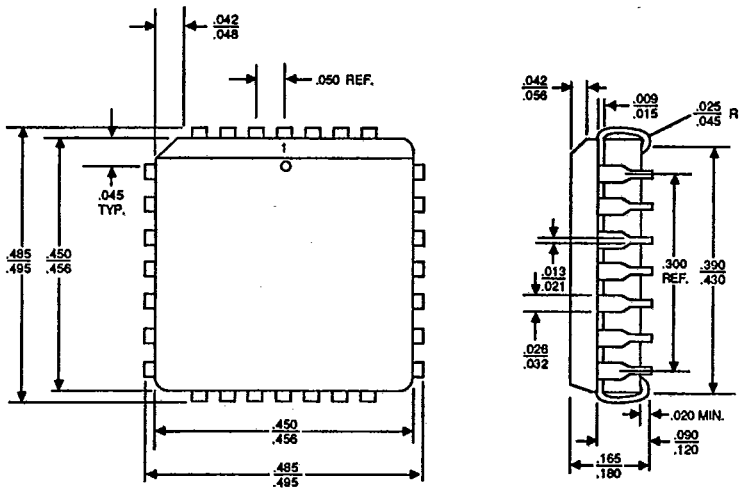
PACKAGE OUTLINES (Cont'd.)

T-90-20

PL 028



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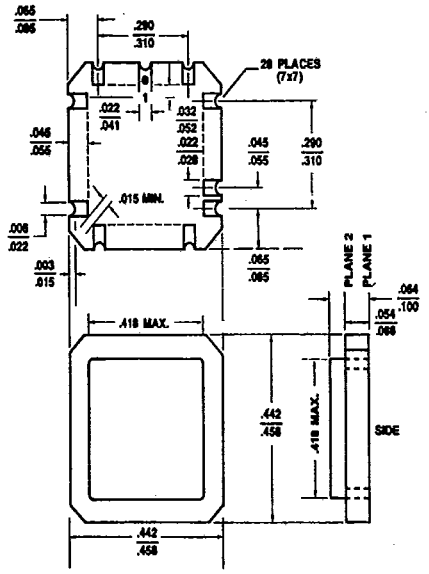
CL 028



PID # 06595D

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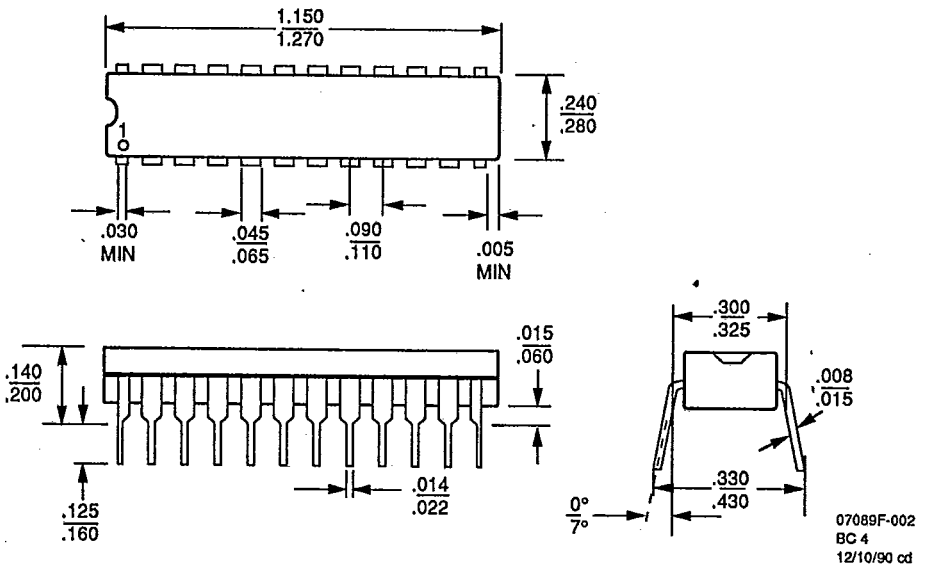
Printed in U.S.A. AIS-WCP-20M-01/88-0

T-90-20

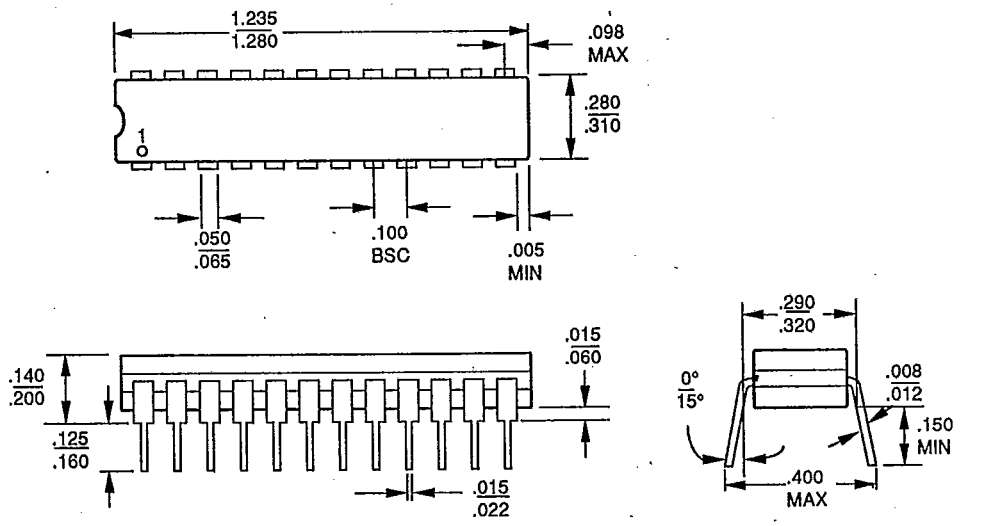
PD3024
24-Pin 300-mil Plastic SKINNYDIP



07089F-002
BC 4
12/10/90 cd

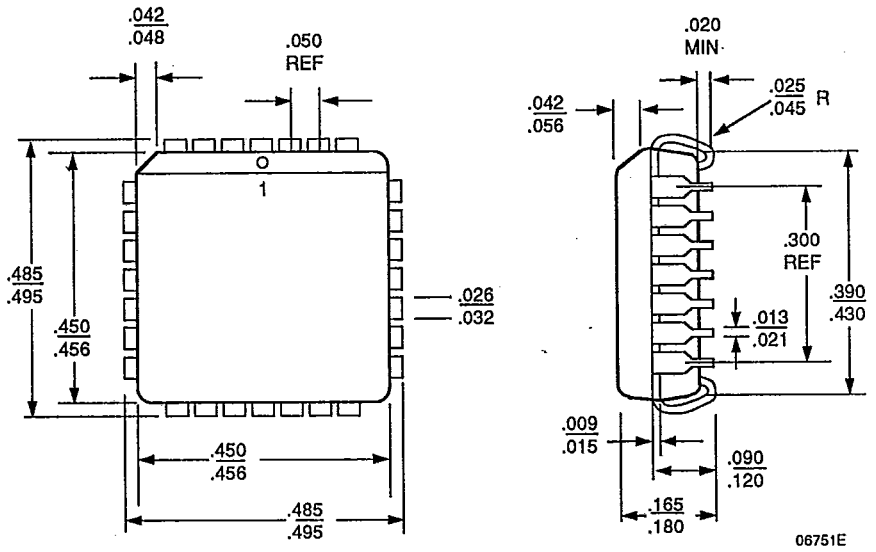
Note:
For reference only. All dimensions measured in inches. BSC is an ANSI standard for Basic Space Centering.

CD3024
24-Pin 300-mil Ceramic SKINNYDIP



06850C

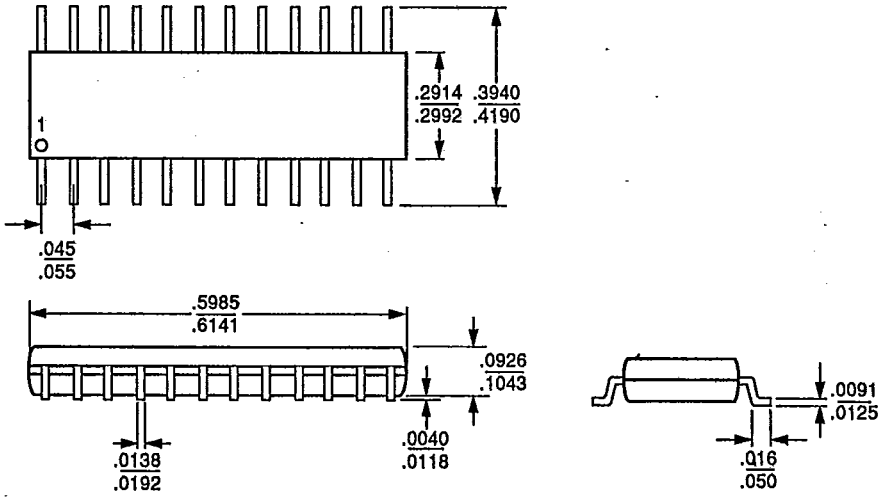
PL 028
28-Pin Plastic Leaded Chip Carrier



06751E

SO 024
24-Pin Plastic Small Outline Package

T-90-20



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