

HEF4021B

8-bit static shift register

Rev. 8 — 18 November 2011

Product data sheet

1. General description

The HEF4021B is an 8-bit static shift register (parallel-to-serial converter) with a synchronous serial data input (DS), a clock input (CP), an asynchronous active HIGH parallel load input (PL), eight asynchronous parallel data inputs (D0 to D7) and buffered parallel outputs from the last three stages (Q5 to Q7).

Each register stage is a D-type master-slave flip-flop with a set direct (SD) and clear direct (CD) input. Information on D0 to D7 is asynchronously loaded into the register while PL is HIGH, independent of CP and DS. When PL is LOW, data on DS is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of CP. Schmitt trigger action makes the clock input highly tolerant of slower rise and fall times.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2. Features and benefits

- Tolerant of slower rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

3. Ordering information

Table 1. Ordering information

All types operate from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$.

Type number	Package	Description	Version
	Name		
HEF4021BP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
HEF4021BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1



4. Functional diagram

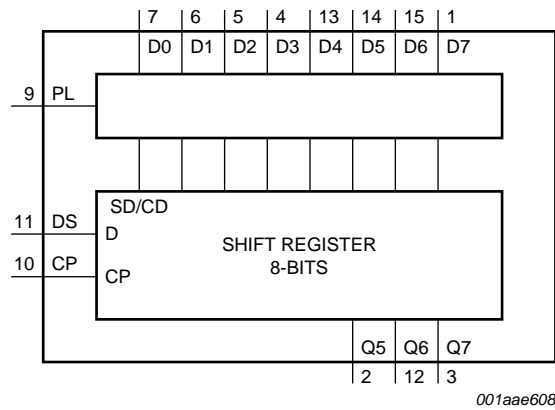


Fig 1. Functional diagram

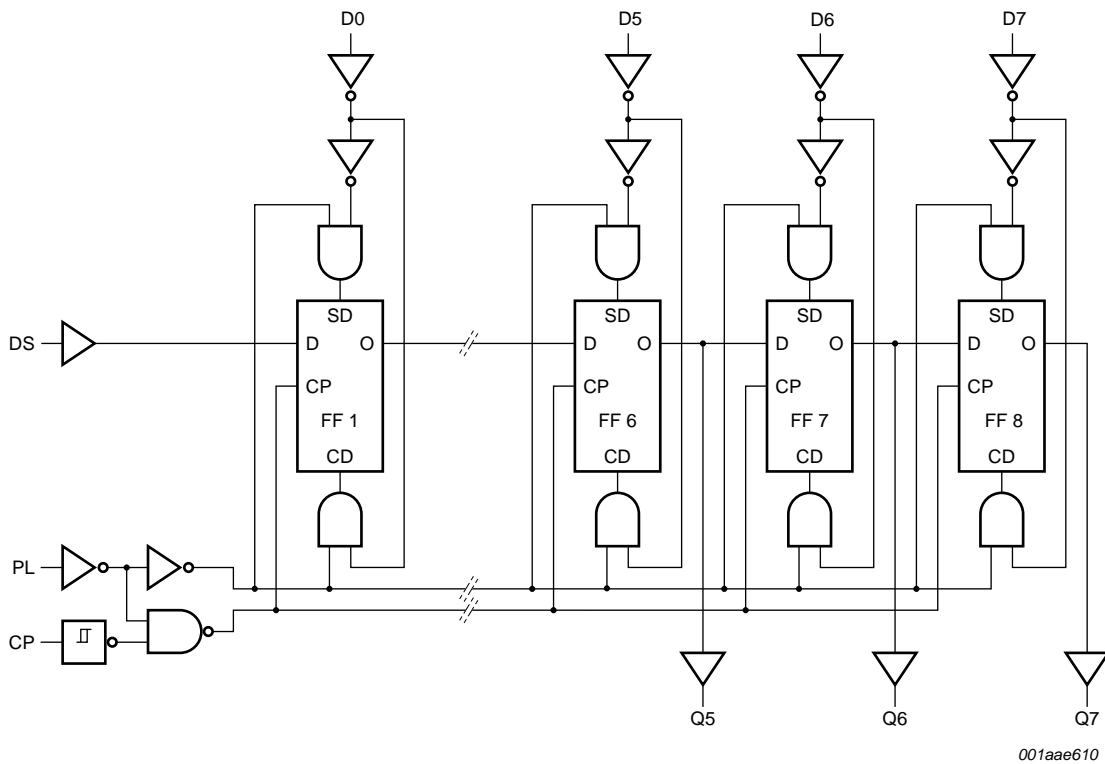


Fig 2. Logic diagram

5. Pinning information

5.1 Pinning

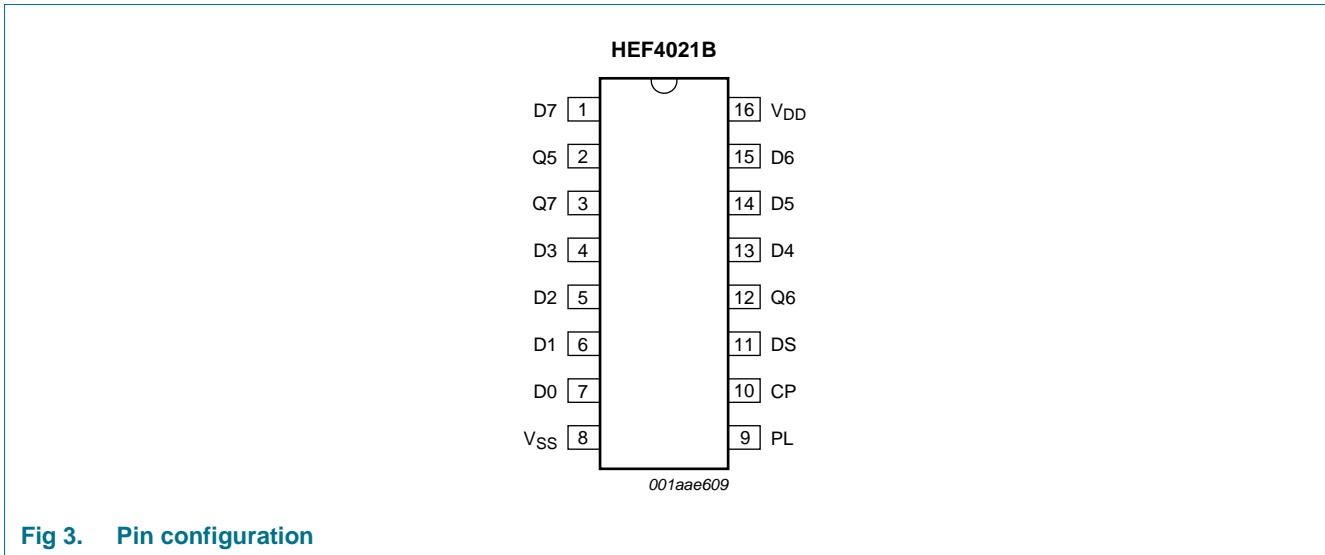


Fig 3. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q5 to Q7	2, 12, 3	buffered parallel output from the last three stages
D0 to D7	7, 6, 5, 4, 13, 14,15, 1	parallel data input
V _{SS}	8	ground supply voltage
PL	9	parallel load input
CP	10	clock input (LOW-to-HIGH edge-triggered)
DS	11	serial data input
V _{DD}	16	supply voltage

6. Functional description

Table 3. Function table^[1]

Number of clock transitions	Inputs			Outputs		
	CP	DS	PL	Q5	Q6	Q7
Serial operation						
1	↑	data 1	L	X	X	X
2	↑	data 2	L	X	X	X
3	↑	data 3	L	X	X	X
6	↑	X	L	data 1	X	X
7	↑	X	L	data 2	data 1	X

Table 3. Function table^[1] ...continued

Number of clock transitions	Inputs			Outputs		
	CP	DS	PL	Q5	Q6	Q7
8	↑	X	L	data 3	data 2	data 1
	↓	X	L	no change	no change	no change
Parallel operation						
	X	X	H	D5	D6	D7

- [1] H = HIGH voltage level; L = LOW voltage level; X = don't care;
 ↑ = LOW to HIGH clock transition; ↓ = HIGH to LOW clock transition;
 data n = data (HIGH or LOW) on the DS input at the nth ↑ CP transition.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V _{DD}	supply voltage		-0.5	+18	V	
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{DD} + 0.5 V	-	±10	mA	
V _I	input voltage		-0.5	V _{DD} + 0.5	V	
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{DD} + 0.5 V	-	±10	mA	
I _{I/O}	input/output current		-	±10	mA	
I _{DD}	supply current		-	50	mA	
T _{stg}	storage temperature		-65	+150	°C	
T _{amb}	ambient temperature		-40	+125	°C	
P _{tot}	total power dissipation	T _{amb} -40 °C to +125 °C				
		DIP16 package	[1]	-	750	mW
		SO16 package	[2]	-	500	mW
P	power dissipation	per output	-	100	mW	

- [1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.
 [2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DD}	supply voltage		3	-	15	V
V _I	input voltage		0	-	V _{DD}	V
T _{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{DD} = 5 V	-	-	3.75	μs/V
		V _{DD} = 10 V	-	-	0.5	μs/V
		V _{DD} = 15 V	-	-	0.08	μs/V

9. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	$T_{amb} = -40\text{ }^{\circ}\text{C}$		$T_{amb} = 25\text{ }^{\circ}\text{C}$		$T_{amb} = 85\text{ }^{\circ}\text{C}$		$T_{amb} = 125\text{ }^{\circ}\text{C}$		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
I_{OL}	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
I_I	input leakage current	$V_{DD} = 15\text{ V}$	15 V	-	± 0.1	-	± 0.1	-	± 1.0	-	± 1.0	μA
I_{DD}	supply current	$I_O = 0\text{ A}$	5 V	-	5	-	5	-	150	-	150	μA
			10 V	-	10	-	10	-	300	-	300	μA
			15 V	-	20	-	20	-	600	-	600	μA
C_I	input capacitance	-	-	-	-	7.5	-	-	-	-	pF	

10. Dynamic characteristics

Table 7. Dynamic characteristics

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; for test circuit see [Figure 7](#); unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	CP to Qn see Figure 4	5 V	[1] 98 ns + (0.55 ns/pF) C_L	-	125	250	ns
			10 V	44 ns + (0.23 ns/pF) C_L	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF) C_L	-	40	80	ns
		PL to Qn see Figure 4	5 V	93 ns + (0.55 ns/pF) C_L	-	120	240	ns
			10 V	44 ns + (0.23 ns/pF) C_L	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF) C_L	-	40	80	ns

Table 7. Dynamic characteristics ...continued
 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; for test circuit see [Figure 7](#); unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula	Min	Typ	Max	Unit
t _{PLH}	LOW to HIGH propagation delay	CP to Qn see Figure 4	5 V	[1] 88 ns + (0.55 ns/pF)C _L	-	115	230	ns
			10 V	39 ns + (0.23 ns/pF)C _L	-	50	100	ns
			15 V	32 ns + (0.16 ns/pF)C _L	-	40	80	ns
		PL to Qn see Figure 4	5 V	78 ns + (0.55 ns/pF)C _L	-	105	210	ns
			10 V	39 ns + (0.23 ns/pF)C _L	-	50	100	ns
			15 V	32 ns + (0.16 ns/pF)C _L	-	40	80	ns
t _t	transition time	Qn; see Figure 4	5 V	[1] 10 ns + (1.00 ns/pF)C _L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C _L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C _L	-	20	40	ns
t _{su}	set-up time	DS to CP; see Figure 5	5 V		+25	-15	-	ns
			10 V		+25	-10	-	ns
			15 V		+15	-5	-	ns
		Dn to PL; see Figure 6	5 V		50	25	-	ns
			10 V		30	10	-	ns
			15 V		20	5	-	ns
t _h	hold time	DS to CP; see Figure 5	5 V		40	20	-	ns
			10 V		20	10	-	ns
			15 V		15	8	-	ns
		Dn to PL; see Figure 6	5 V		+15	-10	-	ns
			10 V		15	0	-	ns
			15 V		15	0	-	ns
t _w	pulse width	CP = LOW; minimum width; see Figure 5	5 V		70	35	-	ns
			10 V		30	15	-	ns
			15 V		24	12	-	ns
		PL = HIGH; minimum width; see Figure 6	5 V		70	35	-	ns
			10 V		30	15	-	ns
			15 V		24	12	-	ns
t _{rec}	recovery time	PL input; see Figure 6	5 V		50	10	-	ns
			10 V		40	5	-	ns
			15 V		35	5	-	ns
f _{clk(max)}	maximum clock frequency	CP input; see Figure 5	5 V		6	13	-	MHz
			10 V		15	30	-	MHz
			15 V		20	40	-	MHz

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. $V_{SS} = 0\text{ V}$; $t_r = t_f \leq 20\text{ ns}$; $T_{amb} = 25\text{ }^\circ\text{C}$.

Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 900 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz,
		10 V	$P_D = 4300 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_o = output frequency in MHz,
		15 V	$P_D = 12000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	C_L = output load capacitance in pF, V_{DD} = supply voltage in V, $\Sigma(f_o \times C_L)$ = sum of the outputs.

11. Waveforms

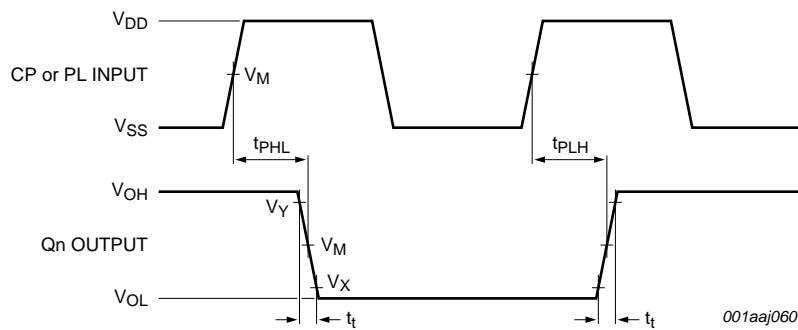


Fig 4. Waveforms showing propagation delays for CP and PL inputs to Qn output and Qn transition times

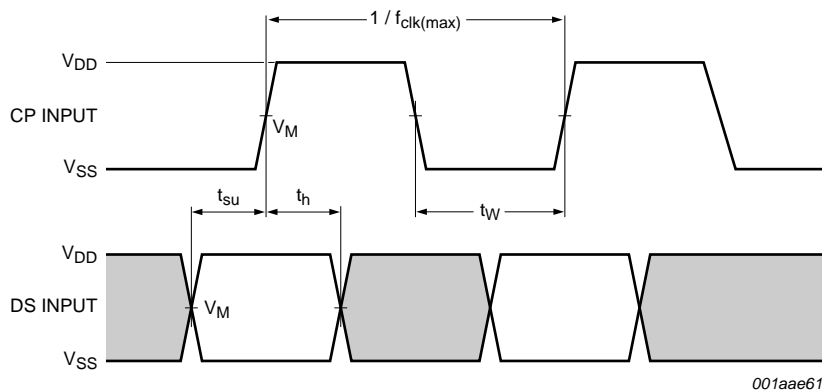
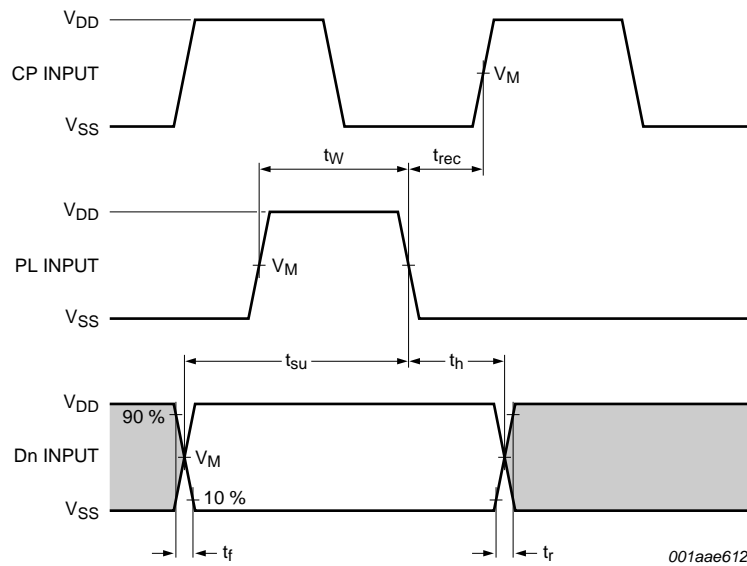


Fig 5. Waveforms showing minimum clock pulse width, set-up time, and hold time for CP and DS.

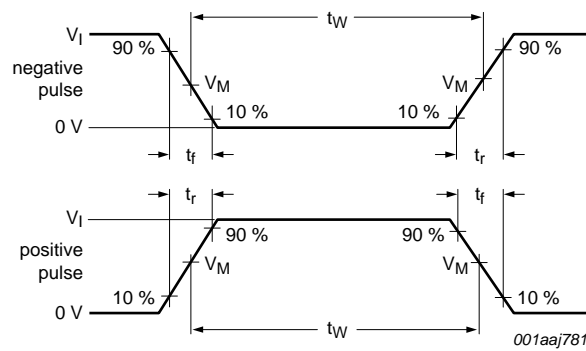


Set-up times and hold times are shown as positive values but may be specified as negative values; Measurement points are given in [Table 9](#).

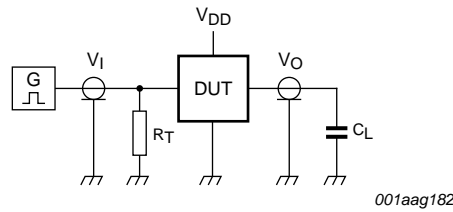
Fig 6. Waveforms showing minimum pulse width and recovery time for PL; set-up and hold times for Dn to PL.

Table 9. Measurement points

Supply voltage	Input	Output		
V _{DD}	V _M	V _M	V _X	V _Y
5 V to 15 V	0.5V _{DD}	0.5V _{DD}	0.1V _{DD}	0.9V _{DD}



a. Input waveform



b. Test circuit

Test data is given in [Table 10](#).

Definitions for test circuit:

DUT = Device Under Test.

C_L = load capacitance including jig and probe capacitance.

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig 7. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input	Load
V_{DD}	V_I	C_L
5 V to 15 V	V_{SS} or V_{DD}	50 pF
	t_r, t_f	≤ 20 ns

12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

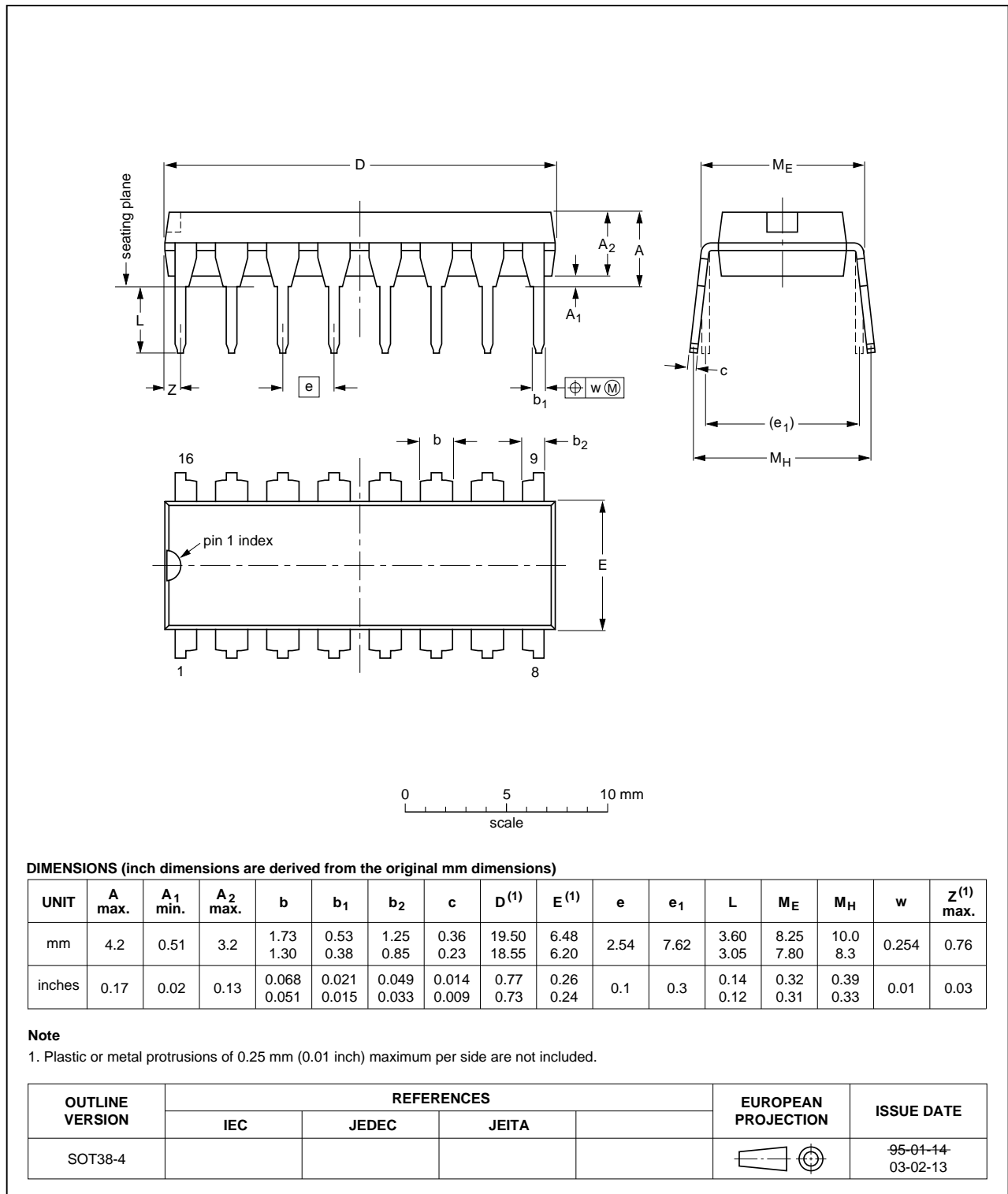


Fig 8. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

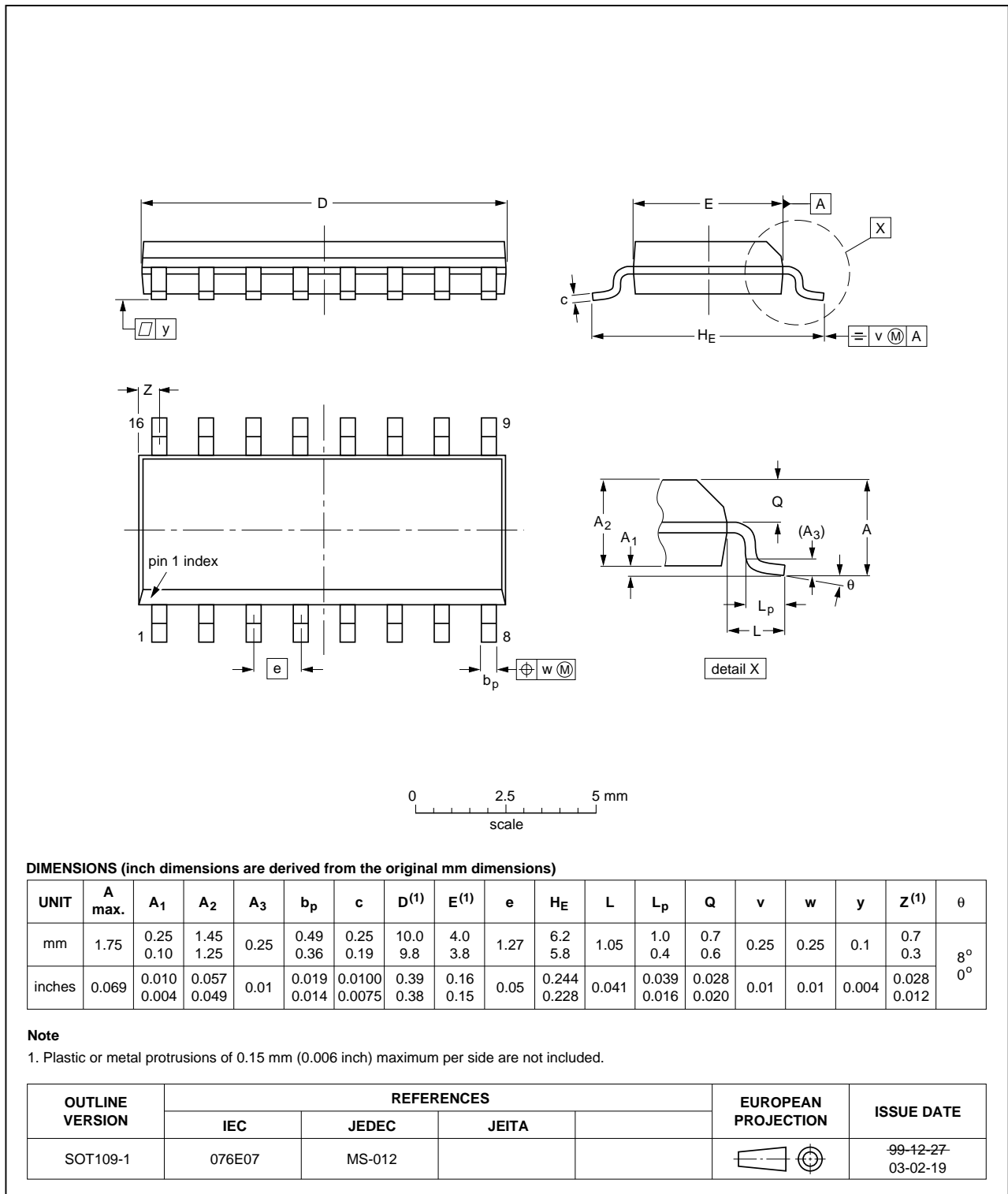


Fig 9. Package outline SOT109-1 (SO16)

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4021B v.8	20111118	Product data sheet	-	HEF4021B v.7
Modifications:		<ul style="list-style-type: none">• Legal pages updated.• Changes in “General description” and “Features and benefits”.• Section “Applications” removed.		
HEF4021B v.7	20111010	Product data sheet	-	HEF4021B v.6
HEF4021B v.6	20091127	Product data sheet	-	HEF4021B v.5
HEF4021B v.5	20090707	Product data sheet	-	HEF4021B v.4
HEF4021B v.4	20081110	Product data sheet	-	HEF4021B_CNV v.3
HEF4021B_CNV v.3	19950101	Product specification	-	HEF4021B_CNV v.2
HEF4021B_CNV v.2	19950101	Product specification	-	-

14. Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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